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STANDARD AVIONICS MODULES (SAM) FOR EXISTING MODEMS

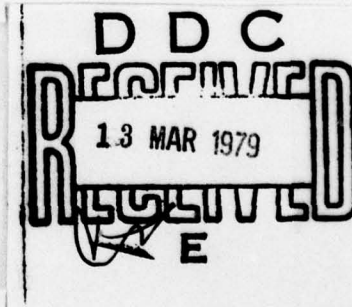
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The objective of this project was to demonstrate the feasibility and cost effectiveness of applying the Standard Avionic Modules concept to communication/navigation ECCM modems. To make the project more tractable and more relevant, two L-band com/nav systems and a general PN PSK modem were considered. The two com/nav systems were JTIDS and GPS, and the PN PSK modem was an AJ modem using PN spreading and was capable of a data rate of 38.4 KBPS.		

20. Abstract - Continued

A performance analysis resulted in a set of composite performance requirements. Signal processing functions were defined which would satisfy the performance requirements. With the performance requirements and signal processing functions several architectures were analyzed and partitioning of the modem function was undertaken.

The final configuration of the modem was directly dependent upon the physical packaging technique adapted. The Navy SHP approach was compared to the Air Force ATR standard, specifically the 1/2 ATR standard and was discarded because of several deficiencies.

- a. The basic module is physically too small to allow complex signal processing functions
- b. Module dimensions restrict signal input/output such that digital function in LSI form could not be accommodated
- c. SHP modules do not accommodate RF circuits
- d. Thermal design was inferior to the Air Force standard.

The final architecture selected was digital in nature, with a programmable microprocessor as its core. The signal was digitized as soon as it was amplified, and filtered. The microprocessor performed the post correlation digital signal processing - acquisition, tracking, demodulation, bit synchronization, and the modem control functions. The other Standard Avionic Modules fabricated and tested were: the IF amplifier (IFA), the frequency generator, (FGN), and the modulator (MOD).

Several conclusions were reached:

- a. Application of the SAM concept to JTIDS, GPS, and the PN PSK modem is feasible and offers potential cost savings
- b. The final digital architecture is superior to an analog based design for several reasons:
 1. Easily and cost-effectively adapted to individual waveforms without major hardware changes e.g., plug-in filters, programmable frequencies, programmable firmware
 2. Digital circuits are more stable and therefore require less maintenance
 3. Digital circuits are more amenable to microminiaturization, i.e., LSI and therefore could cost much less.
- c. The Air Force ATR packaging standard is superior to the Navy SHP approach for tactical aircraft integrated CNI systems.

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FOREWORD

This final technical report covers the work performed between July 1976 and December 1977 under contract number F33615-76-C-1307. It was prepared by TRW Defense and Space Systems Group, Redondo Beach, California for the Air Force Avionics Laboratory (AFAL), Wright-Patterson Air Force Base, Ohio. Mr. Larry L. Gutman was the AFAL Project Engineer for the contract.

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ABBREVIATIONS

ACQ	Acquisition
A/D	Analog to Digital
C/A	Clear Acquisition Code
CCSK	Cyclic Code Shift Keying
C/No	Carrier to Noise Density Ratio
CSK	Code Shift Keying
CW	Continuous Wave
D/A	Digital to Analog
DFT	Discrete Fourier Transform
EAROM	Electrically Alterable Read Only Memory
FH	Frequency Hop
FLL	Frequency Lock Loop
GPS	Global Positioning System
I	Inphase Component of the Signal Waveform
IF	Intermediate Frequency
J/S	Jamming Signal to Desired Signal Power Ratio
JTIDS	Joint Tactical Information Distribution System
LO	Local Oscillator
LSI	Large Scale Integration
MSK	Minimum Shift Keying
MSP	Microsignal Processor
P	Protected Code
PLL	Phase Lock Loop
PN	Pseudo-Noise
PSK	Phase Shift Keying
Q	Quadrature Component of the Signal Waveform
R	Range
\dot{R}	Range Rate
ROM	Read Only Memory
RSED	Reed Solomon Encoder Decoder
SAM	Standard Avionic Module
TDMA	Time Division Multiple Access
TH	Time Hop
TTFF	Time to First Fix
VCO	Voltage Controlled Oscillator

SECTION I INTRODUCTION

This report describes the work performed under AFAL Contract F33615-76-C-1307, Standard Avionics Modules for Existing Modems. The work was performed by Electronic Systems Division of the TRW Defense System and Space Group during the period from July 1976 to December 1977. Section 1.0 of this report outlines the objectives and accomplishments of the project and presents conclusions resulting from the study and recommendations for future work based on this effort. Technical details are presented in subsequent sections.

1.1 BACKGROUND

Recent experience with the rising cost of avionics has prompted DOD to investigate more cost effective methods and approaches of providing aircraft avionics. Not only have the acquisition costs increased, but so have the operational and support costs. The future trend is that unless procurement practices and technical approaches are changed, these costs will continue to escalate. Acquisition costs escalation is mainly caused by general economic inflation and growing complexity of the equipment. Operational and support costs escalation is mainly caused by increased complexity (more difficult to maintain) of equipment and lower skilled personnel. Additionally, modification costs associated with the introduction of a new equipment are comprising a larger share of the life cycle cost. The reason is that today's aircraft are already loaded with so much equipment and space is at such a premium, that introduction of any new equipment creates major cabling and tooling modifications.

Some of the approaches considered by DOD agencies have been aimed at reducing acquisition costs, minimizing modification costs, and providing for equipment growth or modification to accommodate new requirements without having to scrap complete equipment. One approach that has been considered and offered as a partial solution to the proliferation of equipment is that of time sharing of common assemblies in multifunction terminals. In this concept, a multifunction terminal would be a configuration of common and special modules for performing a select number of communication or navigation functions. Depending upon the operational scenario these common modules would be either switched electronically

or manually to accomplish the needed functions. If electronic switching is employed, time sharing of the common processing functions can be accomplished on a micro-time basis, i.e., every few milliseconds, as opposed to a macro-time basis of every few seconds or minutes.

Another approach to more cost-effective avionics is the Standard Avionics Module concept. This is the approach that was adopted for this project. Under this concept, standard modules capable of performing selected processing functions are developed and used repeatedly for different equipment applications. For example, employing this concept, a single IF amplifier which can be set to the appropriate gain and bandwidth could be designed for JTIDS, GPS, and TACAN. The benefits would be one non-recurring engineering cost as opposed to three, and lower production cost because of one large build quantity instead of three small build quantities. Under present procurement practices, little if any benefit is transferred from one project to another, e.g., JTIDS to GPS or vice versa.

1.2 SUMMARY

The work was performed in accordance with the four task items in the Statement of Work. The technical task items were as follows:

Task 1 - Basic System Design: develop a basic conceptual system design to the level sufficient to identify trade-offs, analysis and initial partitioning for standardization.

Task 2 - Functional Partitioning and Form Factor Selection: determine functional partitioning of the subsystem considering modularity, flexible interconnections, and multi-purpose utilization.

Task 3 - Fabrication of Subsystem in SAM Format: fabricate the selected SAM functions to form operating portions of the partial subsystem terminal.

Task 4 - Test, Analysis, Summary and Recommendations: perform functional module tests and analyze the test results. Summarize and document the results of the effort.

During Task 1, a review and analysis was conducted of two specific L-Band spread spectrum terminals - GPS and JTIDS. This included performance characteristics and data or signal processing requirements. To encompass a broad range of applications, a generic PSK waveform using direct sequence PN was also defined. Digital signal processing, using as a

core element programmable digital processors, was selected as the basis for modular multi-function elements within the systems analyzed. Critical trade studies performed include analog-to-digital quantization and dithering, carrier acquisition and tracking loops, and phase tracking loop comparisons. An initial terminal functional partitioning was selected based on factors such as processing requirements, waveform performance and timing, and available technology.

The module partitioning was evaluated during Task 2 as part of a detailed analysis of the terminal block diagrams. Standardization at a function level and packaging constraints were traded with processing performance requirements and capabilities. The standard module boundaries with the necessary iterations were then selected. The one-half ATR card with 144 input/output pins is the digital card type selected as the SAM concept for all modules. The RF modules used a similar form factor. The Navy SHP modules was discarded for the following reasons:

- a) the basic module is physically too small to allow complex signal processing functions. The SHP 2A module is approximately 2" x 4" and about one half the area of a 1/2 ATR card.
- b) module dimensions restrict signal input/output such that digital functions in LSI form could not be accommodated. SHP 2A modules are limited to 80 pins versus 144 pins for the 1/2 ATR card.
- c) SHP modules do not accommodate RF circuits.
- d) SHP thermal design was inferior to the Air Force standard. The SHP is designed for convection cooling versus conduction cooling for the 1/2 ATR card.

The fabrication phase, Task 3, involved only the basic Standard Avionic Modules that offered the highest potential for multi-application utilization. The SAM's developed include the micro-signal-processor (MSP), the modulator (MOD), the 70 MHz IF amplifier (IFA) and the frequency generator (FGN). The MSP performs all post-correlation digital signal processing - acquisition, tracking, demodulation and bit synchronization - using a 25 mega-instruction per second parallel pipeline microprocessor. The MOD accommodates BPSK, QPSK, MSK, FSK and AM with an output at 70 MHz. The IFA incorporates a selectable bandpass filter, amplification (+80 db) and automatic gain control. The FGN provides all the frequencies for the

terminal modules using a programmable voltage controlled oscillator. The MSP was fabricated using one-half ATR "universal pins" digital cards in the stitch-wire configuration. Ten cards were used with the special carousel test fixture. The three RF modules were machined housings in a one-half ATR form factor and standard printed circuit boards. Seven other modules (including two other SAM's) were designed to detailed circuit/logic levels using the card type selected but were not fabricated.

Module functional tests were conducted on all the completed hardware SAM's. Specific parameters of each were verified such as gain, processing throughput, spectral purity and hardware or firmware programmability. No integrated tests, such as the MOD driving the IFA, were done as other modules were necessary for a complete link. An evaluation of the completed SAM's does indicate the viability of the module boundaries, the associated input/output signal selection and the module substitution capability of technology transparency.

The complete module descriptions for the demodulator and modulator for the GPS and generic PSK waveforms are summarized in Table 1. Twelve modules exist - nine modules for the demodulator and three modules for the modulator. Six standard avionic modules can be used interchangeably among the different L-Band terminals. The other modules are specialized functions that cannot be adapted from one waveform to another. The programmable SAM's include the IF amplifier, A to D converter, digital correlator, frequency generator, modulator and the micro-signal-processor. The functional versatility of the SAM's results from selectable bandpass filter modules in the IF amplifier and A to D converter, a counter programmable VCO in the frequency generator, high-speed LSI correlator chip with a digital output in the correlator, and the firmware programmable general-purpose parallel pipeline micro-signal-processor. These modules formed the building blocks such that a terminal, such as GPS, can be organized as a composite of the SAM's and the special-purpose modules.

TABLE 1. SAM/EM SUMMARY TABLE

DEMULATOR		CONVERSION/PROCESSING	FEATURES	NOTES
IF AMPLIFIER	IFA	<ul style="list-style-type: none"> - BANDPASS FILTERING - AMPLIFICATION - AUTOMATIC GAIN CONTROL 	<ul style="list-style-type: none"> - SELECTABLE BANDPASS FILTER (PLUG-IN SUBMODULE) - GAIN TO +90 DB 	<ul style="list-style-type: none"> - STANDARD MODULE - ONE 1/2 ATR CARD EQUIVALENT
QUADRATURE A/D CONVERTER	ADC	<ul style="list-style-type: none"> - DOWNCONVERT I, Q SIGNAL - A/D QUANTIZATION 	<ul style="list-style-type: none"> - SELECTABLE LP FILTER - A/D CONVERTER: 20 MSPS 2 BPS 	<ul style="list-style-type: none"> - STANDARD MODULE - ONE 1/2 ATR CARD EQUIVALENT
DOPPLER WPEOFF	DWO	<ul style="list-style-type: none"> - DOPPLER REMOVAL WITH LOCAL ESTIMATE 	<ul style="list-style-type: none"> - DIGITAL VCO MODULATING ADC 70 MHZ 	<ul style="list-style-type: none"> - ONE ATR CARD EQUIVALENT
DIGITAL CORRELATOR	COR	<ul style="list-style-type: none"> - CODE WPEOFF - CARRIER LOOP - EARLY/LATE CORRELATION - CODE LOOP 	<ul style="list-style-type: none"> - BASIC ELEMENT - 32 BIT LSI CORRELATOR WITH 8 BIT DIGITAL OUTPUT 	<ul style="list-style-type: none"> - STANDARD MODULE - FOUR 1/2 ATR CARDS
CODE GENERATOR (GPS)	GPN	<ul style="list-style-type: none"> - GENERATES RECEIVED CODE REPLICA 	<ul style="list-style-type: none"> - PRESETTABLE IN PARALLEL PN GENERATORS 	<ul style="list-style-type: none"> - MODIFIED GPS CODE GENERATOR - ONE 1/2 ATR CARD
CONTROLLER	CTL	<ul style="list-style-type: none"> - PROVIDES ALL CLOCKS AND CONTROL SIGNALS FOR COR, GPN, AND ADC 	<ul style="list-style-type: none"> - FULL CENTRALIZED SYNCHRONOUS CONTROL 	<ul style="list-style-type: none"> - TWO 1/2 ATR CARDS
FREQUENCY GENERATOR	FGN	<ul style="list-style-type: none"> - GENERATES 70 MHZ (DWO) AND 82 MHZ (CTL) - PLL USED AS SUBMODULES 	PROGRAMMABLE: <ul style="list-style-type: none"> - VCO PLUG-IN FUNCTION - VCO DIVIDER - LOOP FILTER 	<ul style="list-style-type: none"> - STANDARD MODULE - TWO SUBMODULES REQUIRED - TWO 1/2 ATR CARDS

TABLE 1. SAM/EM SUMMARY TABLE (CONTINUED)

DEMODULATOR

FUNCTION	CONVERSION/PROCESSING	FEATURES	NOTES
SPP SPECIAL PURPOSE PROCESSOR	<ul style="list-style-type: none"> - DATA PREACCUMULATION TO REDUCE BANDWIDTH - FORMATS DATA OUTPUT 	<ul style="list-style-type: none"> - BLOCK TRANSFERS TO MSP 	<ul style="list-style-type: none"> - DEDICATED TO GPS AND PSK APPLICATION - FOUR 1/2 ATR CARDS
MSP MICRO SIGNAL PROCESSOR	<ul style="list-style-type: none"> - PERFORMS ALL POST-CORRELATION DIGITAL SIGNAL PROCESSING IN A MICROPROCESSOR - ALGORITHMS INCLUDE ACQUISITION OR PHASE/CODE TRACKING LOOPS, DATA DEMOD, BIT SYNC AND SEQUENCE CONTROLLER 	<ul style="list-style-type: none"> - PSK ALGORITHMS AS LISTED - REALTIME PROCESSING UP TO 38.4 KBPS - FULL PARALLEL ARCH. - MICROPROGRAMMABLE - 5M WDS/SEC DMA - HARDWARE MULTIPLIER - 16-BIT DATA WORDS - AMD 2901 CPU - 400 NSEC MACHINE CYCLE - INSTR EXECUTION RATES: UP TO 20 MIPS 	<ul style="list-style-type: none"> - STANDARD MODULE - EIGHT 1/2 ATR CARDS <p>FOR DIP IC CONFIGURATION AND 4K DATA MEMORY/1/2 K PROGRAM MEMORY</p>

MODULATOR

FUNCTION	CONVERSION/PROCESSING	FEATURES	NOTES
MOD MODULATOR	<ul style="list-style-type: none"> - UPCONVERSION - AMPLIFICATION/FILTERING - PN ⊕ DATA 	<ul style="list-style-type: none"> - ACTIVE MODULATORS - ACCOMMODATES BPSK, QPSK, MSK, FSK, AM 	<ul style="list-style-type: none"> - STANDARD MODULE - ONE 1/2 ATR CARD EQUIVALENT
TPN PN GENERATOR	<ul style="list-style-type: none"> - GENERATES TRANSMIT PN CODE 	<ul style="list-style-type: none"> - GPN VARIATION 	<ul style="list-style-type: none"> - TWO 1/2 ATR CARDS
FGN FREQUENCY GENERATOR	<ul style="list-style-type: none"> - GENERATES 70 MHZ (MOD) AND 20 MHZ (TPN) 	<ul style="list-style-type: none"> - SAME AS DEMOD FGN 	<ul style="list-style-type: none"> - STANDARD MODULE - TWO 1/2 ATR CARD EQUIVALENT

TABLE 1. SAM/EM SUMMARY TABLE (CONTINUED)

SAM TEST SYSTEM

FUNCTION	CONVERSION/PROCESSING	FEATURES	NOTES
MODEM ADAPTER	<ul style="list-style-type: none"> - DATA BUFFER/TRANSLATOR - DATA COMPARATOR (HI-SPD); - MSP LOADER/DUMP - BACKUP OPERATOR PANEL - GENERATES ALL MODE CONTROLS 	<ul style="list-style-type: none"> - INCORPORATES DAIS INTER-FACE - MONITORS MSP PROGRAM EXECUTIONS - MICROCOMPUTER INTERFACE 	<ul style="list-style-type: none"> - WIRE-WRAP CARDS AND CHASSIS - INCLUDES MODEM POWER SUPPLIES AND OSCILLATOR

SAM PRODUCTION

FUNCTION	DESCRIPTION	FEATURES
STANDARD DIGITAL CARD	<p>SIZE: 1/2 ATR 3.69 X 6.25 INCHES</p> <p>I/O PINS: 144 CONTACTS</p> <p>POWER DISSIPATION: 12 WATTS MAX</p> <p>IC DENSITY: 40 TO 50 16-PIN DIP IC'S</p>	<p>DESIGNED FOR MIL-E-5400 ENVIRONMENT</p> <p>STITCH WIRE LAB MODEL CARD; FIXED AND UNIVERSAL PATTERN</p> <p>PARTITIONS DIGITAL FUNCTIONS INTO WELL-DEFINED GROUPS</p>

Each module is characterized by a number of 1/2 ATR cards required as a form factor. The 1/2 ATR card was selected as an optimum compromise between existing equipment retro-fit, RF and digital functional partitioning, and signal input/outputs, power dissipation handling and component densities. This is also summarized in Table 1.

A detailed SAM modem (modulator/demodulator) block diagram is depicted in Figure 1. The upper half is the demodulator starting with the modulated 70 MHz IF frequency input on the left side into the IF amplifier where the signal is filtered and amplified. The signal is then digitized and down converted by the A to D converter. The quantized signals are next processed by the correlator performing a matched filter operation on the PN data. The special-purpose processor translates and buffers the high rate data for the micro-signal-processor input. The micro-signal-processor implements, through firmware, the acquisition, tracking and demodulation algorithms as well as modem mode control functions. The supporting functions include the code generator that provides a PN data reference for auto-correlation in the digital correlators. The doppler wipe-off module is a commandable digital frequency synthesizer functioning as a local oscillator for the down conversion in the A to D converter. The controller provides all the specialized gated clock and timing signals within the modem while the frequency generator is the basic stable frequency source. The modulator provides quadra-phase modulation of the 70 MHz IF with inphase and quadrature digital data inputs. A clock source is provided in the module - the same demodulator frequency generator - and another PN generator for exclusive-original PN data onto the output digital data.

A complete module tabulation of the estimated volume, component counts and power dissipation is given in Table 1a. All of the modem modules together with a 400 Hz power supply can be enclosed by a 1/2 ATR long (19") chassis.

Many signal processing functions, historically done in the analog domain as fixed configuration hardware, are allocated to the micro-signal-processor (MSP). The MSP is maximally utilized when operating on multiple signal processing algorithms simultaneously. The same hardware is time-shared among all algorithms. Therefore a major requirement is high data throughput and the MSP parallel pipeline architecture provides this capability. The MSP parallel pipeline replaces up to five different signal

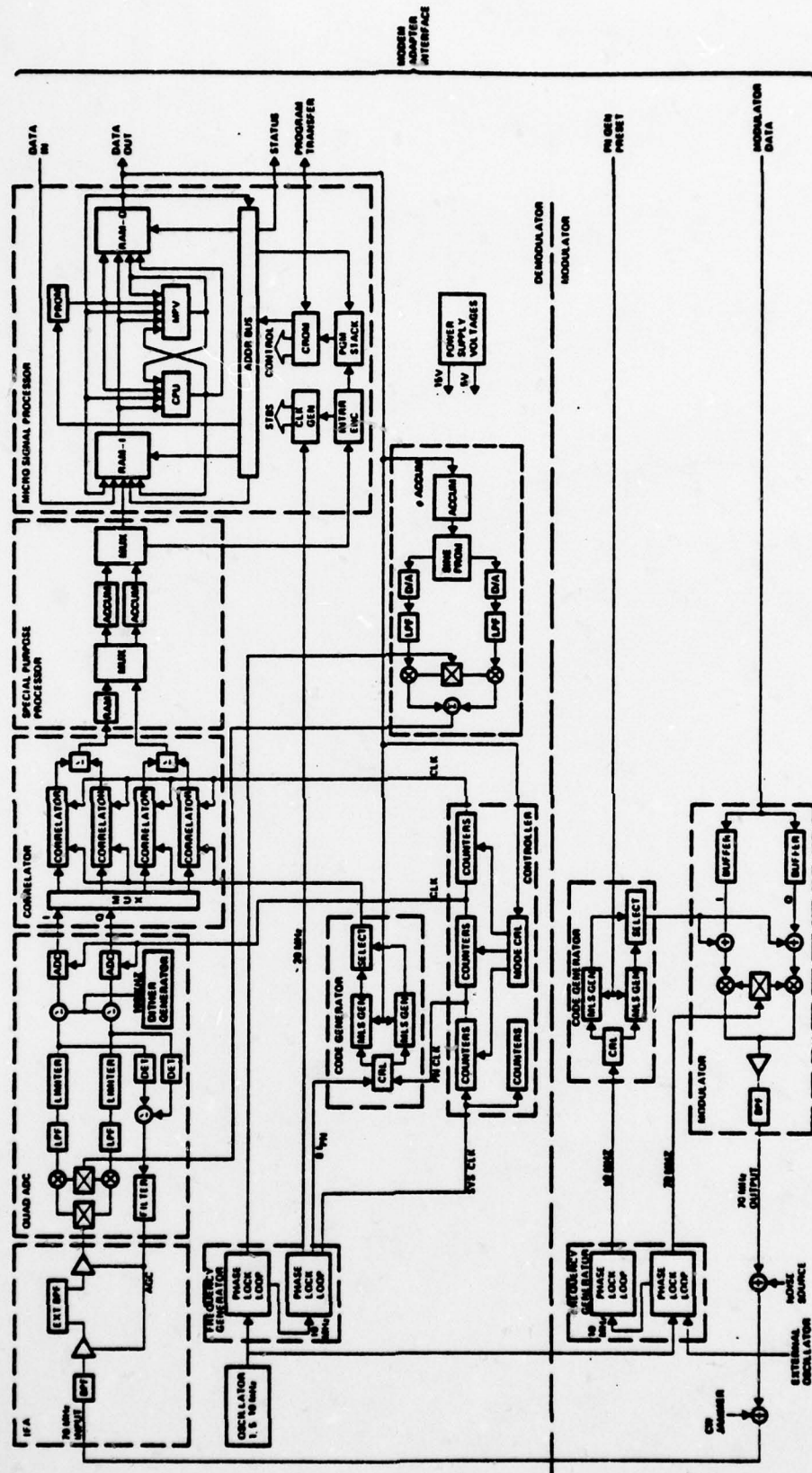


Figure 1. SAM/EM Modem Detailed Block Diagram

TABLE 1A. SAM/EM MODULE SUMMARY

<u>DEMODULATOR</u>	<u>CARDS/RF MODULE</u>	<u>COMPONENT COUNT IC'S/DISCRETES/FUNCTIONS</u>	<u>POWER DISSIPATION (WATTS)</u>
IF AMPLIFIER*	/1	4/ 34	2.4
A TO D CONVERTER*	/1	20/ 64/3	4.5
DOPPLER WIPE-OFF	2/	30/ 71/1	2.6
CORRELATOR*	4/	78/ 80	23.6
CODE GENERATOR	1/	34/ 35	3.7
CONTROLLER	2/	84/ 90	12.2
FREQUENCY GENERATOR*	/2	24/126	4.8
SPECIAL PURPOSE PROCESSOR	4/	140/100	21.1
MICRO SIGNAL-PROCESSOR*	8/	165/120	37.5
	21/4	579/720/3	112.4
MODULATOR			
MODULATOR*	/1	7/ 51/1	1.3
CODE GENERATOR	2/	53/ 50	4.0
FREQUENCY GENERATOR*	/2	24/126	4.8
	2/3	84/227/1	10.1

* STANDARD MODULES

processors and allows adaptive operation such as switching from a frequency lock loop to a phase lock loop during acquisition. Firmware programmability also allows different demodulation algorithms to be evaluated in real time with filter coefficients and configurations being iterated. The MSP algorithms being implemented are summarized in Figure 1b. Initially as an example, data is processed by the selected GPS acquisition algorithm. Upon acquiring, the phase lock and frequency lock loops are activated for coarse and fine carrier tracking. The code tracking loop, an early-late gate configuration, provides the phase error signals to the digital correlators. The bit sync generates the clock signals for the in-phase/quad-phase data or, in the GPS case, the Manchester data is decoded. All the algorithms are summarized in Table 1b with an indication of use with GPS or the generic PSK waveforms.

About 200 MSP firmware instructions were required for the algorithms, the executive and input/output routines. 256 instructions was the given capacity. There was significant processing margin based on an analysis of available processing time versus instruction/operation executions. GPS required about 40 microseconds versus 125 microseconds limit. The generic PSK used about 17 microseconds of 26 microseconds allowed.

1.3 CONCLUSIONS

Based on the results of the work performed, the feasibility and cost effectiveness of applying the SAM concept to communication/navigation ECCM modems was demonstrated. The fundamental SAM architecture was chosen to be compatible with a general class of waveforms; as such it was not tailored to any specific waveform structure or parameter. The generic PSK (rates up to 38.4 K bps), GPS and JTIDS waveforms were considered representative of the general class of spread-spectrum waveforms, either of the direct sequence or frequency hopped/PN type, that will be deployed during the next decade.

The SAM concept is based on functional modules that are a common thread throughout the selected terminals. The common modules would tend to lower design and development costs as well as total life cycle costs. Required spaces would be reduced. These modules are segmented into the

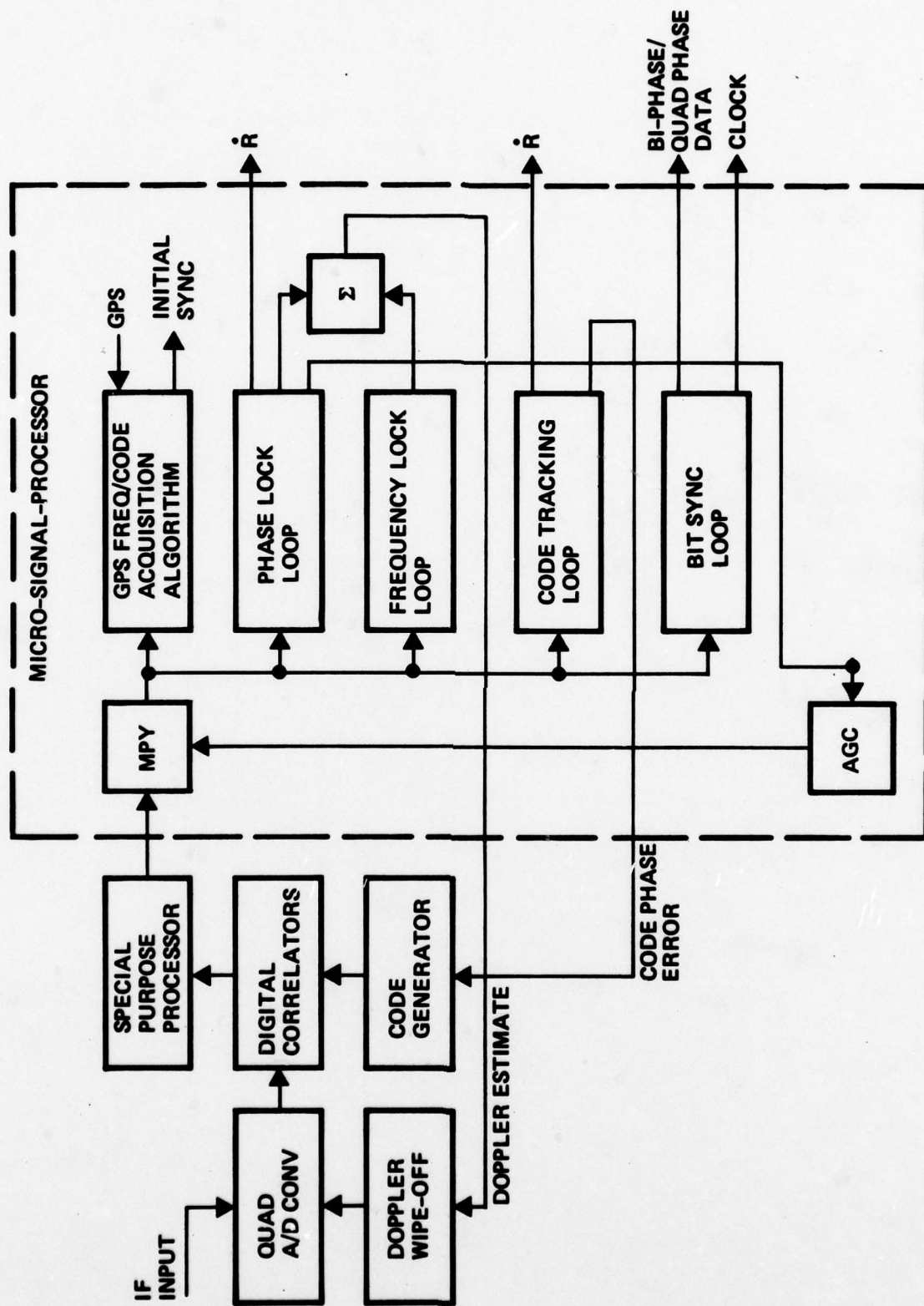


Figure 1B. MSP Signal Processing Algorithms Interrelationship

TABLE 1B. MSP ALGORITHM SUMMARY TABLE

<u>ALGORITHM</u>	<u>PARAMETERS</u>	<u>APPLICATION</u>
FREQUENCY/CODE ACQUISITION	PARALLEL TESTING 16 TIME HYPOTHESES 4 FREQUENCY HYPOTHESIS DFT (4 POINT) IMPLEMENTATION 3 OF 4 DETECTOR	GPS
FREQUENCY LOCK LOOP	SECOND ORDER LOOP DFT (4 POINT) IMPLEMENTATION FREQUENCY RANGE ± 19.7 KHZ	GPS
PHASE LOCK LOOP	THIRD ORDER LOOP BIPHASE FEEDBACK LOOP ALGORITHM	GPS, GENERIC PSK
CODE TRACKING LOOP	EARLY-LATE GATE LOOP SECOND ORDER LOOP TIME RESOLUTION - $1/8$ CHIP	GPS, GENERIC PSK
MANCHESTER/BIT SYNC	NONCOHERENT TRANSITION DETECTOR	GPS
BIT SYNC LOOP	DATA TRANSITION TRACKING LOOP SECOND ORDER LOOP BIPHASE OR QUAD-PHASE DATA	GPS, GENERIC PSK
AGC	SIMPLE INTEGRATOR MODULATES INPUT TO A FIXED LEVEL	GPS, GENERIC PSK

standard avionic modules (SAM's) and specialized modules. Terminal partitioning was based on major functions such as amplifiers, PN generators, correlators, modulators and microprocessors. Specialized modules are dedicated and unique to the particular waveform.

The SAM concept offers flexibility as a result of the higher level partitioning. Generic functions can now be substituted by different technologies that are within the form factor and packaging requirements. This allows technology improvements to be easily accommodated - technology transparency. Also module second sourcing is facilitated.

Terminal module adaptability is achieved by the use of multiple plug-in submodules as in bandpass filters and VCO's, and firmware programmability. The latter is imbedded in the microprocessor used for signal processing - the micro-signal-processor. The firmware allows different algorithms to be chained together in adaptive modes and allows real-time filter coefficient evaluation. Algorithm substitution is simply done by control memory (read-only memories) replacements.

Two major system considerations were instrumental in meeting the project objectives. The first is the use of a digital signal processing architecture and the second is the application of the one-half ATR card packaging approach.

The digital signal processing approach has the advantages of being more stable and reliable than analog techniques, thus eliminating adjustments and precision components, and hardware compression techniques can easily be applied. The latter applies both to the use of large scale integration (LSI) and high-performance microprocessors/microcomputers. Digital logic is more amendable to LSI with much research and technology investigation being conducted to improve densities, yields, and speeds while lowering power dissipation. The LSI production learning curve falls rapidly thus making LSI attractive cost-wise.

The high-performance microprocessor using a general purpose parallel pipelined architecture is quite capable of processing multiple algorithms on an interleaved time-shared basis. A single function can now replace up to five separate signal processors. The selected micro-signal-processor

(MSP) is a core element in the SAM concept permitting hardware reduction, LSI applicability and programmability combined in a simple module.

The other major system consideration is the selection of the one-half ATR card approach. A review of the existing and proposed packaging standards indicated that the ATR approach and the one-half ATR size specifically had the advantage of:

- allowing greater component densities even in low cost dual-in-line (DIP) integrated circuits. This in turn facilitated the definition of optimum module boundaries. For example, the modulator is a single one-half ATR card and the micro-signal-processor consists of 8 cards divided into memory, central processor, controller, address generators, input/output and multipliers.
- higher signal input/output pins necessary for digital parallel data paths where data is transferred bit-parallel (e.g., 16 bits per word). Historical data indicates that up to 144 pins are required for digital implementations.
- higher power dissipation capabilities of up to 15 watts per card. This permits a broad range of digital bipolar and RF technologies applications. A variety of technologies can be used consistent with technology transparency.

The composite effect of the digital signal processing and the one half ATR packaging produced a realizable SAM concept.

Although the major program objectives were met, further work is recommended in the following areas:

- the basic structure should be extended to a more general class of terminals such as the inclusion of narrow band systems such as HF, VHF and UHF.
- application of digital signal processing to a multi-purpose terminal where two or more waveforms are simultaneously processed. This constitutes an interleaved time-shared configuration taking advantage of the duty cycle of selected waveforms. When one is inactive, probabilistically, the other waveform can be accommodated.
- completion of the SAM modules, both hardware and verification and validation of the algorithm firmware. An end-to-end modem test and evaluation, combined with real-time microprocessor throughput performance tests, would completely determine the feasibility of the SAM concept.

SECTION II

GENERAL SYSTEM DESCRIPTION

2.1 Waveform Descriptions

In configuring the SAM terminal, two specific waveform types and a third generic class of waveforms were considered for the terminal demonstration. These are the Navstar GPS waveform, the JTIDS waveform and a generic class of bi-phase and quad-phase PSK waveforms. Each of these are spread-spectrum waveforms either of the direct-sequence type or the frequency hop/PN type. In order to understand the terminal processing, it is important to understand the waveform structures. Accordingly, a brief description of each waveform is presented in the following sections. Since the GPS and JTIDS programs are in a development phase, the waveform parameters are subject to change. Similar comments apply to performance requirements.

2.1.1 Navstar GPS

The GPS is designed to provide worldwide three-dimensional navigation to users based upon signal time-of-arrival measurements from transmitters of known location. There are two GPS waveforms, the Clear (C/A) signal and the Protected (P) signal. The C/A signal is designed for ease of acquisition and can be used for reduced precision navigation by low complexity users. The signal is a direct-sequence bi-phase PN waveform having a chip rate of 1.023 Mchips/sec. The C/A code is 1023 chips long so the code epoch rate is 1000 Hz. The data carried by the C/A code is identical to the data carried by the P code and is at a rate of 50 bits per second.

The P code is designed to provide high precision navigation and improved antijam protection. Like the C/A code, the waveform is direct sequence bi-phase PN at a chip rate of 10.23 Mchips/sec. The P code is essentially nonrepetitive, being at least 7 days long when not controlled by the TRANSEC device. Acquisition is available only to those users who possess the means to reduce the code state uncertainty to a reasonable interval. The data rate is 50 bits/sec as in the C/A signal. Table 1 summarizes these characteristics. Figure 1c shows the timing relationships between the C/A code epoch and the data.

TABLE 2. GPS WAVEFORM PARAMETERS

<u>C/A SIGNAL</u>	
WAVEFORM CLASS	DIRECT SEQUENCE BI-PHASE PN
CHIP RATE	1.023 MCHIPS/SEC
CODE EPOCH RATE	1000 Hz
DATA RATE	50 BPS
<u>P SIGNAL</u>	
WAVEFORM CLASS	DIRECT SEQUENCE BI-PHASE PN
CHIP RATE	10.23 MCHIPS/SEC
CODE EPOCH RATE	ESSENTIALLY NON-REPETITIVE
DATA RATE	50 BPS

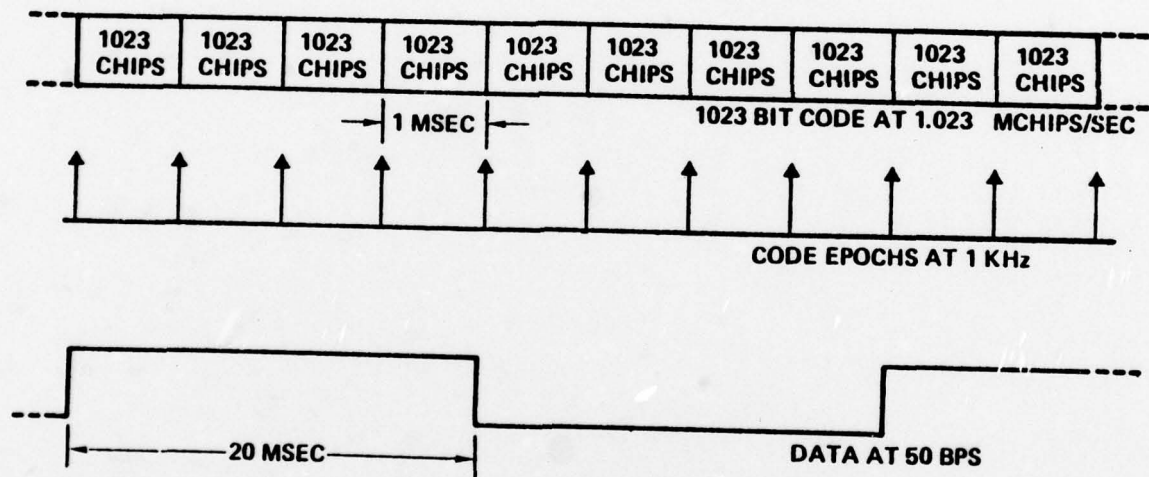


Figure 1c. C/A Signal Timing

2.1.2 Generic PSK Waveforms

In order to demonstrate the validity of the standard module concept, the terminal design was configured to accommodate a family of PSK waveforms of the direct sequence bi-phase or quad-phase PN type. The waveform varies in chip rate from 76.8 Kchip/sec up to 9.8304 Mchips/sec. The data rate varies from 75 bits/sec up to 38.4 Kbits/sec and takes the form of bi-phase or quad-phase data modulation. The PN code to be used with this family of waveforms is assumed to be non-repetitive. Table 3 summarizes these features.

TABLE 3. GENERIC PSK WAVEFORMS

WAVEFORM CLASS	-----	DIRECT SEQUENCE BI-PHASE/QUAD-PHASE PN
CHIP RATE	-----	76.8 KCHIPS&SEC —→ 9.8304 MCHIPS/SEC
CODE EPOCH RATE	-----	ESSENTIALLY NON-REPETITIVE
DATA RATE	-----	75 BPS —→ 38.4 KBPS
DATA MODULATION	-----	BI-PHASE/QUAD PHASE

Table 4 shows the various combinations of PN rate and data rate which will be within the capabilities of the terminal. The first eight columns and first ten rows correspond to the generic class of PSK waveforms. The table entries show the ratio of PN rate to data rate. For example, for a PN rate of 76.8 Kchips/sec at a data rate of 75 bits/sec, there are 16 x 64 PN chips/bit. The ratio are broken down to multiples of 16 because the data correlation is to be performed in a 32-bit digital correlator with the data being sampled at twice the PN rate. Therefore in this example, 64 correlations must be combined to form a data bit.

The ninth and tenth columns and last row correspond to the GPS C/A and P signal cases, respectively. Note that the PN rate to data rate ratio is not an exact multiple of 16. Therefore, in combining correlator outputs to form data bits, one of the correlations is adjusted to accommodate this.

TABLE 4. PN/DATA RATE COMBINATIONS

PN RATE DATA RATE	76.8K	153.6K	307.2K	614.4K	1.2288M	2.4576M	4.9152M	9.8304M	1.023M	10.23M	0
75 BPS	16 x 64	16 x 128	16 x 256	16 x 512	16 x 1024	16 x 2048	16 x 4096	16 x 8192	-	-	32 x 1/32 (2400)
150 BPS	16 x 32	16 x 64	16 x 128	16 x 256	16 x 512	16 x 1024	16 x 2048	16 x 4096	-	-	32 x 1/32 (4800)
300 BPS	16 x 16	16 x 32	16 x 64	16 x 128	16 x 256	16 x 512	16 x 1024	16 x 2048	-	-	32 x 1/32 (9600)
600 BPS	16 x 8	16 x 16	16 x 32	16 x 64	16 x 128	16 x 256	16 x 512	16 x 1024	-	-	32 x 1/32 (19200)
1200 BPS	16 x 4	16 x 8	16 x 16	16 x 32	16 x 64	16 x 128	16 x 256	16 x 512	-	-	32 x 1/32 (38400)
2400 BPS	16 x 2	16 x 4	16 x 8	16 x 16	16 x 32	16 x 64	16 x 128	16 x 256	-	-	32 x 1/32 (76800)
4800 BPS	16 x 1	16 x 2	16 x 4	16 x 8	16 x 16	16 x 32	16 x 64	16 x 128	-	-	32 x 1/32 (153600)
9600 BPS	-	16 x 1	16 x 2	16 x 4	16 x 8	16 x 16	16 x 32	16 x 64	-	-	32 x 1/32 (307200)
19200 BPS	-	-	16 x 1	16 x 2	16 x 4	16 x 8	16 x 16	16 x 32	-	-	32 x 1/32 (614400)
38400 BPS	-	-	-	16 x 1	16 x 2	16 x 4	16 x 8	16 x 16	-	-	32 x 1/32 (1228800)
50 BPS	-	-	-	-	-	-	-	-	20 x 32 x 31 31/32	200 x 32 x 31 31/32	

The last column indicates the situation for conventional data which is not PN coded. The table entries show that the data is over-sampled (32 samples per bit) which allows use of the correlators as matched filters. The entries in parentheses show the required sample rate.

2.1.3 JTIDS Waveform

The JTIDS waveform is another example of a spread-spectrum waveform which could be processed in the SAM modules. It is a time hopped, frequency hopped, direct sequence PN waveform. The PN rate is 5 Mchip/sec and the modulation is minimal-shift-keying (MSK). This is somewhat different from PSK and its processing requires a different configuration of the input circuit to the correlators. The data modulation is 32-ary cyclic code shift keying. That is, data is encoded in 5 bit words into cyclic shifts of a fixed 32 bit code. Error correction encoding is a (31,15) Reed-Solomon code. These characteristics are summarized in Table 5.

Figure 2 shows the two types of JTID waveforms. Both are based on a 26 μ sec "event." In the 2B waveform, each event consists of one PN burst of 32 chips and duration 6.4 μ sec followed by 19.6 μ sec of deadtime. In the 3B waveform, each event consists of two identical (except for PN code) PN bursts of 32 chips each followed by 6.6 μ sec of deadtime. The deadtime in both cases is utilized to perform the M-ary decoding of the previous pulse. It is also used for hopping the frequency synthesizer.

2.2 Signal Processing Functions/Requirements

The following summarizes the processing capabilities required of the terminal for each of the waveform classes. In addition, performance requirements are given for the GPS and generic class of waveforms.

2.2.1 GPS Processing Functions

The GPS functions are those related to frequency and code acquisition and tracking, and data demodulation. In the normal mode, the receiver must search a range uncertainty equal to 1023 chips and a frequency uncertainty as great as 3.6 kHz (4.5 σ). Both frequency and code are acquired to coarse resolution first. Following initial acquisition, the frequency, phase and code tracking loops are activated to reduce the errors to an acceptable level and provide tracking of signal dynamics. The frequency locked loop is used to provide fast frequency acquisition while the phase-locked loop

TABLE 5. JTIDS WAVEFORM PARAMETERS

WAVEFORM CLASS	TH/FH/PN
NETWORK ORGANIZATION	TDMA
EVENT DURATION	26 μ SEC
PULSE DURATION	6.4 μ SEC
PN RATE	5 MHz
PN MODULATION	MSK
DATA MODULATION	32-ARY CSK
CODING	(31, 15) REED-SOLOMON

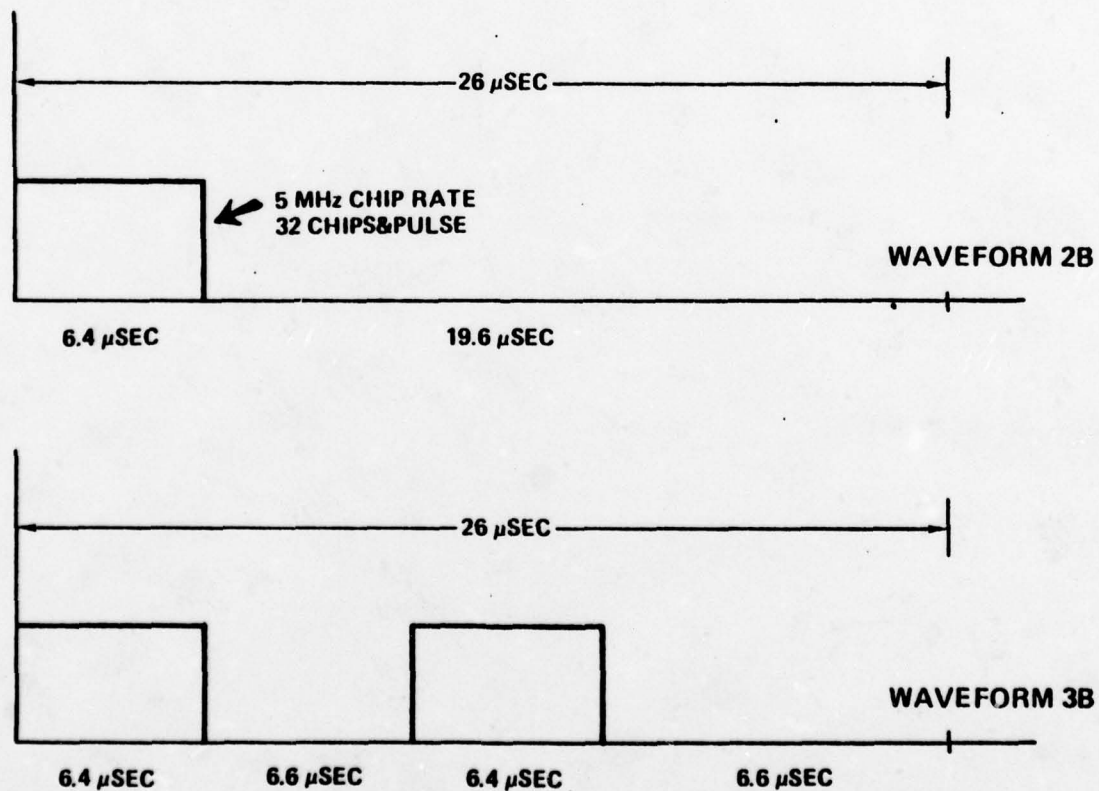


Figure 2. JTIDS Waveform 2B/3B

provides improved tracking once the signal frequency is within the loop bandwidth.

For direct mode acquisition of the P code, a frequency uncertainty of up to 800 Hz and a range uncertainty equivalent to 1500 PN chips must be searched. As in the normal mode case, the initial acquisition results in a coarse estimate of code phase and frequency. The frequency locked loop, phase-locked loop and delay lock loop refine the initial estimate.

Data demodulation for both the C/A and P code is coherent bi-phase PSK. The phase-locked loop provides the coherent reference for the demodulator. Table 6 summarizes the processing functions to be performed by the terminal on the GPS waveform.

TABLE 6. GPS PROCESSING FUNCTIONS

NORMAL MODE ACQUISITION (C/A CODE)

- SEARCH R AND \dot{R} UNCERTAINTY
- FREQUENCY LOCK LOOP ACQUIRE/TRACK
- PHASE LOCK LOOP ACQUIRE/TRACK
- DELAY LOCK LOOP ACQUIRE/TRACK
- BIT SYNC ACQUIRE

DIRECT MODE ACQUISITION (P CODE)

- SEARCH R AND \dot{R} UNCERTAINTY
- FREQUENCY LOCK LOOP ACQUIRE/TRACK
- PHASE LOCK LOOP ACQUIRE/TRACK
- DELAY LOCK LOOP ACQUIRE/TRACK

DATA DEMODULATION (C/A AND P CODE)

- COHERENT BI-PHASE PSK

2.2.2 GPS Performance Requirements

Tables 7, 8, and 9 contain some of the key GPS requirements as they relate to signal processing capability. The acquisition requirements are given in terms of a time-to-first-fix and probability of acquisition. The position uncertainties and frequency uncertainties determine the search ranges for the acquisition algorithms. The significance of the code doppler rate is that it sets an upper limit to the integration time for acquisition. If the integration time is such that code doppler causes the signal PN code to shift relative to the local code by more than $1/2$ a chip, then decorrelation (loss in output signal to noise ratio) could occur.

The range and range rate accuracy requirements have bearing on the code tracking resolution of the receiver and the doppler measurement criterion. The minimum range error requirement corresponds to a code tracking accuracy of $1/12$ of a PN chip (1σ). This implies that the receiver timing must have resolution of at least $3/10$ of a chip. The actual receiver timing resolution must be better than this since the effects of noise must also be taken into account.

2.2.3 Generic PSK Waveform Processing Functions

For the generic family of waveforms, no frequency or code acquisition capability is planned since acquisition requirements are normally specific for each application. Instead, it will be assumed that code and frequency estimates are available and that the receiver must provide phase and code tracking of signal dynamics in addition to bi-phase or quad-phase data demodulation (see Table 10).

2.2.4 Generic PSK Waveform Processing Requirements

The processing requirements for the generic PSK waveforms are given in Table 11. They influence the terminal design in various ways. The requirement to track doppler rate necessitates the use of a third-order phase-locked loop, or equivalent. The extended frequency track range sets requirements on the tracking loop tunable oscillator. In a digital receiver, the frequency resolution requirement is met by providing sufficient tuning resolution in the digital VCO. The code timing resolution corresponds to $1/4$ chip at the highest chip rate and is accommodated by using an internal clock rate which is eight times the PN rate.

TABLE 7. GPS ACQUISITION REQUIREMENTS

	NORMAL MODE ACQ		DIRECT MODE ACQ	
	< 24	< 19	< 34	< 27
J/S RATIO (dB)				
TTFF (SEC)	360	240	720	300
PROBABILITY OF SUCCESS (%)	90	90	90	90
POSITION UNCERTAINTY (KM)	175	175	9.26	9.26
1σ (CHIPS)	597	597	316	316
VELOCITY UNCERTAINTY (M/SEC)	150	150	30	30
1σ (Hz)	788	788	158	158
MAXIMUM VEHICLE ACCEL (M/SEC ²)	10	10	10	10
(Hz/SEC)	53	53	53	53
MAXIMUM VEHICLE JERK (M/SEC ³)	50	50	50	50
(Hz/SEC ²)	263	263	263	263
TOTAL FREQUENCY UNCERTAINTY (Hz)	811	811	158	158
1σ				
CODE RATE (CHIPS/SEC)	0.5	0.5	1.6	1.6
1σ				

TABLE 8. GPS DEMODULATION REQUIREMENTS

	P CODE		C/A CODE	
	MIN	ULT	MIN	ULT
CARRIER TRACK	40	43	30	33
CODE TRACK (HOLD-ON)	42	49	32	39
BIT ERROR RATE (10^{-5})	42	47	32	39

J/S MARGINS (dB)

TABLE 9. GPS PSEUDO RANGE/RANGE RATE
MEASUREMENT ACCURACY

ERROR (1σ LEVEL)	P CODE		C/A CODE	
	MIN	ULT	MIN	ULT
RANGE (METERS)	5	1.5	25	15
(NSEC)	16.7	5.0	83.3	50
RANGE RATE (M/SEC)	0.02	0.006	0.02	0.006
(Hz)	0.1	0.03	0.1	0.03
J/S (dB)	40	50	30	40
C/N ₀ (dB-Hz)	34.5	34.5	34.5	34.5

TABLE 10. GENERIC PSK WAVEFORM PROCESSING FUNCTIONS

- PHASE LOCK LOOP ACQUIRE/TRACK
- DELAY LOCK LOOP ACQUIRE/TRACK
- BI-PHASE/QUAD-PHASE DATA DEMODULATION

TABLE 11. GENERIC PSK WAVEFORM PROCESSING REQUIREMENTS

PARAMETER	REQUIREMENT
DOPPLER RATE	100 Hz/SEC MAXIMUM
DOPPLER ACCELERATION	50 Hz/SEC ² MAXIMUM
FREQUENCY TRACK RANGE	± 15 KHz MAXIMUM
FREQUENCY RESOLUTION	1.0 Hz
CODE DOPPLER RATE	3 PARTS IN 10 ⁶
CODE OFFSET RANGE	2 PARTS IN 10 ⁵
CODE TIMING RESOLUTION	25 NSEC

2.2.5 JTIDS Waveform Processing Functions

Although it was not intended that the terminal demonstrate the processing of JTIDS waveforms, the modules were designed such that they could be configured with that capability (see Table 12).

The JTIDS receiver functions include the capability for detecting a multiple pulse preamble. This is provided for by utilizing a sufficient number of correlator modules and a JTIDS preprocessor circuit for post-detection processing. 32-ary CSK demodulation is readily accommodated in the correlator module design by providing for reference code recirculation. Error correction decoding would require a dedicated SAM microprocessor programmed to perform the (31,15) Reed-Solomon decoding algorithm.

For treatment, the ability to generate a 32-ary CSK signal with MSK PN modulation is required and is provided for in the design of the programmable modulator.

2.3 General Common Module System Architecture

The following describes the SAM terminal in functional terms and indicates how the waveform processing requirements addressed in the previous section influence the design of the various modules.

The architecture of the SAM terminal is designed for flexibility in accommodating a variety of waveform processing requirements. As such, a key feature is the degree to which digital processing is utilized. Digital processing offers the distinct advantage of being reprogrammable to handle different waveform formats and data rates through changes in the timing and control function. A second feature is the use of a high speed micro-signal processor (MSP) to perform many of the signal processing algorithms. The MSP offers the advantage of versatility and ease of modification, being software controlled. It can also assume some of the timing and control functions for the terminal. A third feature of the SAM terminal is the architecture itself and the module partitioning. The architecture was chosen to be compatible with a general class of waveforms. The interface is at a standard 70 MHz IF with a quadrature downconversion to baseband. The architecture is not tailored to any particular waveform structure or parameter. The partitioning of the terminal into modules was based on a functional rather than a physical basis. That is, the modules defined here

TABLE 12. JTIDS WAVEFORM PROCESSING FUNCTIONS

RECEIVE

- MULTIPLE PULSE FREQUENCY HOP PREAMBLE DETECTION
- 32-ARY CSK DEMODULATION
- DELAY LOCK LOOP CODE TRACKING
- ERROR CORRECTION DECODING

TRANSMIT

- MESSAGE ENCODING
- 32-ARY CSK MODULATION
- MSK PN MODULATION

each encompasses a complete signal processing function and are capable of use in a variety of situations. The partitioning involved a tradeoff between smaller functions, which allow greater flexibility but require more design time to apply, and larger functions, which minimize design time but are less flexible. The partitioning shown here is felt to be a good compromise.

2.3.1 SAM Terminal Description

Figure 3 is a diagram of the SAM terminal partitioned into modules. A generic configuration is shown. The actual complement of modules required varies with the application.

The transmitted signal is generated at a 70 MHz IF frequency at low level (0 dBm) in the Modulator module based on data received from the Micro-Signal Processor. The received 70 MHz signal is first processed in the IF amplifier which provides gain, gain control and bandlimiting of the signal. The signal is mixed down to in-phase and quadrature baseband components in the Quad ADC module. The downconversion L.O. is a tunable digital frequency synthesizer which allows frequency pretuning and/or frequency and phase tracking. It is controlled by the MSP which generates tune control signals based upon software tracking algorithms. The quadrature signals are sampled and quantized to two bits each in the Quad ADC module.

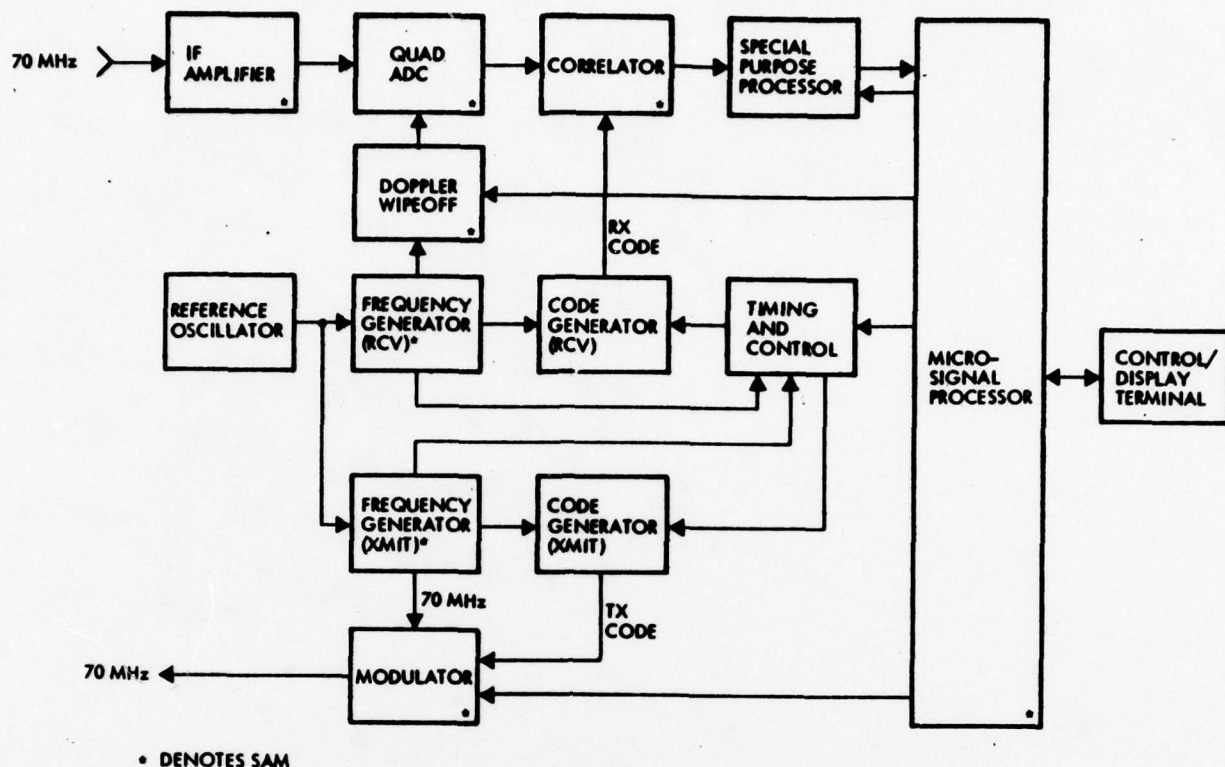


Figure 3. SAM Modem Functional Block Diagram

The quantized signals are then processed in the Correlator module, which operates as a matched filter. The number of Correlator modules required depends on the specific application. Switching is provided which allows the modules to be configured to fit the application. The modules utilize an LSI digital correlator chip which is 32 bits long and has a digital output. The correlators can be cascaded to form longer correlators.

The Special Purpose Processor module provides the interface between the Correlator and MSP. Its function is to correct the output data from the Correlator module into a form suitable for the MSP. This may involve processes such as accumulation, threshold detection and comparison, etc. In general, the Special Purpose Processor reduces the data rate to a point where it can be efficiently handled by the MSP. It is not a SAM module and may be different for each application.

The MSP is the core of the SAM terminal. By performing many of the signal processing functions in firmware, a standard hardware design can be programmed for a variety of tasks that conventionally would require special purpose hardware. Although it is true that the firmware is different for each application, the microprocessor still retains most of the advantageous features of a standard module.

Functionally, the MSP mechanizes the acquisition, tracking and demodulation algorithms and performs some of the control functions for the terminal. It also provides the interface with the control and display functions.

2.3.2 Signal Processing Flows

The following describes how different waveforms are processed in the SAM terminal and what functions each of the modules performs. Three cases are considered, GPS, generic PSK, and JTIDS. Although it is not intended that JTIDS processing be demonstrated in the SAM terminal, the description will show how the modules can be adapted to such a function.

2.3.2.1 GPS Receiver Processing

The RF signal is first processed in the IF amplifier where it is filtered and gain controlled. The filter bandwidth is selected to be 1 MHz (for the C/A signal) or 10 MHz (for the P signal).

The 70 MHz IF signal is downconverted and quantized in A/D converter. Two-bit quantization is used and the sampling rate is 20.46 MHz (twice the chip rate) for the P signal and 2.046 MHz for the C/A signal.

The digitized quadrature components of the GPS signal are correlated against the reference PN code (generated in the PN code generator) in the digital correlator. Although the digital correlator device is a parallel correlator, it is used in a serial mode for GPS. That is, the correlators are used to compute partial correlation sums with higher level accumulation being performed in the microprocessor. The correlators are time shared to perform the punctual, early, and late correlations for code tracking. The PN code is shifted directly into the reference register of the correlator although at a slightly higher rate than the signal samples to accomplish the time sharing operation.

The correlator outputs are processed in the GPS special purpose processor which performs higher level accumulation of the correlator outputs.

The processed GPS signal is then transferred to the MSP. Table 13 lists the receive and control processing functions performed in the MSP. They include acquisition control, frequency tracking, data demodulation, code tracking, and parity check decoding.

TABLE 13. MICROPROCESSOR FUNCTIONS FOR GPS

●	Receive processing functions
	C/A and P code acquisition algorithm
	Frequency tracking
	Phase tracking
	Code tracking
	Bit synchronization
	Data demodulation (PSK)
	Range determination
	Range rate determination
●	Control functions
	Code generator initialization and control
	Mode control
	Module programmable element control
	Terminal display

2.3.2.2 Generic PSK Processing

The generic PSK modulated waveforms are generated in the Modulator module using data supplied through the MSP. Depending upon the selected data rate and PN rate, the Modulator generates a continuous 70 MHz bi-phase or quad-phase modulated signal.

The 70 MHz signal is amplified, filtered and gain controlled in the IF amplifier. It is then downconverted to in-phase and quadrature baseband components and quantized to two bits per channel in the quadrature A/D converter. The signal is sampled at twice the PN rate to keep the time offset loss at an acceptable level. Also, any a priori known frequency offset in the signal can be removed by pretuning the Doppler Wipeoff module. Unknown frequency offsets are removed by the frequency locked loop or phase-locked loop mechanized in the MSP.

The quantized signals are next processed in the Correlator module. As in the GPS case, the correlators are used in a serial correlation mode for

data demodulation, providing partial integration results to the Special Purpose Processor for further integration. The correlators are also time-shared to generate the early/late correlation magnitudes for code tracking. This is accomplished by sliding the incoming signal samples past a fixed reference code in 1/2 chip steps. The correlator output is then sampled not only at the estimated time of coincidence, but also at 1/2 chip earlier and 1/2 chip later.

The partial correlation results are processed further in the Special Purpose Processor, which combines these results into an integration over a full bit interval. The level of integration required depends upon the ratio between PN rate and data rate (see Table 4).

Data from the Special Purpose Processor is then transferred to the MSP. Table 14 lists the functions performed by the MSP. Note that signal tracking functions are provided, but no acquisition function is indicated. This is because it was felt that the acquisition parameters would be unique to each application, making it difficult to arrive at a generic scenario. In addition, the ability of the SAM terminal to perform an acquisition function will be demonstrated for GPS.

TABLE 14. MICROPROCESSOR FUNCTIONS FOR GENERIC PSK

- Transmit processing functions
 - Data generation
- Receiver processing functions
 - Phase tracking
 - Code tracking
 - Data demodulation
- Control functions
 - Code generator initialization and control
 - Mode control
 - Module programmable element control
 - Terminal display

2.3.2.3 JTIDS Processing

The following description is included to illustrate the use of the SAM modules in processing the JTIDS signal. The 70 MHz IF signal, which has already been dehopped, is amplified, filtered and gain controlled in the IF amplifier. It is then downconverted to in-phase and quadrature baseband channels and quantized to two bits per channel in the A/D Converter module. In this case, the sampling rate is equal to the PN rate rather than twice the PN rate because the JTIDS MSK modulation has a correlation function which is wider than for PSK modulation. Therefore, the spacing between samples can be greater with minimal effect on the time offset loss.

The quantized JTIDS signals drive the Correlator module. For preamble acquisition, the PN codes are loaded directly into the reference register of the correlators, which then perform as passive matched filters. For data demodulation, the cyclic code shift keyed (CCSK) pattern is loaded into the correlator reference register. The PN code is stripped off the incoming signal prior to loading the signal into the correlator. Once the full signal pulse is loaded into the correlator (32 samples), the reference pattern is recirculated and all 32 possible shifts of the cyclic code are correlated against the signal. This is the demodulation process for CCSK. One correlator is provided for each channel for preamble acquisition. Three correlator modules are required for the data channel. They are necessary for the early/late gate code tracking function. One correlator is used as the punctual correlator. That is, its associated PN code timing is matched to the estimated timing of the received signal. The other two correlators use PN code references which are shifted one chip earlier and one chip later than the punctual code and yield estimates of the degree of signal correlation with the early and late PN codes. The three correlators in the data channel are obtained by switching two of the correlators from the acquisition channels to the data channel.

To complete the JTIDS processing a JTIDS Special Purpose Processor is necessary to integrate the terminal hardware efficiently with the micro-processor firmware. The 32-ary CCSK demodulation would be completed in the preprocessor. The 32 correlator outputs for each signal pulse are processed by the preprocessor and the envelope value is computed and the largest output is identified. In addition the early and late correlator outputs

corresponding to the largest practical output are retained. The largest output is compared to a threshold for erasure detection. For preamble acquisition, the Special Purpose Processor compares each of the correlator outputs to a predetermined threshold. Initial acquisition is declared if an M out of N criterion is satisfied (for example, two or more threshold crossings out of four). The latter criterion is implemented as a ROM lookup table.

The JTIDS receive processing is completed in the micro-signal-processor (MSP). The MSP implements the JTIDS transmit/receive and control functions is listed in Table 15. Included are tracking, acquisition and decoding functions.

Data transfers from the special purpose processor would be through the use of a parallel 16 bits/time slot TDM bus. This centrally controlled demand assigned bus provides a multiprocessor access capability with all the channels. It facilitates high rate digital input/output data handling using a common interconnection at 5M words/sec.

Two MSPs are required, one is dedicated to performing the (31,15) Reed-Solomon encoding/decoding (RSED) function while the other MSP is shared among the other tasks.

TABLE 15. MICRO-SIGNAL-PROCESSOR FUNCTIONS FOR JTIDS

- Receive processing function
 - Network entry and sync acquisition
 - Deinterleaving
 - Reed-Solomon (31,15) decoding
 - Parity check decoding
 - Message header decoding
 - PN code tracking (early/late gate tracking)
 - Network time synchronization
 - Message time of arrival computation
- Transmit processing functions
 - Parity check encoding
 - Reed-Solomon (31,15) encoding
 - Interleaving
 - 32-ary CCSK modulation

TABLE 15. MICRO-SIGNAL-PROCESSOR FUNCTIONS FOR JTIDS (Continued)

- Control functions

- Code/clock generator initialization with time-of-day estimate
- Code generator preset
- Realtime/terminal time clock correction
- Threshold setting
- Module programmable element control
- Transmit/receive control
- Mode control (1,2,3 and 4)
- Terminal display

2.3.2.4 JTIDS Transmit Processing

The microprocessor performs the encoding and interleaving of the JTIDS message. In addition, it performs the 32-ary cyclic encoding of the data. This consists of converting data in 5-bit groups into a cyclic shift of a fixed predetermined 32-bit code. The code word would subsequently be processed in a transmit digital signal generator. In this module, the baseband data is mixed with the PN code and the resulting data is minimum shift keyed (MSK) modulated. The modulator would be implemented as a ROM, which generates a digital sample representation of the quadrature MSK components. The ROM outputs are converted to analog form in a D/A converter and lowpass filtered. This method of modulation is very flexible in that it can be readily adapted to different forms of modulation if required. By changing the values stored in the waveform ROM, different modulation formats can be generated.

The baseband quadrature components are modulated onto quadrature 70 MHz carriers and combined in the Modulator module.

2.4 Signal Processing Algorithms

The signal processing algorithms to be implemented in the MSP are presented here in the form of flow diagrams. The processing rates are also given to indicate the operating speed required of the various processing elements. A loading analysis for the MSP is presented showing the fractional utilization of the capacity of the machine.

These algorithms are of a standard type in some cases, such as the Costas loop and the early/late loop, or they are the result of design studies, such as the GPS acquisition algorithm. The intent here is not to

derive "optimum" processing algorithms, but to present representative examples of algorithms which may be used in modems to demonstrate the feasibility of the SAM concept.

Figure 4 shows the relationship of the processing algorithms, which reside in the MSP, and the rest of the SAM terminal hardware. As shown, the primary interfaces are with the Special Purpose Processor for received data, the Doppler Wipeoff module for frequency control and the Code Generator for PN code control. The algorithms within the MSP include the GPS frequency and code acquisition algorithm, a frequency-locked loop, phase-locked loop, code tracking loop, bit sync loop and a Manchester/bit sync algorithm for GPS. In addition, a gain control algorithm is included which functions as a normalizer to preserve the dynamic range of the processor.

The algorithm outputs include bi-phase or quad-phase data, a pseudo-range estimate from the code tracking loop, a range rate estimate from the phase-locked loop and clock control signals from the bit sync loops. The control for the Doppler Wipeoff module comes from the phase-lock/frequency lock loop in the form of digital tuning commands. The code tracking loop provides a control signal to the timing circuit of the code generator to mechanize timing shifts. Other outputs include an initial sync marker for GPS code acquisition and a Manchester/bit sync marker for GPS.

2.4.1 GPS Algorithm Flow (P Code)

The sequencing of algorithms for GPS P code processing is shown in Figure 5. The first algorithm to be activated is the acquisition algorithm, which provides a coarse estimate of signal frequency and PN code state. The algorithm runs continuously until coarse acquisition is declared, at which point the acquisition verification algorithm is initiated. The verification algorithm is of fixed duration at the end of which an indication will be given as to whether the coarse acquisition estimate was valid or not. If not, then the terminal reverts back to the acquisition algorithm. If acquisition is verified, then the frequency locked loop and code locked loop algorithms are initiated simultaneously.

The frequency locked loop algorithm has two modes of operation, a wideband and a narrowband mode. In the wideband mode, if the lock detector indicates an out-of-lock condition, the terminal reverts to the acquisition

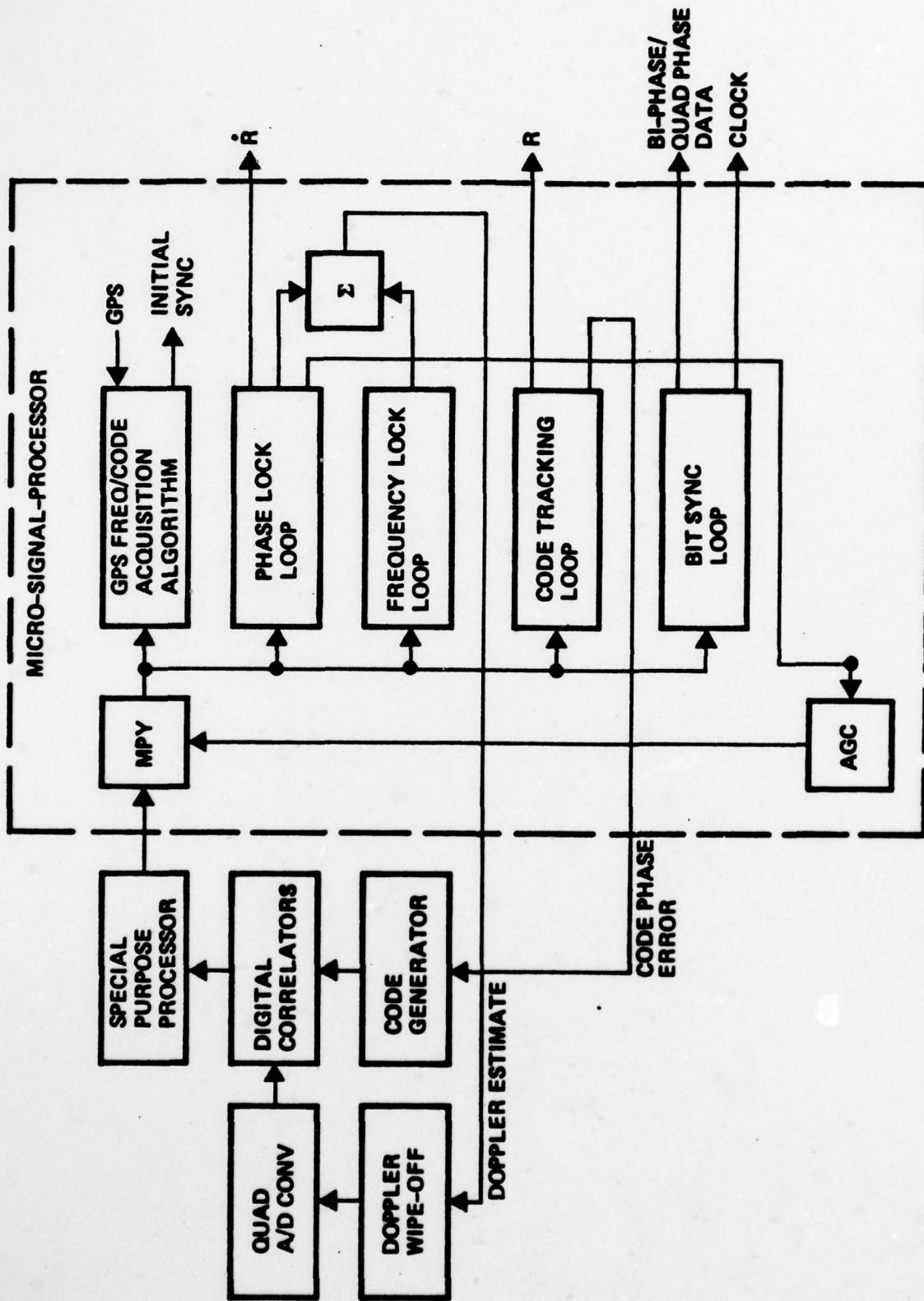


Figure 4. MSP Signal Processing Algorithms Interrelationship

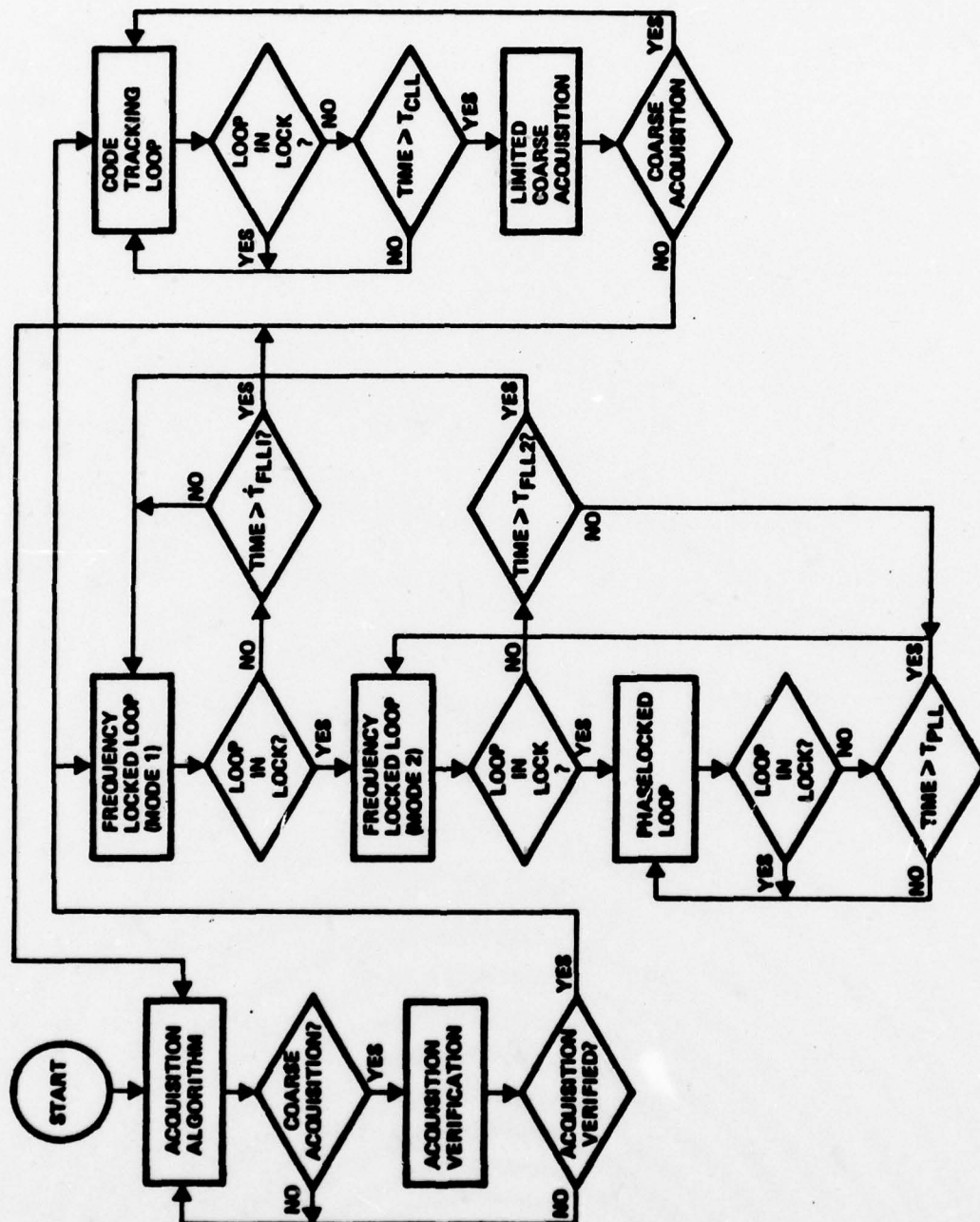


Figure 5. GPS Algorithm Flow (P Code)

algorithm. In the narrowband mode, an out-of-lock indication causes the terminal to revert back to the wideband mode. Once frequency lock is obtained, the phase-locked loop algorithm is activated. If phase-lock is lost, then the narrowband mode of the frequency locked loop is activated.

The code tracking loop also utilizes a lock indicator to trigger a limited coarse acquisition search if loss of code lock is indicated.

2.4.2 GPS Algorithm Flow (C/A Code)

The algorithm sequencing for the C/A code Figure 6 is slightly different than that for the P code because of the Manchester sync and bit sync requirement. Manchester sync must be acquired before the transition can be made from mode 1 of the frequency-locked loop and code tracking loop to mode 2. Similarly, bit sync must be acquired to transition to mode 3. In the frequency-locked loop, the different modes correspond to different discriminator bandwidths. In the code tracking loop, they correspond to increased integration times.

2.4.3 GPS Code/Frequency Acquisition

Coarse estimates of signal frequency and code timing are made simultaneously in the GPS acquisition algorithm. Figure 7 is a functional representation of the algorithm and also shows the data rates at several points for the normal mode (C/A code) and direct mode (P code). The algorithm is basically a fixed sample size test in which multiple hypotheses are tested simultaneously. The suggested approach tests 16 time hypotheses and four frequency hypotheses simultaneously, utilizing the capabilities of the parallel digital correlator and the ability of the MSP of perform a 4-point discrete Fourier transform.

Input data is sampled at twice the PN rate and input to the correlator modules. The correlator reference code remains fixed as the input signal is shifted in for 16 samples. The correlator outputs for the 16 samples are added to the existing 16 values in the accumulator. After 16 samples are taken, the correlator reference code is advanced by 16 clocks which results in the reference code having the same timing relationship relative to the incoming signal as at the start of the previous 16 correlation

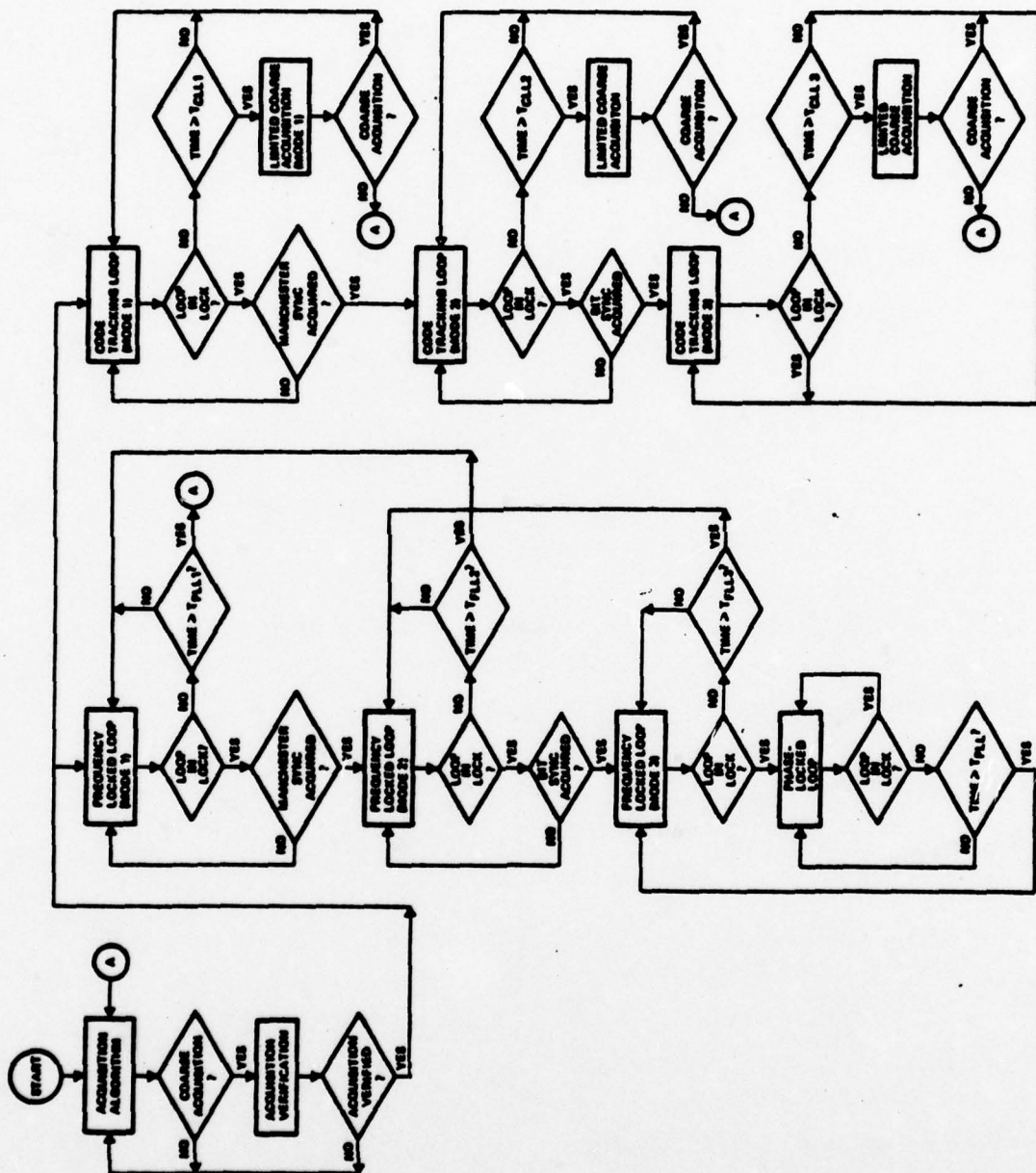
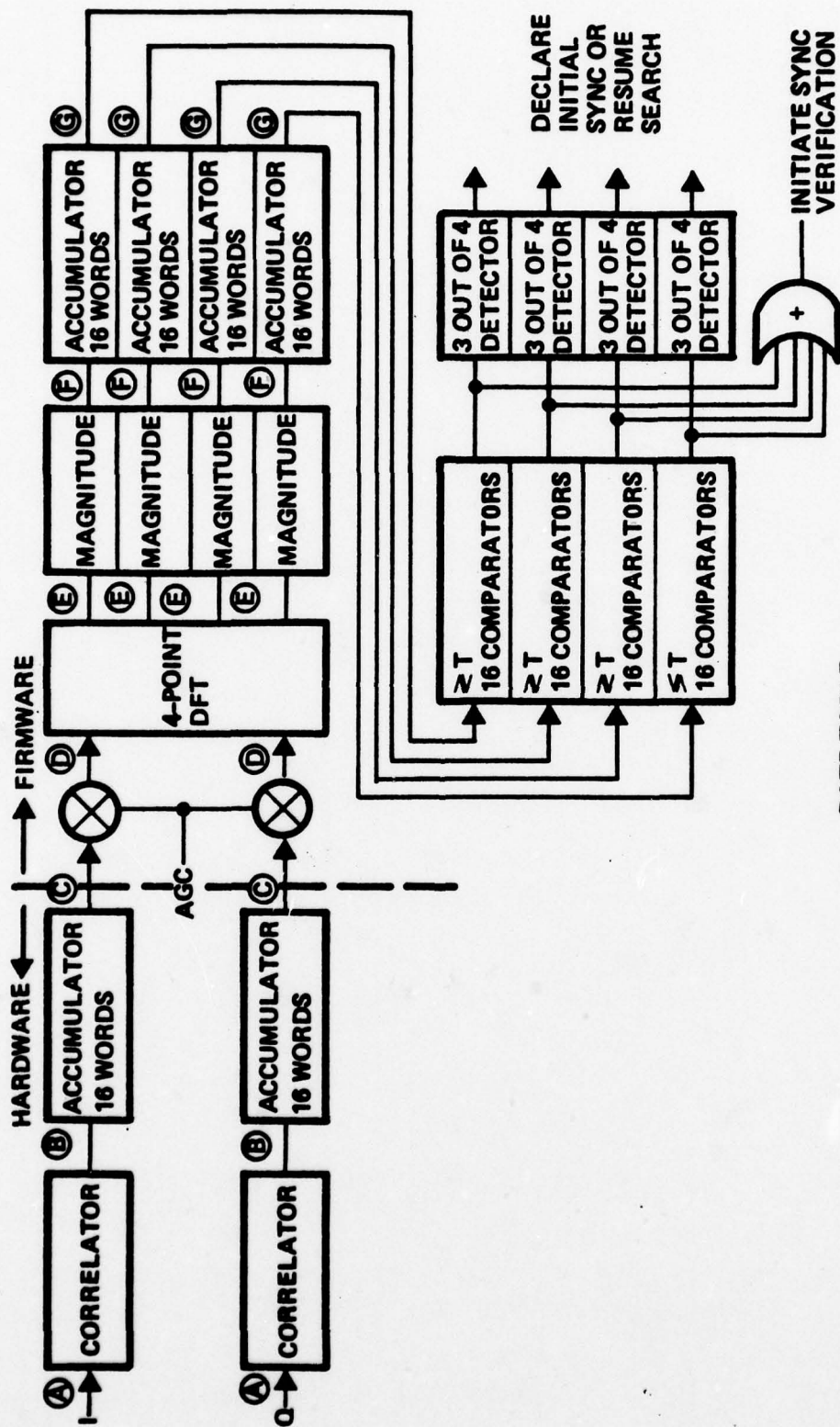


Figure 6. GPS Algorithm Flow (C/A Code)



RATE TABLE

	A	B	C	D	E	F	G
NORMAL MODE	2.046×10^6	16×64000	16×4000	16×4000	16×1000	16×1000	16×20
DIRECT MODE	20.46×10^6	16×640000	16×800	16×800	16×200	16×200	16×20

Figure 7. GPS Code/Frequency Acquisition

samples. As a result, the values stored in each of the 16 words of the accumulator corresponds to one of 16 time hypotheses. Note that in-phase and quadrature values are accumulated independently, resulting in a coherent integration. The correlator output is sampled 16 times for every 32 input clocks, so the sample rate is 16 times the input rate divided by 32. This results in a correlator output rate of 16×64000 per second for the C/A code or 16×640000 for the P code. These are average rates. The correlator outputs actually occur in 16 word bursts where 16 consecutive outputs occur at twice the average rate followed by a dead time of equal duration during which the reference code is the correlators being advanced.

The degree of part correlation accumulation is selected based upon the desired processing bandwidth. For the C/A code, each of the 16 time hypotheses variables is accumulated independently and for each hypothesis, 16 consecutive samples are accumulated. This results in an average rate out of the accumulator of 16×4000 per second and corresponds to a processing bandwidth of 4000 Hz. This bandwidth encompasses the full residual frequency uncertainty for the GPS C/A code. For the P code, 800 samples are accumulated resulting in an output rate of 16×800 and a bandwidth of 800 Hz.

The accumulator outputs are multiplied by a gain control input to maintain the dynamic range of the digital processing. The result is then processed in a 4 point DFT. Each DFT output corresponds to a filter having bandwidth and filter spacing equal to $1/4$ the input bandwidth. Each DFT output occurs at a rate of 16×1000 for the C/A code or 16×200 for the P code. The magnitude $(I^2 + Q^2)$ of each output is computed and the results are accumulated further in four accumulator banks of 16 words each. Note that this is a noncoherent accumulation of samples so that the bandwidth remains constant. For the C/A code, 50 accumulations are performed and for the P code, 10 accumulations are performed.

The accumulator outputs constitute a 16×4 matrix corresponding to one of 16 time hypotheses and one of 4 frequency hypotheses. The presence of a signal is determined by comparing each of these accumulator outputs to a threshold. Any threshold exceedance will cause the sync verification mode to be entered, in which the hypothesis in question is examined again for three additional times, using the same processing bandwidths and inte-

gration times as before. If the threshold is exceeded two out of these three tests, the modem is declared to have acquired initial sync. If not, the acquisition search is resumed.

2.4.4 Frequency-Locked Loop

The frequency-locked loop tracks doppler rate with no steady-state error and jerk with finite steady-state error. It features variable discriminator bandwidth allowing the bandwidth to be optimized for each operating mode. Wider bandwidths are used for initial pull-in and narrower bandwidths are used for fine tracking. The combination of the frequency locked loop algorithm and Doppler Wipeoff module provides a frequency resolution of 0.6 Hz and a tracking range of ± 19.7 KHz. This is sufficient to meet all requirements for the SAM terminal.

The algorithm is shown in Figure 8. The correlator and first accumulator operate at the same rates as in the acquisition algorithm. The difference is that only one channel is required, rather than 16. The second accumulator determines the discriminator bandwidth. Depending on the degree of accumulation, bandwidths ranging from 4 KHz down to 200 Hz for the GPS normal mode, and 800 Hz down to 200 Hz for the direct mode are provided. Utilization of the lower bandwidths in the normal mode requires that the Manchester code be removed prior to accumulation. The accumulator outputs are processed in a 4 point DFT in which only the central two points are computed. The DFT output rates range from 1 KHz down to 50 Hz. The magnitudes of the outputs are calculated and subtracted. This forms the discriminator characteristic which is based upon differencing the outputs of two filters, one offset higher and one lower than center frequency. The discriminator output is then filtered in a second-order filter and the result drives the numerically controlled oscillator in the Doppler Wipeoff module.

2.4.5 Phase-Locked Loop

The phase-locked loop is a third-order loop which is capable of tracking a frequency jerk with finite steady-state error. It is a decision-feedback configuration which offers improved performance over a Costas loop at high signal to noise ratios and is easier to implement for quad-phase data. The combination of this algorithm with the Doppler Wipeoff module provides a phase tracking resolution of 0.35° .



Figure 8. Frequency Locked Loop

Figure 9 shows the algorithm. The correlator and accumulator function in the same manner as for the frequency locked loop. For application to the generic PSK forms of modulation, the correlator input rate is twice the PN rate or 64 times the data rate if the signal is not PN coded. The correlator output rate is then the input rate divided by 32. The accumulators then provide further integration of the correlator outputs with a resultant output rate equal to the data rate in the PN coded cases, and twice the data rate in the non-PN coded cases.

Further accumulation is performed which reduces the sample rate to the data rate for all cases and the result is then threshold. The output of the threshold comparison is an estimate of the data, and is used to multiply the phase error signal generated in the quadrature channel. For bi-phase operation, only one of the comparators is required. The error signals generated in each channel are summed and input to a second-order filter whose output drives the NCO in the Doppler Wipeoff module.

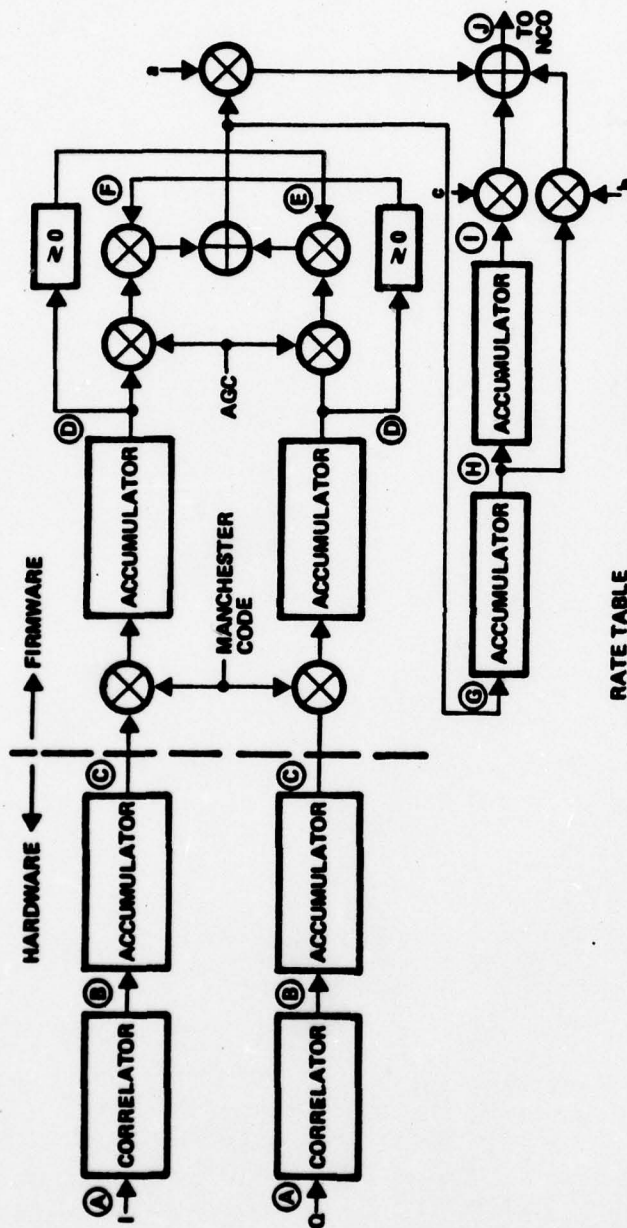
2.4.6 Code Tracking Loop

The code tracking loop is a classical early-late configuration in which timing error signals are generated by differencing correlation measurements taken $1/2$ chip early and $1/2$ chip late relative to nominal time. The second-order loop tracks code doppler with zero steady-state error and is implemented to provide timing resolution of $1/8$ chip.

Figure 10 shows the code tracking algorithm. The hardware correlator is time shared to generate the early and late correlation measurements. The accumulators following the correlator integrate the early and late values independently. These values are also maintained independently through the firmware accumulator stage. The magnitudes of the early correlation and the late correlation are then computed and differenced to generate the timing error signal. The processing bandwidths vary according to the mode of operation as determined by the degree of accumulation. The error signal is filtered in a proportional plus integral filter whose output controls the clock frequency in the timing generator.

2.4.7 GPS Manchester/Bit Sync

In processing the GPS C/A code, it is necessary to resolve Manchester and bit sync prior to demodulation of data. The algorithm shown in Figure 11 is a noncoherent transition detector which performs both these functions. The inner product of the accumulated data for two successive clock



RATE TABLE

	A	B	C	D	E	F	G	H	I	J
GPS NORMAL MODE	2.046×10^8	64000	4000	50	50	NA	50	50	50	50
GPS DIRECT MODE	20.46×10^8	640000	800	50	50	NA	50	50	50	50
GENERIC - PN RATE PR	2 γ	PR/16	DR	DR	DR	NA	DR	DR	DR	DR
GENERIC - PN RATE - 0	2 γ	2 x DR	2 x DR	DR	DR	NA	DR	DR	DR	DR
GENERIC - PN RATE PR	4 γ	PR/16	DR	DR	DR	NA	DR	DR	DR	DR
GENERIC - PN RATE - 0	4 γ	2 x DR	2 x DR	DR	DR	NA	DR	DR	DR	DR

Figure 9. Phase-Locked Loop

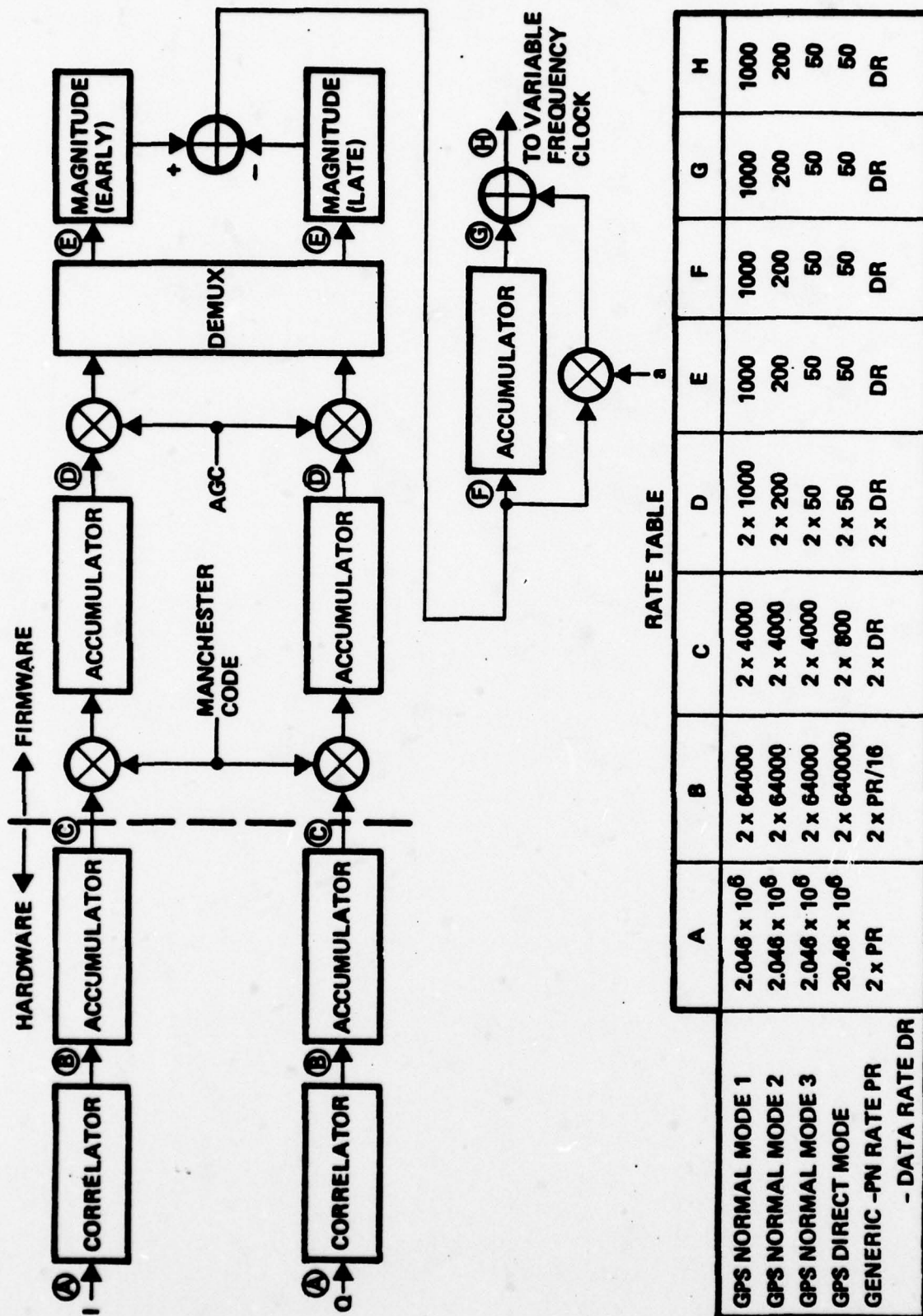
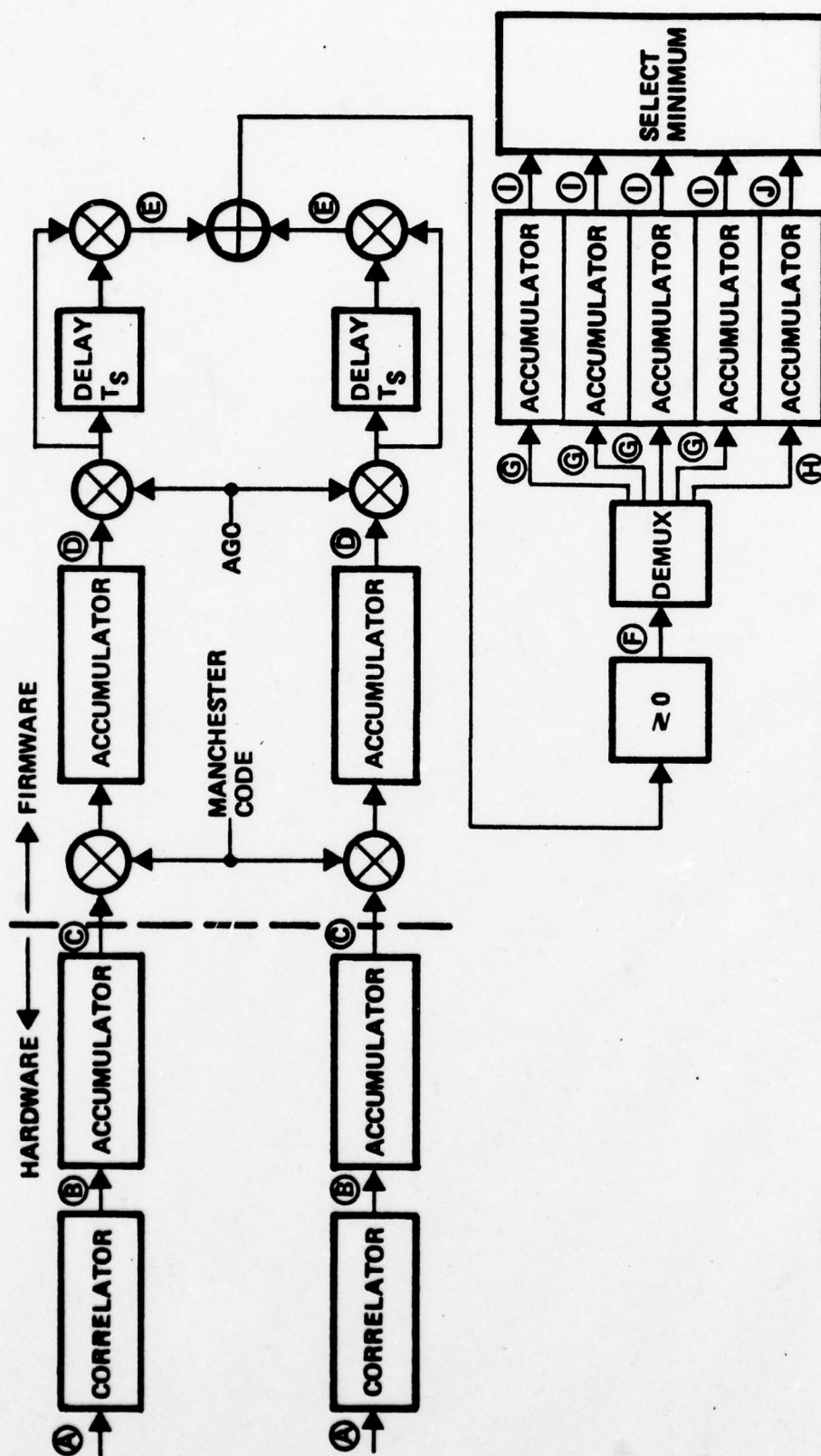


Figure 10. Code Tracking Loop



RATE TABLE

	A	B	C	D	E	F	G	H	I	J
MANCHESTER SYNC	2.046 x 10 ⁶	64000	4000	1000	1000	1000	200	200	2	2
BIT SYNC	2.046 x 10 ⁶	64000	4000	200	200	200	50	NA	2	NA

Figure 11. GPS Manchester/Bit Sync

intervals is computed and compared to a threshold. If a transition has occurred, the inner product will be negative. If no transition has occurred, the inner product will be positive. The number of positive and negative threshold crossings is accumulated over a number of clock intervals for each of the possible transition locations (5 for Manchester sync and 4 for bit sync). At the end of the accumulation interval (0.5 second) the accumulator containing the smallest (most negative) quantity will correspond to the correct transition point. The algorithm is implemented twice in succession, once for Manchester sync and once for bit sync.

2.4.8 Data Transition Tracking Loop

For non-PN coded generic PSK data, it is necessary to track the bit transition point for efficient demodulation. The data transition tracking loop shown in Figure 12 performs this function by integrating across a data bit transition to generate a timing error signal and using the transition detection to determine the direction of the error.

The output of the hardware accumulator consists of $1/2$ bit integrations. These outputs are combined in one case to form an integration over a full bit and these are compared to a zero threshold. The comparator outputs are used to determine whether or not a bit transition has occurred. The $1/2$ bit integrations are also combined such that the result is an integration over $1/2$ of one bit and $1/2$ of the succeeding bit. This result is then delayed by $1/2$ bit to align it with the transition detector output. If a transition has occurred, then the mid bit integration results represent a legitimate error signal and it is gated through to the loop filter. If a transition has not occurred, the error signal is not valid and is not gated through to the loop filter. The loop filter is an integral plus proportional filter which provides the capability to track bit rate doppler with no steady-state error. Timing resolution to $1/24$ bit is provided.

2.4.9 MSP Data Processing Load

An estimate of the MSP loading for the various algorithms presented previously was performed and the results are summarized in Table 16. The number of instructions required for each of the algorithms is given in the upper left of the table. For GPS, the maximum data rate into the MSP is 4000 sets of 16 words each second. This occurs during acquisition as can be seen in the table of Figure 7. Thus the allowable processing time for

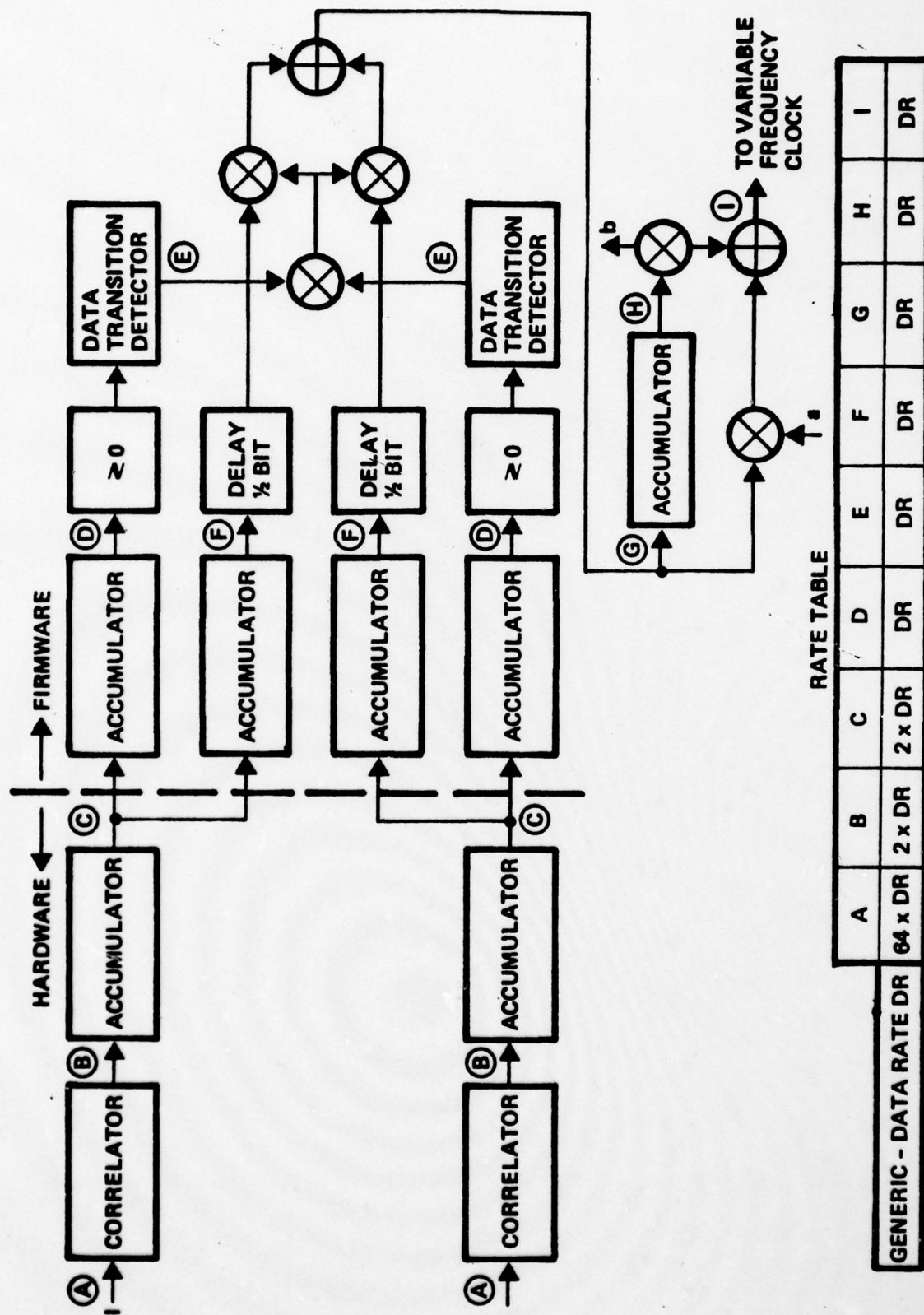


Figure 12. Data Transition Tracking Loop

each set of 16 words is 125 msec. For the generic class of PSK waveforms, the highest input rate to the MSP is six words per data bit which at the highest data rate is 230.4×10^{-3} samples per second or equivalently, the allowable processing time is 26 msec per data bit.

The table shows the processing time required to perform the algorithm of GPS and for the generic PSK waveforms. In each case the required time is less than the available time. Note that for all functions, several algorithms must be performed simultaneously.

2.5 Performance Analysis

The following analyses were performed to aid in selecting design parameters for the SAM terminal and to provide an estimate of the level of performance to be expected from the terminal. In most cases, a summary of the results is presented here and the detailed analyses are presented as appendices.

2.5.1 Digital Modulation Distortion of MSK Signals

The modulator proposed for the SAM terminal is a digital modulator in which in-phase and quadrature components of the signal are digitally synthesized and subsequently converted to analog form. It is of interest, therefore, to know what the effect of sample rate and filtering is on the waveform distortion, which can be considered transmitted noise. Figure 13a shows the set-up of the problem. The MSK waveform, represented by in-phase and quadrature components, consists of half-sine waves. The sampled waveform consists of a staircase function which approximates the sine shape. The staircase function is then filtered in a lowpass filter and the parameter of interest is the error between the filtered waveform and the ideal sine wave. Mean square error was selected as the criterion of distortion. It is also possible to define a signal-to-noise ratio as shown in Figure 13b.

The mean square error and signal-to-noise ratio were computed for a variety of filter types and sample rates. The results are summarized in Figure 14. The dashed lines indicate the effect of minimizing the mean square error through the choice of the parameter t shown in Figure 13a. As can be seen, a signal-to-noise as high as 27 dB can be obtained by using a 3-pole Butterworth filter at a sample rate of 5 samples per pulse. Also shown in Figure 14 for comparison are the results if no filter is used. To

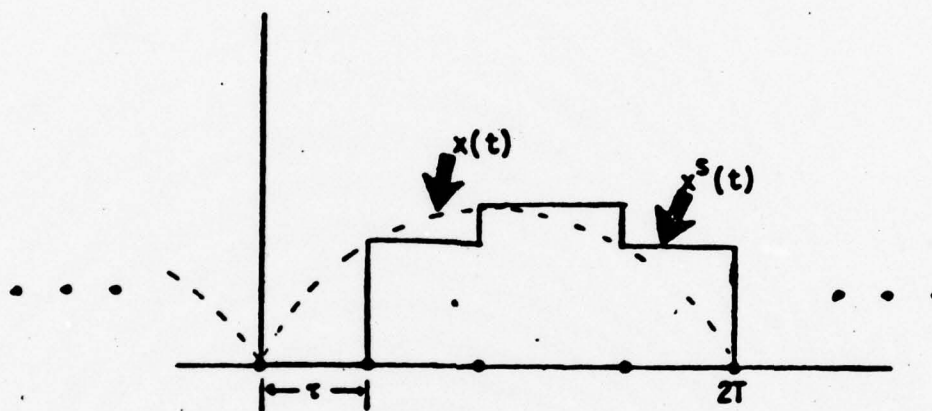


Figure 13A. Sampled MSK Pulse



Figure 13B. MSK Distortion Model

$$\text{SNR} = \frac{\text{CONTINUOUS WAVEFORM ENERGY}}{\text{MEAN-SQUARE ERROR}} = \frac{0.5}{\text{MSE}}$$

Figure 13C. SNR Definition

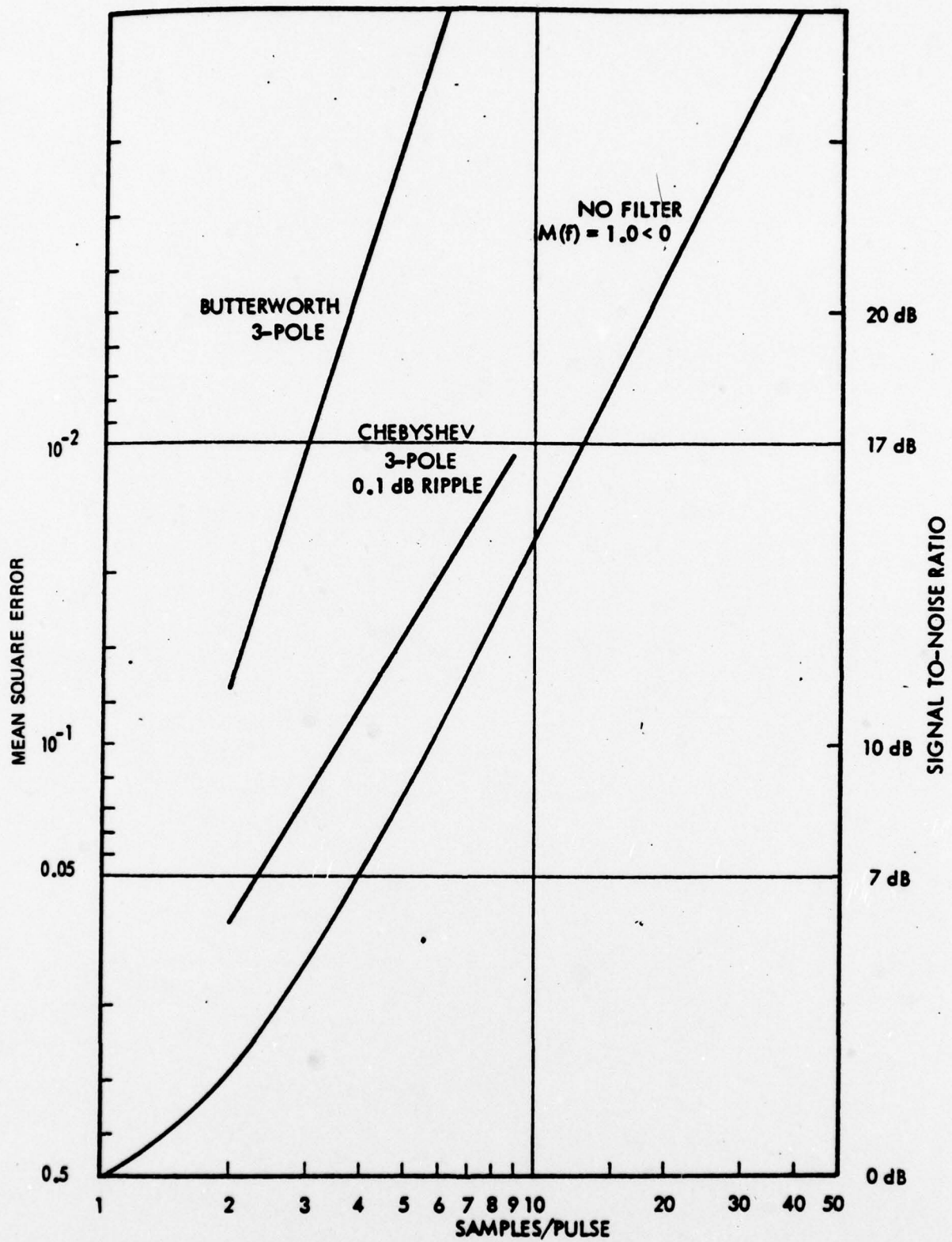


Figure 14. MSK Waveform Distortion

obtain the same signal to noise ratio, a sample rate as high as 40 samples per pulse must be used. The analysis shown here is presented in detail in Appendices A and B.

2.5.2 Quantization and Dithering

The SAM terminal is dependent on digital signal processing to provide the required flexibility to adapt to different waveform processing requirements. As such, considerable effort was spent on analyzing the effects of amplitude quantization on the receiver performance. In addition, the technique of adding dither to enhance performance was also investigated. Figure 15 summarizes the approach to the problem. We are interested in comparing the performance of the digital processor, in particular the digital correlator, to an ideal analog correlator. The criterion of performance is signal-to-noise ratio; defined as the ratio of the square of the mean to the mean square value at the output of the correlator. Two situations are of general interest, one in which Gaussian noise is the predominant form of disturbance, and the second in which CW interference is predominant. The effects of dither addition are indicated.

Figure 16 shows the model used for this analysis. It is a non-coherent M-ary digital demodulator. The received signal is converted to in-phase and quadrature channels and filtered to remove double frequency terms. The dither waveform is then added at this point and the signals are sampled and quantized. The quantized samples are then correlated against the reference sequence in a digital correlator, whose output is proportional to the number of agreements between the received sequence and the reference sequence. The correlator outputs are then squared and added to form the decision variable. We are interested in the signal-to-noise ratio at the output of the correlators. Parameters of interest are the quantizer threshold settings relative to the input level, and the number of levels of quantization.

Two basic types of memoryless quantizers were examined. Figure 17 shows the transfer characteristic for a hardlimiting quantizer having an even number, 26, of output levels. This type of quantizer is characterized by an output step at the zero level input. Figure 18 shows a deadzone quantizer which is characterized by zero output for inputs in a deadzone region around zero. This quantizer has an odd number, 26-1, of levels.

- **PURPOSE**

DETERMINE THE EFFECTS OF AMPLITUDE QUANTIZATION AND ADDITION OF A DITHER WAVEFORM TO DIGITAL CORRELATION RECEIVER PERFORMANCE

- **METHOD**

EVALUATE QUANTIZATION LOSS FACTOR, L , FOR DIFFERENT QUANTIZER CHARACTERISTICS AND INPUT NOISE CONDITIONS

$$L \triangleq \frac{\text{SNR}_q}{\text{SNR}_0}$$

WHERE SNR_q = OUTPUT SNR FOR QUANTIZING RECEIVER

SNR_0 = OUTPUT SNR FOR LINEAR MATCHED FILTERING

EVALUATE EFFECTS OF ADDITION OF A DITHER WAVEFORM TO A/D INPUT

- **RESULTS PRESENTED**

QUANTIZATION EFFECTS WITH WHITE GAUSSIAN NOISE

QUANTIZATION EFFECTS WITH NARROWBAND INTERFERENCE

EFFECTS OF DITHER ADDITION

Figure 15. Quantization and Dithering

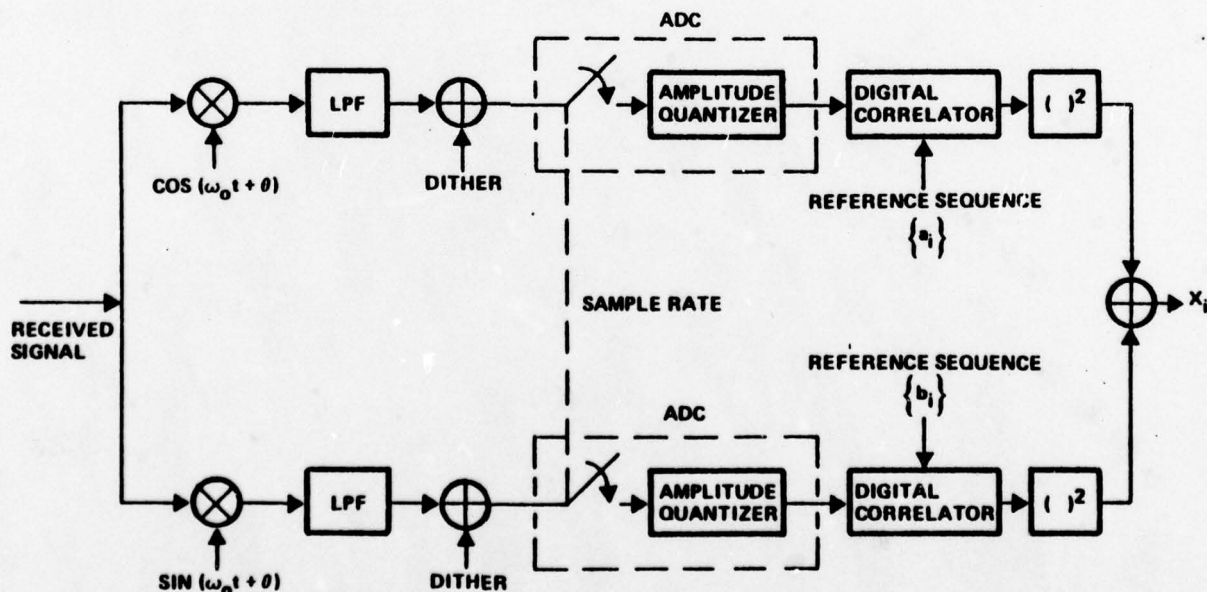


Figure 16. Non-Coherent M-ary Digital Processing Demulator

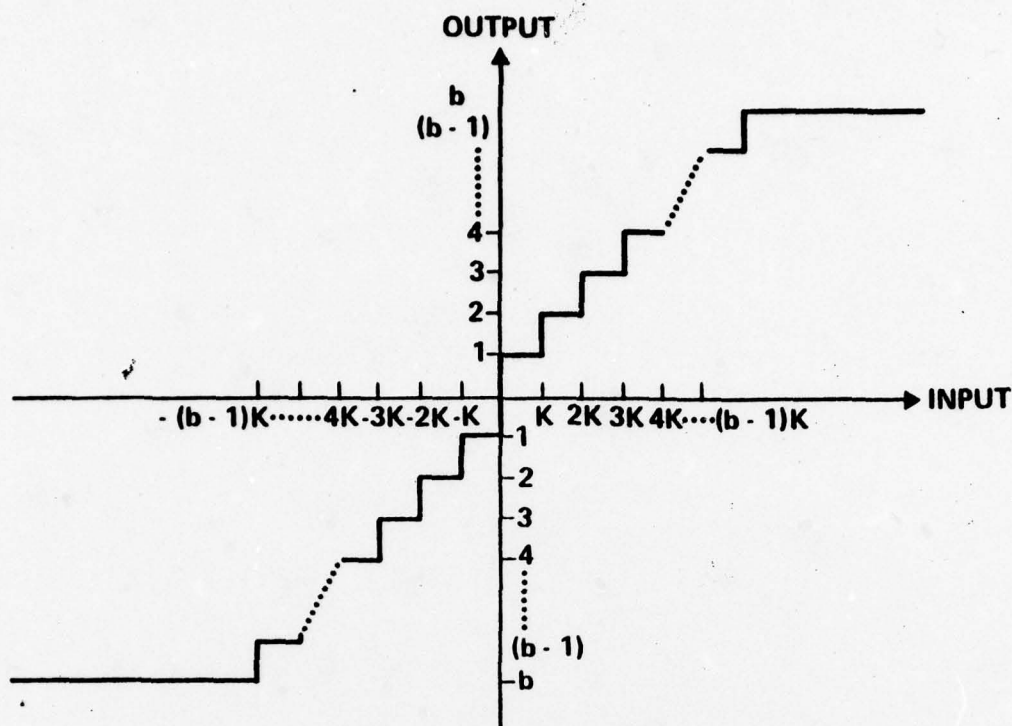


Figure 17. Hardlimiting Quantizer Characteristic
Even Number $2b$ of Intervals

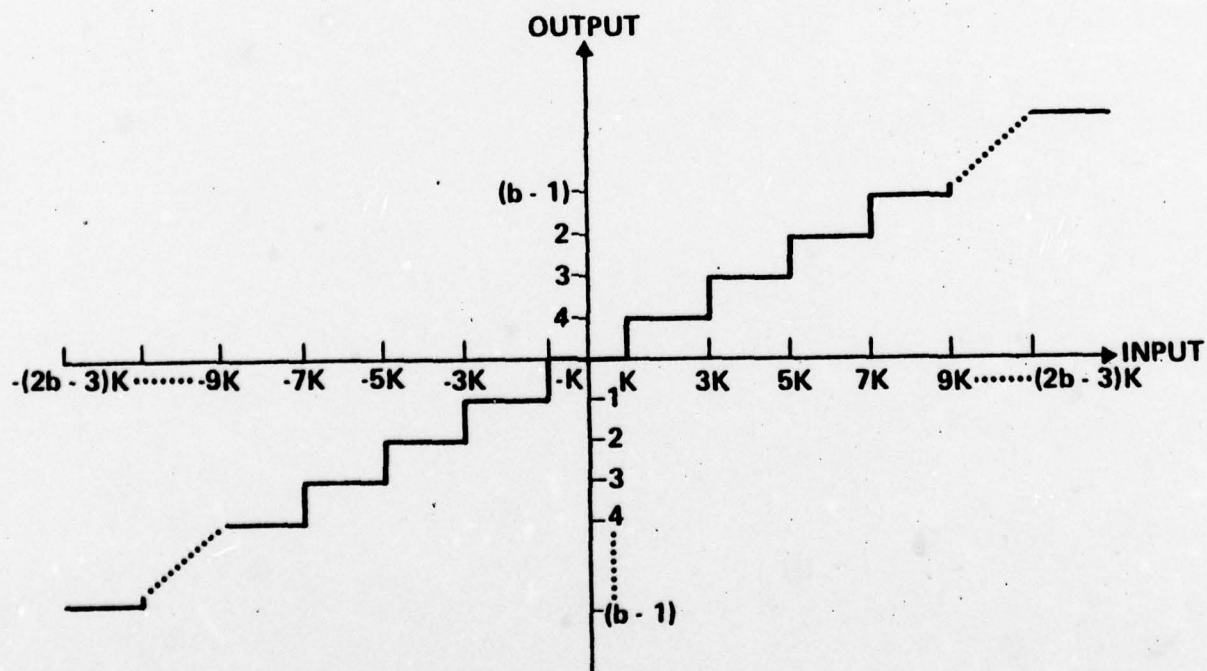


Figure 18. Deadzone Quantizer Characteristic
Odd Number $2b-1$ of Intervals

An analysis was performed to determine the loss in signal to noise ratio due to quantization as a function of the number of quantization levels. The results for Gaussian noise are shown in Figure 19. The loss ranges from approximately 2 dB for a two-level hardlimiting quantizer (1 bit), down to less than 0.2 dB for a 15 level deadzone quantizer (4 bits). It was determined from these results that a 4 level quantizer presented the best tradeoff of performance (0.7 dB loss) versus complexity.

A general four level quantizer characteristic is shown in Figure 20. The maximum output values are normalized at ± 1 and the intermediate values are $\pm k$. The input thresholds are at $\pm q$. It is of interest to know the optimum values for k and q . Figure 21 is a plot of the loss factor L as a function of the threshold value q for various values of k . The optimum value for k appears to be $k = 1/3$ with a corresponding threshold setting of $q = \sqrt{N}$ where N is the noise power at the input to the quantizer. Note, however, that the curve for $k = 1/3$ displays a rather broad maximum, allowing for errors in the threshold setting. These results indicate the necessity for some form of gain control to maintain the threshold levels at the proper point. The results for $k = 1$ correspond to a hardlimiting two level quantizer and those for $k = 0$ correspond to a three level deadzone quantizer. For the deadzone quantizer, as the threshold increases, the loss increases since threshold crossings caused by the signal decrease. In effect, the signal is suppressed. For hardlimiting quantizers, however, increasing the threshold results in the quantizer degenerating to a two-level hardlimiting quantizer.

The loss factor L was also computed for CW interference and the results are shown in Figure 22. The results differ significantly from the Gaussian noise case. For certain threshold settings, the digital correlator provides better performance than the analog correlator ($L > 1$). This is not inconsistent with theory since the analog correlator is only optimum for Gaussian noise interference. The threshold setting, however, is fairly critical. As can be seen, there is a sharp drop in performance if the threshold is set higher than the RMS level of the interference. This is true because at this point the signal (which is assumed to be much smaller than the interference) can no longer cause a threshold crossing and the 4 level quantizer degenerates to a 2 level quantizer. To allow for gain

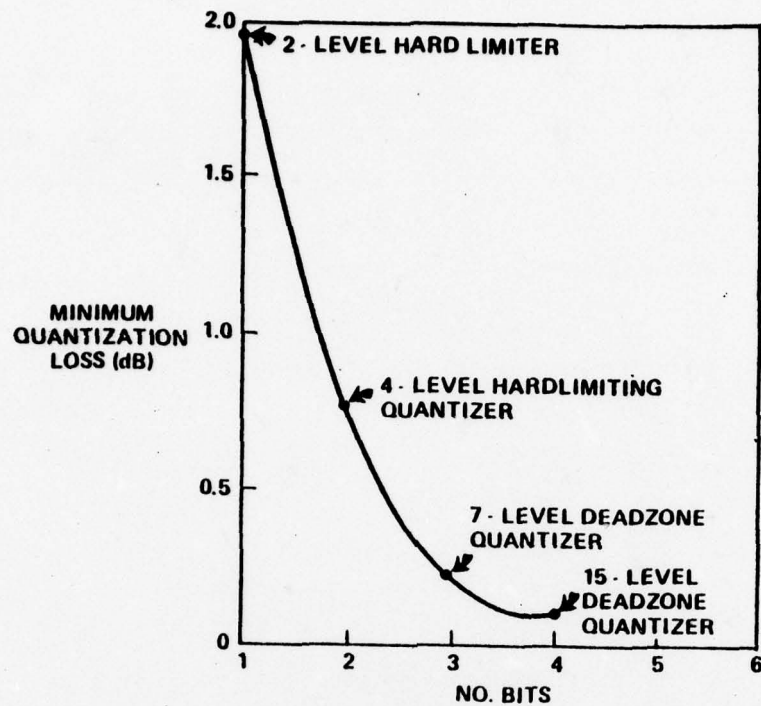


Figure 19. Minimum Quantization Loss vs Number of Bits (in Gaussian Noise)

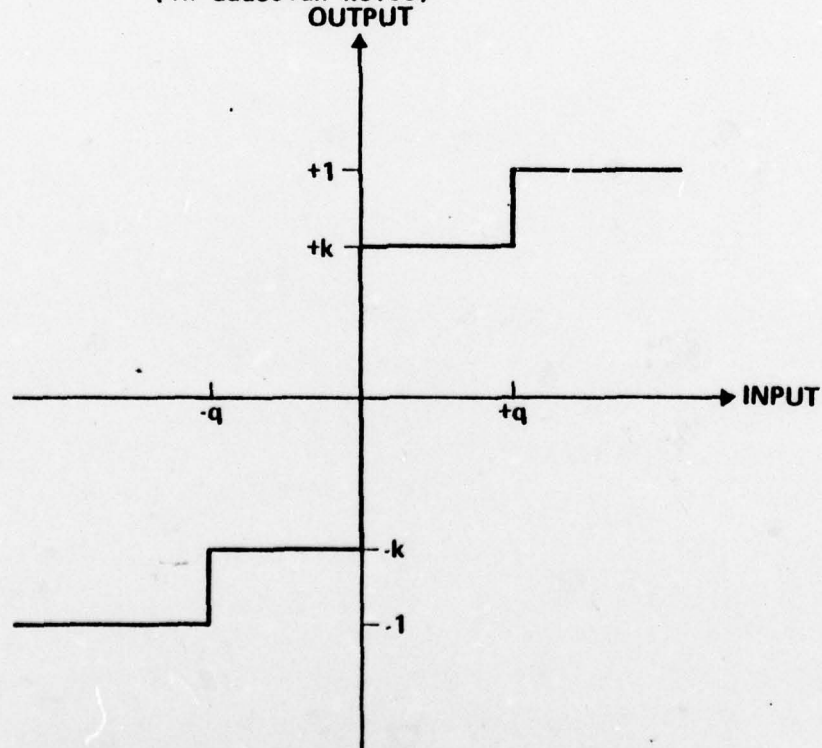


Figure 20. General Four Level Quantizer Characteristic

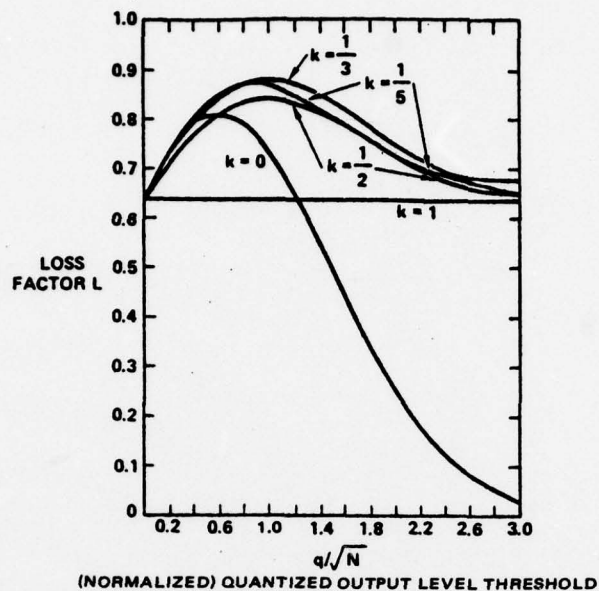


Figure 21. Loss (L) in Output SNR for Four-Level Quantized DMF in (Strong) Additive Gaussian Noise

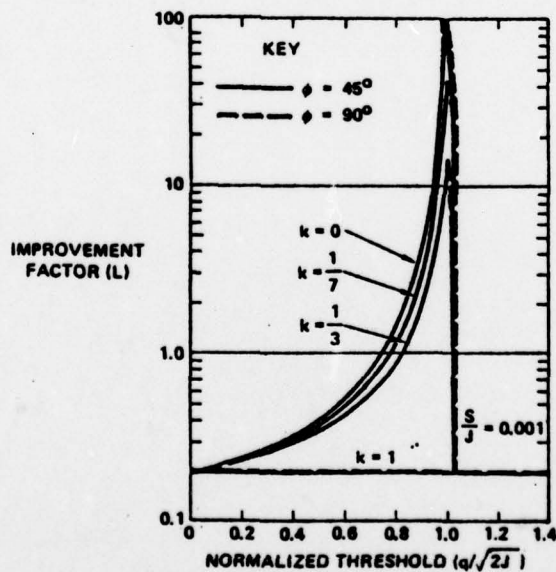


Figure 22. Improvement Factor as a Function of Quantizer Parameters for 4-Phased Digital Matched Filter ($S/J = 0.001$) in CW Interference

control errors, the threshold can be set at approximately $q = 0.8\sqrt{2J}$ which provides reasonable performance in Gaussian noise or CW interference.

The reason CW interference is so effective in a digital correlator is that for small signal-to-noise ratio and certain choices of interference amplitude, the sum of signal plus interference will with high probability fall between the thresholds with the quantizer output being independent of the signal polarity. Thus, the signal is completely suppressed. The addition of dithering to the signal prevents this "capture" effect. By adding noise to the signal, the probability that the sum of signal plus interference plus dither will fall close to a quantizer threshold such that the signal polarity will determine the quantizers output level is increased. This effect results if the dither amplitude and distribution are selected appropriately. Figure 23 shows the effect of adding triangle dither where the peak-to-peak dither amplitude is equal to the quantizer step size. It is assumed that the dither frequency is much higher than the data rate so that sufficient averaging occurs over a data bit interval. The loss in signal-to-noise ratio relative to an ideal correlation is plotted versus the ratio of interference amplitude to quantizer step size. Again, a requirement for some form of gain control is indicated to maintain the interference amplitude somewhere between 0.5Δ and 1.5Δ for best performance (2 bit quantizer). If the interference amplitude falls below 0.5Δ , then the quantizer noise, proportional to Δ^2 , is large compared to the jammer power and hence the SNR is significantly affected. For larger values of AJ , however, the degradation is not significant since Δ^2 is small compared to jammer. As the ratio of AJ to W increases, there is a point at which performance again degrades because the A/D converter saturates. The point of saturation is a function of the number of quantization levels. A significant result, however, is that with proper AGC, loss in CW interference is independent of the number of quantization levels.

Figure 24 summarizes the results of the A/D analysis. The detailed analysis is contained in Appendix C.

2.5.3 Carrier Acquisition and Tracking - Frequency Locked Loop versus Phase-Locked Loop

A frequency locked loop and phase-locked loop were compared in terms of frequency acquisition time and RMS frequency tracking error. Figure 25

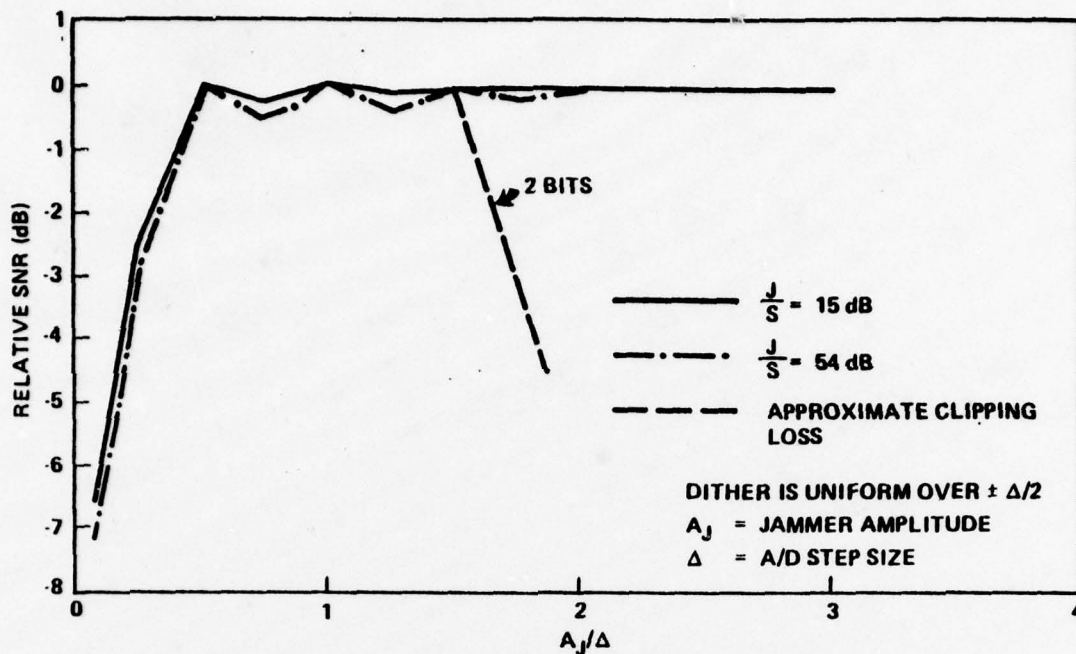


Figure 23. SNR Loss for Triangle Dither with Hardlimiting A-D in CW Interference

- **QUANTIZATION AND GAUSSIAN NOISE**

1 BIT QUANTIZER	—	1.96 dB LOSS
2 BIT QUANTIZER	—	0.74 dB LOSS
3 BIT QUANTIZER	—	0.24 dB LOSS

- **2 BIT HARDLIMITING (4 LEVEL) QUANTIZER GIVES GOOD PERFORMANCE IN COMBINED GAUSSIAN NOISE PLUS NARROWBAND INTERFERENCE**
- **A LOW FREQUENCY DITHER WAVEFORM REDUCES THE PROBABILITY OF COMPLETE SIGNAL CAPTURE BY A TONE INTERFERER**
- **A SAWTOOTH DITHER SHOULD BE USED WITH A DITHER PEAK TO JAMMER PEAK AMPLITUDE RATIO ≈ 1.4**
- **AGC IS NECESSARY TO PROPERLY LOAD THE A/D. AGC ACCURACY WITHIN 1 dB IS SUFFICIENT**
- **LOSS IN CW INTERFERENCE WITH DITHERING IS INDEPENDENT OF THE NUMBER OF LEVELS OF QUANTIZATION WITH PROPER AGC**

Figure 24. Results

- COMPARE PERFORMANCE OF FLL AND PLL IN TERMS OF ACQUISITION TIME AND RMS FREQUENCY ERROR
- DETERMINE DESIGN GUIDELINES FOR BOTH SYSTEMS
- METHOD
 1. CHOOSE LOOP BANDWIDTH SO AS TO OPTIMIZE TRADEOFF BETWEEN DYNAMIC TRACKING ERROR AND RMS ERROR DUE TO NOISE

$$\begin{array}{ll} \text{FLL: DYNAMIC FREQ ERROR} = \sigma_F & \longrightarrow B_{LP} \\ \text{PLL: DYNAMIC PHASE ERROR} = \sigma_\phi & \longrightarrow B_{LP} \end{array}$$
 2. DETERMINE σ_F AT THIS LOOP BANDWIDTH
 3. DETERMINE ACQUISITION TIMES FOR FREQ STEP INPUT

$$\begin{array}{ll} \text{FLL: } T_{ACQ} \triangleq \text{TIME FOR } \Delta f \text{ TO DECAY TO } \Delta f_0 \\ \text{PLL: } T_{ACQ} \triangleq \text{DURATION OF CYCLE SLIPPING TO REDUCE } \Delta f \text{ TO } \Delta f_0 \end{array}$$

Figure 25. Carrier Acquisition and Tracking Frequency - Locked Loop vs Phased-Locked Loop

shows the general method used in the analysis. First, the loop bandwidth was selected so as to optimize the tradeoff between error due to signal dynamics and error due to noise. Then the resulting tracking errors were compared as a function of carrier-to-noise density ratio. The acquisition times for a frequency step input were also computed where acquisition time is defined to be the time required for the frequency error to decay to a preselected level.

Figure 26 shows the configuration of the loops under consideration, one being a standard Costas phase-locked loop and the other being a frequency locked loop with an I-Q discriminator. Both loops have nearly identical configurations, the only difference being that the error signal generated in the I-Q multiplier of the Costas loop is proportional to phase offset and the error signal in the frequency locked loop is proportional to frequency. The frequency discriminator can take several forms and these are discussed and analyzed in Appendix D. As indicated in the earlier

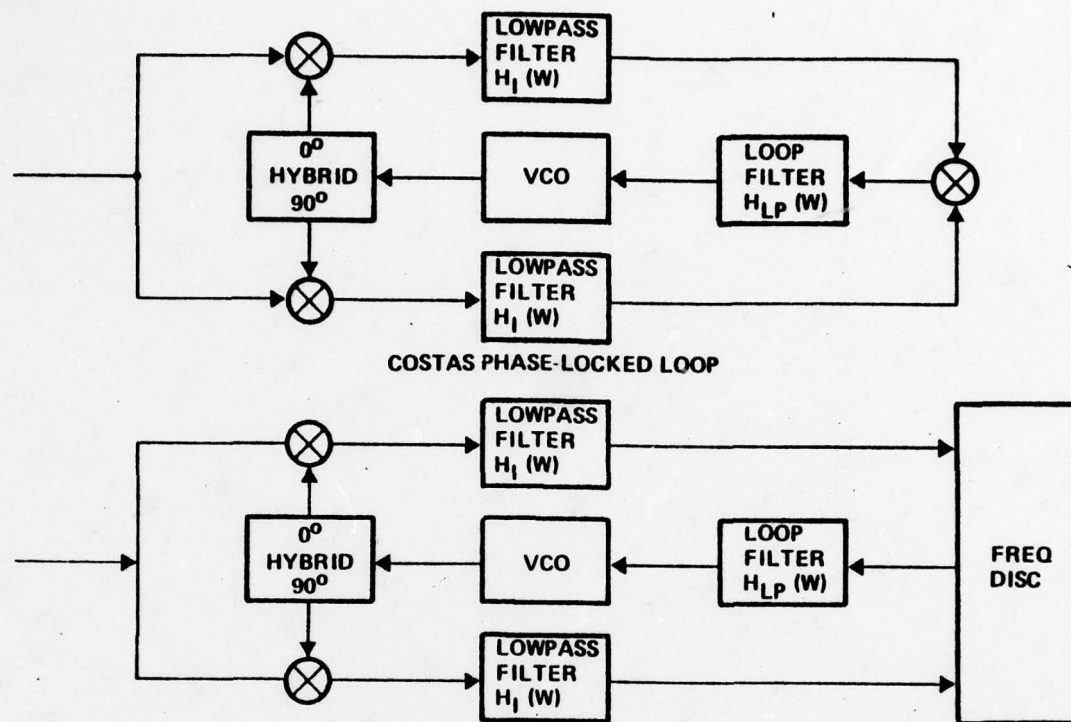


Figure 26. Tracking Loop Configurations

discussion on algorithms, the frequency discriminator will be formed by differencing the outputs of two filters offset in frequency resulting from a DTF processing of the input I-Q values.

A detailed analysis of the two types of loops is given in Appendix E. The key results are summarized here. Table 17 compares the tracking capability of the FLL versus the PLL. The steady-state error for the FLL is frequency error and phase error for the PLL. As the table indicates, for ideal filters, a PLL will provide the same tracking capability as a FLL having higher order. For example, a second-order PLL will track doppler acceleration, but a third-order FLL is necessary for the same signal dynamics.

Figure 27 is a plot of the "optimized" loop bandwidth versus carrier-to-noise density ratio for the FLL. The criterion of optimality is the sum of the error variance due to noise and the error variance due to signal

TABLE 17. EFFECTS OF SIGNAL DYNAMICS FLL VS PLL

HIGHEST ORDER EFFECT	LOOP FILTER		LOOP ORDER	STEADY STATE ERROR	
	FLL	PLL		FLL	PLL
DOPPLER OFFSET	$\frac{S+A}{S}$	1	1	0	CONSTANT
DOPPLER OFFSET	$\frac{S+A}{S^2}$	$\frac{S+A}{S}$	2	0	0
DOPPLER RATE	$\frac{S+A}{S}$	1	1	CONSTANT	INCREASING
DOPPLER RATE	$\frac{S+A}{S^2}$	$\frac{S+A}{S}$	2	0	CONSTANT
DOPPLER ACCELERATION	$\frac{S+A}{S^2}$	$\frac{S+A}{S}$	2	CONSTANT	INCREASING
DOPPLER ACCELERATION	$\frac{S+A}{S^3}$	$\frac{S+A}{S^2}$	3	0	CONSTANT

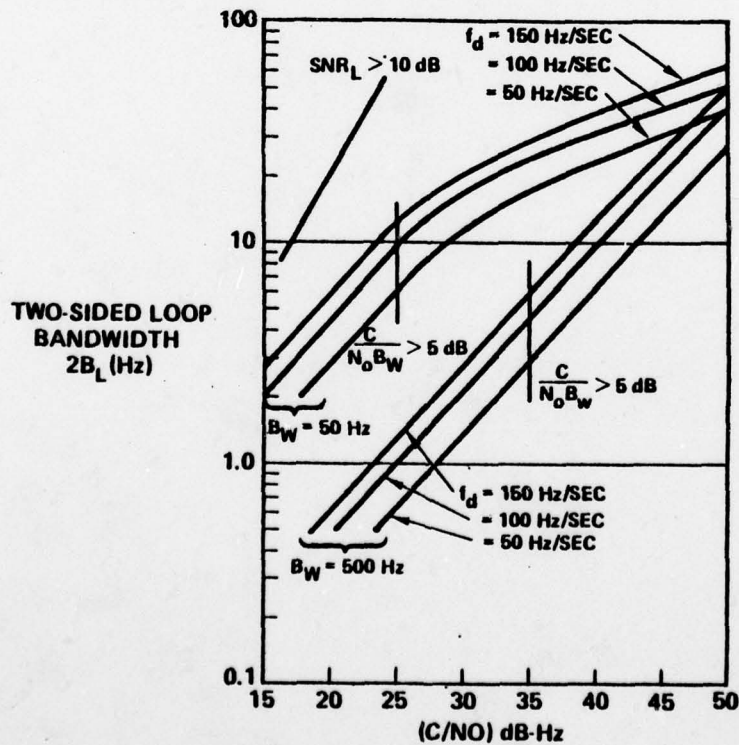


Figure 27. FLL Optimized Loop Bandwidth vs C/N_0

dynamics. The noise error variance increases as the loop error variance increases but the dynamic error variance decreases with increasing loop bandwidth. Thus there is an optimum choice of bandwidth. Two families of curves are shown as distinguished by different discriminator input bandwidths B_W . Within each family, the curves are parameterized by doppler rate f_d . For larger input bandwidths, the loop bandwidths must be smaller since the discriminator output signal-to-noise ratio is degraded. As the carrier-to-noise density ratio increases, the optimum loop bandwidth increases since noise is reduced. A similar situation holds as the doppler rate is increased. Note that for both families of curves, the loop signal-to-noise ratio is greater than 10 dB.

Figure 28 shows a similar set of curves for the Costas second-order loop. The same characteristics hold true here as in the previous case. In general, only those portions of the curves to the right of the line indicating the 10 dB loop signal-to-noise ratio are valid since loop behavior becomes nonlinear at some point below this. Figure 29 shows similar curves assuming third-order loops except that the curves are parameterized by doppler acceleration rather than doppler rate.

The RMS frequency errors for the second and third-order Costas loop and frequency locked loop are shown in Figures 30 and 31 assuming the optimum bandwidth is used at each point. In general, the FLL output performs the PLL at high carrier-to-noise density ratios. The third order loop appears to have somewhat better performance than the second-order loop. An RMS frequency error of less than 1 Hz is achievable for $C/N_0 > 30$ dB.

A key reason for considering the FLL is its improved performance relative to the Costas loop in acquisition time. Figure 32 shows a plot of acquisition time as a function of loop bandwidth for the FLL and PLL for different frequency offsets. For the PLL, two cases are considered, one in which the PLL is swept in frequency, and the other in which the PLL is allowed to acquire naturally. In almost all cases, the FLL provides faster acquisition times for the same loop bandwidth. The difference becomes increasingly larger as the loop bandwidth is made much smaller than the frequency offset.

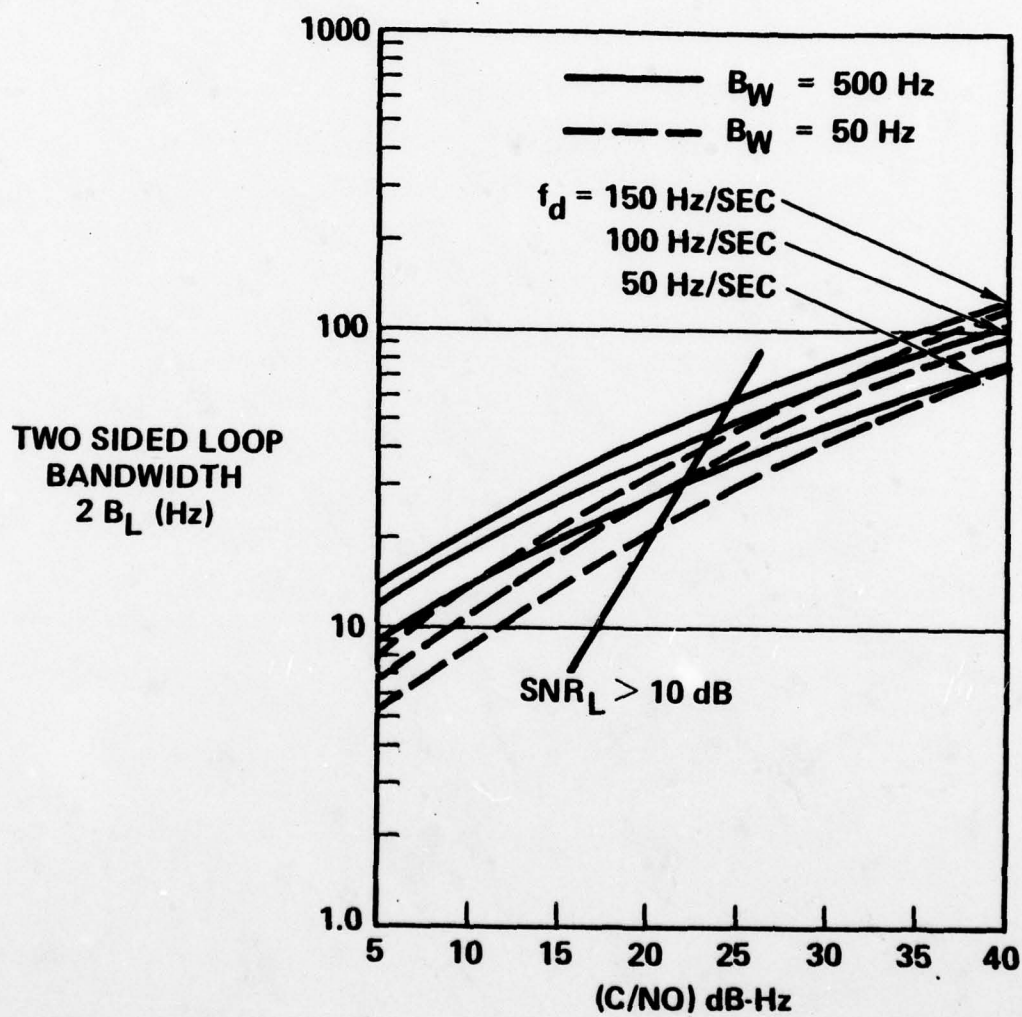


Figure 28. Optimized Second Order Costas Loop Bandwidth vs C/N₀

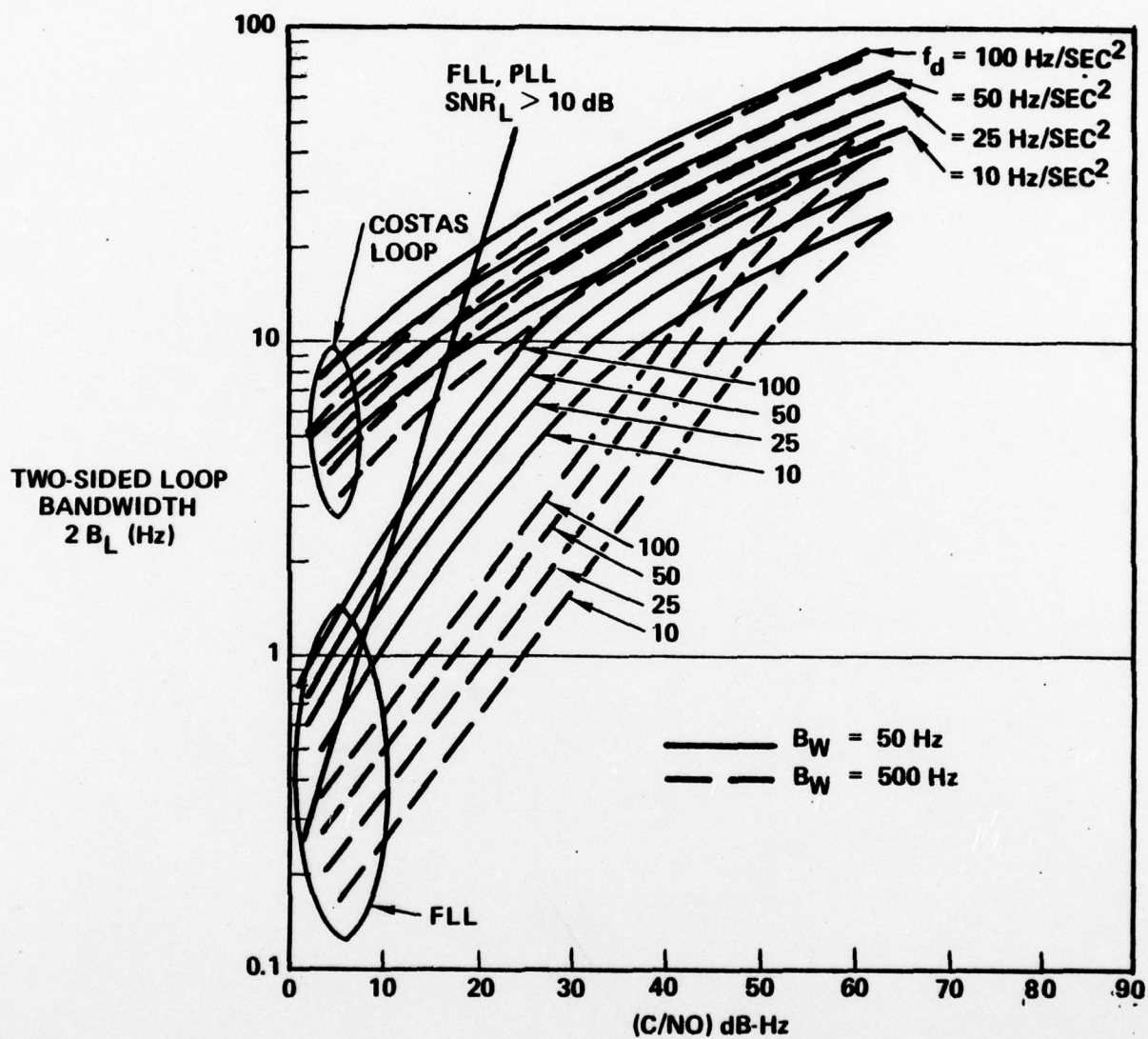


Figure 29. Optimized Loop Bandwidths for Third-Order Costas Loop and FLL

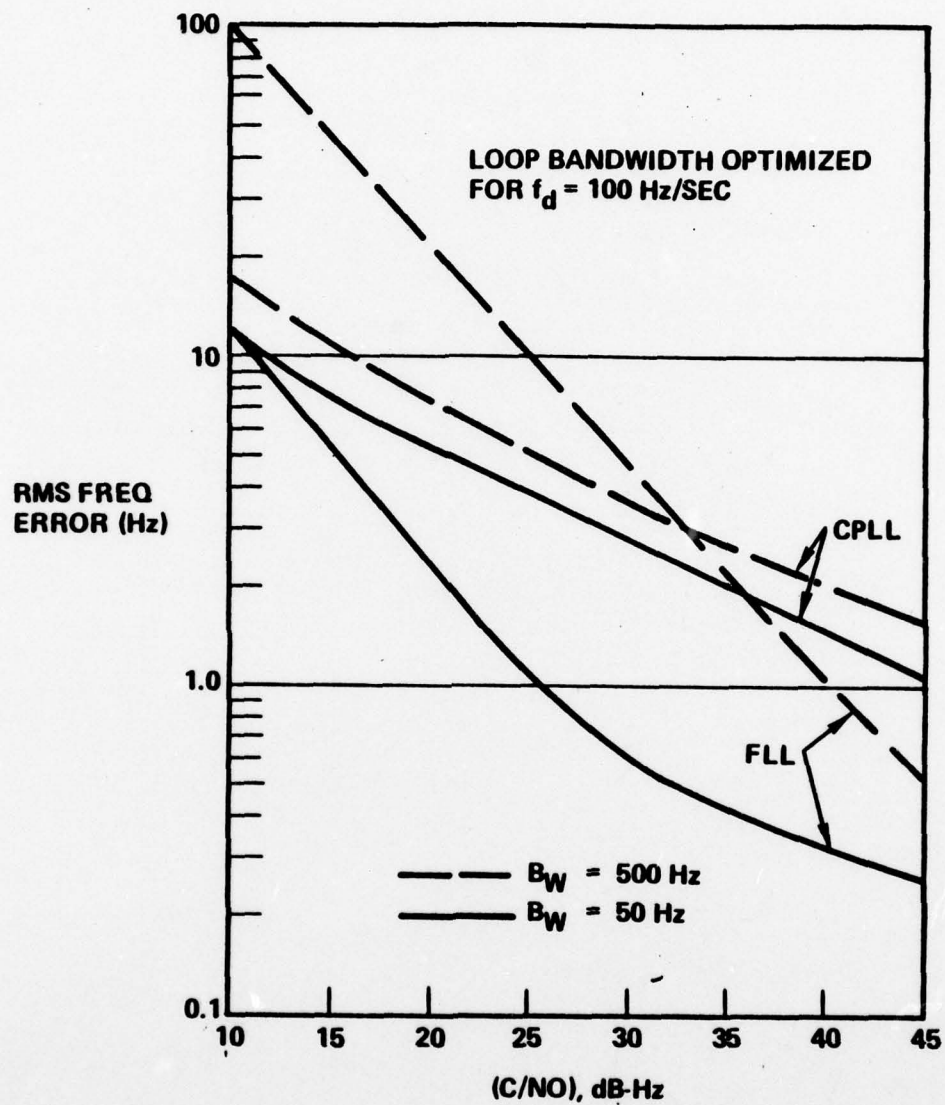


Figure 30. RMS Frequency Error for Second Order Costas Loop and Second Order IQFLL

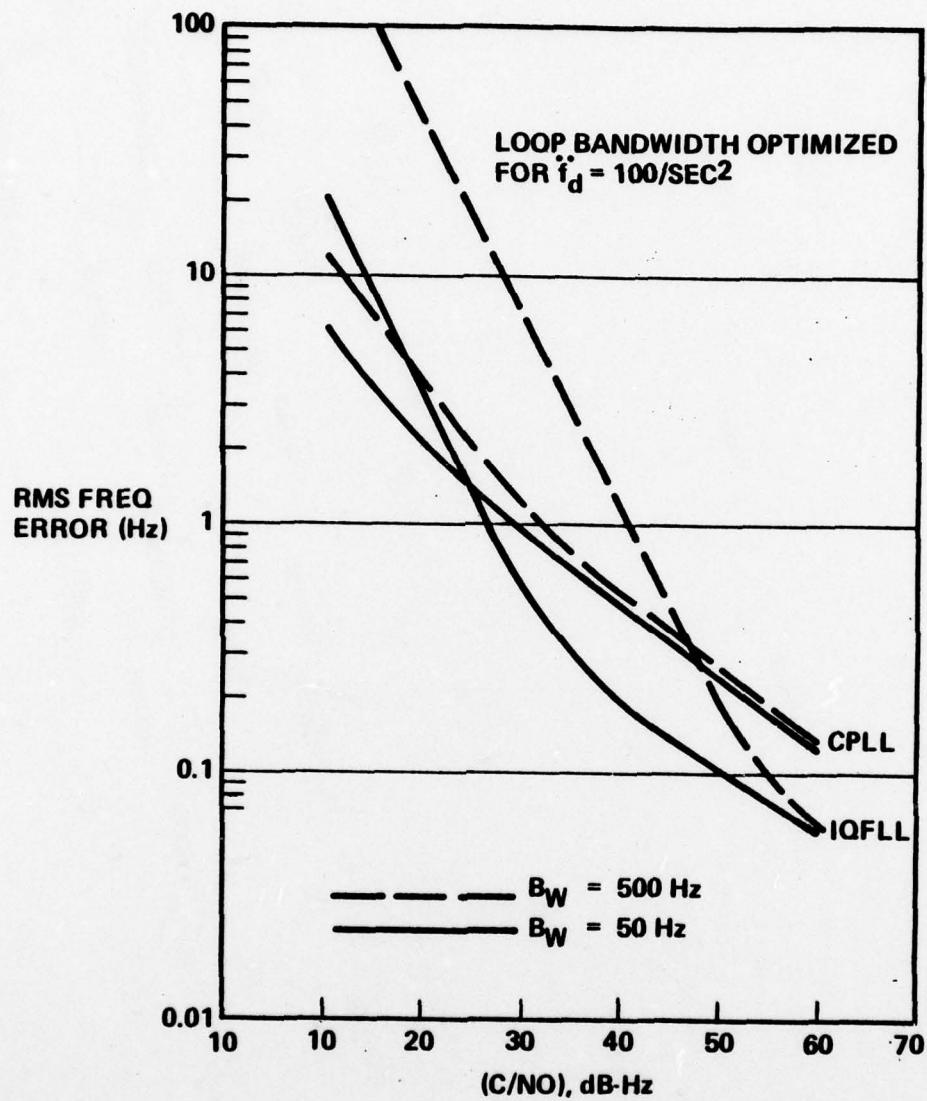


Figure 31. RMS Frequency Error for Third Order CPLL and Second Order IQFLL

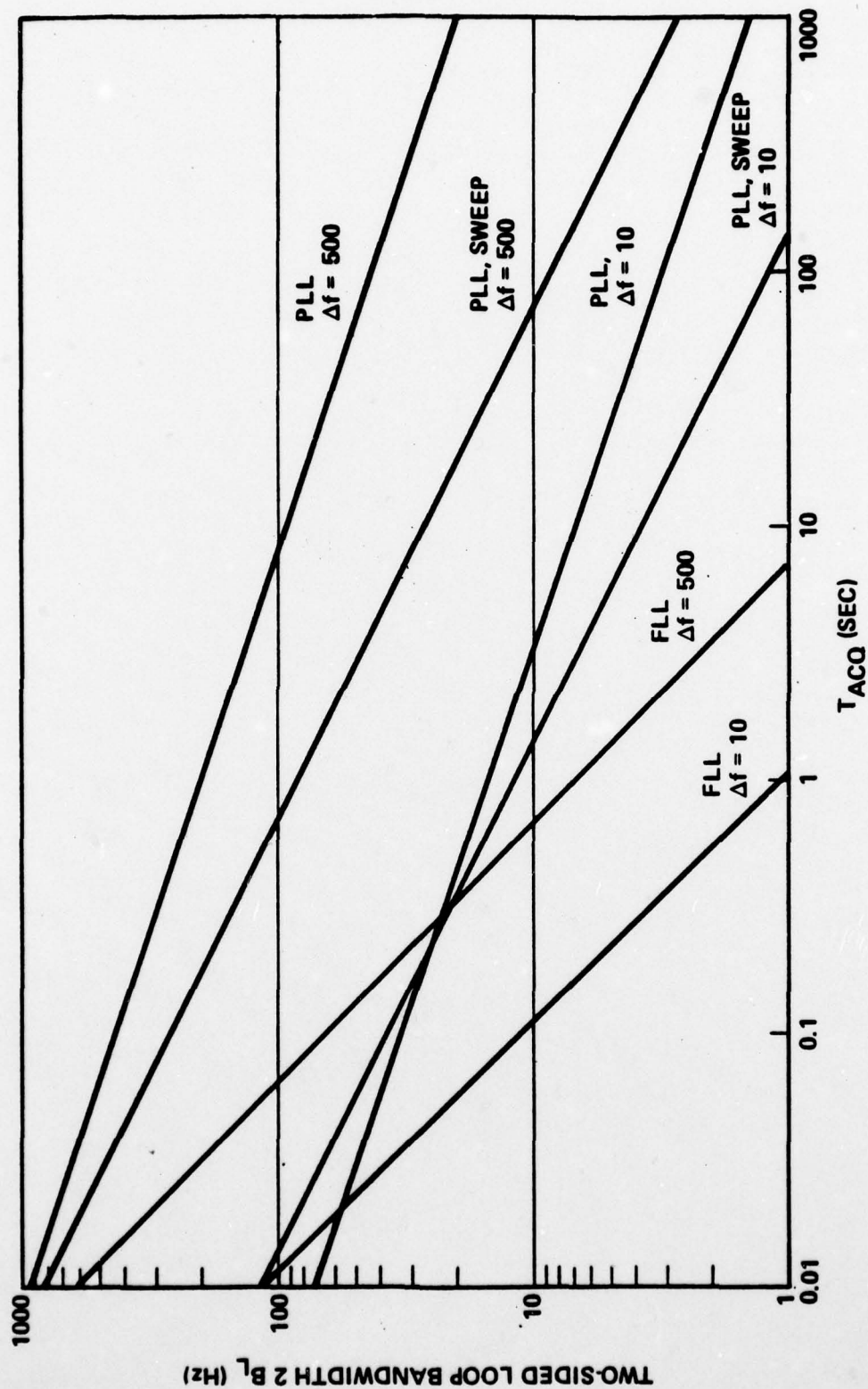


Figure 32. PLL vs FLL Acquisition Time

Figure 33 lists some general conclusions which can be drawn from this analysis. At high signal-to-noise ratios, the FLL exhibits superior performance. In general however, the PLL is to be preferred except for acquisition and tracking during extended range jerk conditions. Therefore, it appears that the FLL should be used for acquisition and the PLL for tracking. If loss of lock is indicated in the tracking mode, then the FLL should be reactivated. This operating philosophy is indicated in the signal processing algorithms described earlier.

2.5.4 Phase Tracking Loop Comparisons

Several configurations for phase tracking loops were analyzed and compared in terms of phase tracking performance. There were the Costas loop, I-Q loop and the decision feedback loop. Figure 34 shows the Costas loop and decision feedback loop. The I-Q loop is identical to the Costas loop except that the lowpass filters in the quadrature channels are replaced by integrate and dump filters. The I-Q loop therefore requires an estimate of bit timing. The decision feedback loop differs from the Costas loop in that a decision is made on the received data and this decision is used to determine the polarity of the error signal generated in the quadrature channel. In the Costas loop, a hard decision is not made, and instead a "soft" estimate of the modulation is used to modulate the error signal.

Figure 35 compares the phase tracking performance of the various loop as a function of signal-to-noise ratio. The curve marked PLL is the performance of an ideal phase-locked loop tracking an unmodulated carrier and therefore represents a lower bound on loop performance. In all cases, loop bandwidth is normalized at 1/10 the data rate. The family of curves for the Costas loop is parameterized by the cutoff frequency of the lowpass filters in the quadrature arms, assuming a simple RC configuration. As can be seen, cutoff frequencies ranging from 1 to 3 times the data rate result in approximately equivalent performances.

The curves show that both the decision feedback loop and the I-Q loop offer better performance than the Costas loop. At higher signal-to-noise ratios, performance is nearly equal to the ideal PLL. At lower signal-to-noise ratios the decision feedback loop degrades quickly due to the errors being made in the modulation estimate. However, over the range of interest, the decision feedback loop is the preferred approach, not only because of performance, but because of ease of implementation.

- FOR $\frac{C}{N_0} > 10 \cdot (\text{MAXIMUM FREQ UNCERTAINTY, Hz})$ THE FLL PROVIDES SUPERIOR PERFORMANCE BOTH IN TERMS OF TRACKING ABILITY AND ACQUISITION PERFORMANCE
- FOR $\frac{C}{N_0} < 10 \cdot (\text{MAXIMUM FREQ UNCERTAINTY, Hz})$ THE DUAL BANDWIDTH PLL IS SUPERIOR
- FOR A COHERENT SYSTEM OPERATING OVER A WIDE RANGE OF DOPPLER AND INPUT NOISE CONDITIONS A DUAL BANDWIDTH, SWEPT VCO PLL PROVIDES BETTER OVERALL PERFORMANCE THAN A FLL AIDED SYSTEM
- FOR A NONCOHERENT SYSTEM A FLL WOULD BE SUFFICIENT AND DESIRABLE IN TERMS OF SIMPLICITY
- FOR ACQUISITION DURING EXTENDED RANGE JERK CONDITIONS A FLL SHOULD BE USED

Figure 33. Conclusions

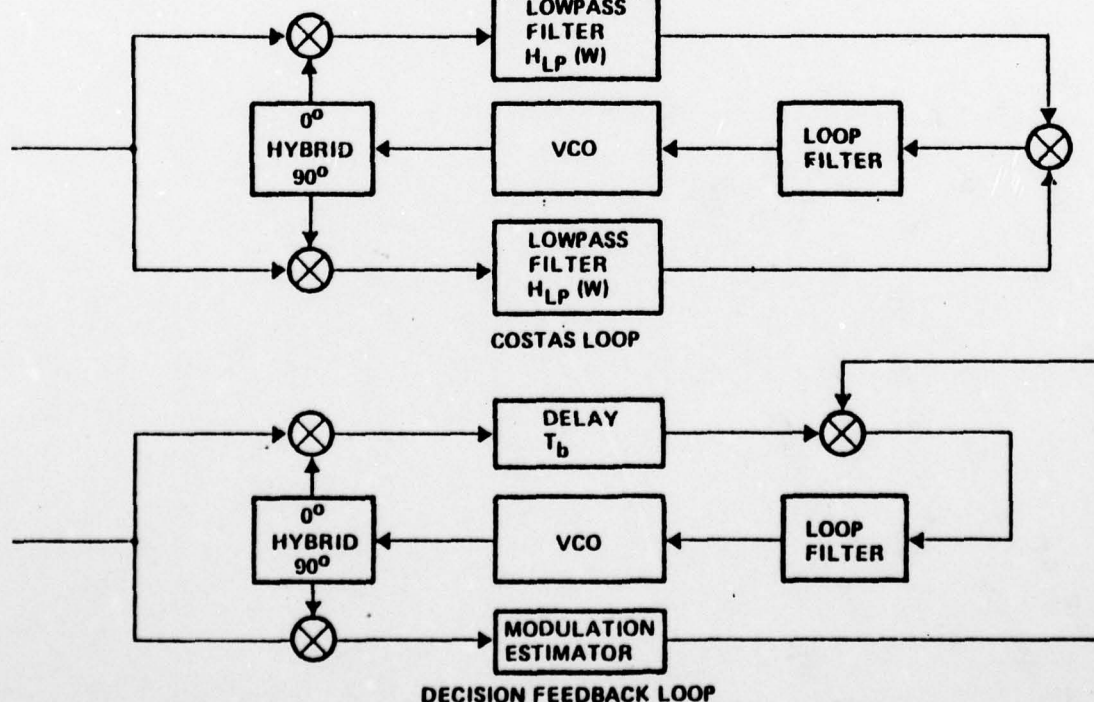


Figure 34. Bi-Phase Tracking Loop Configurations

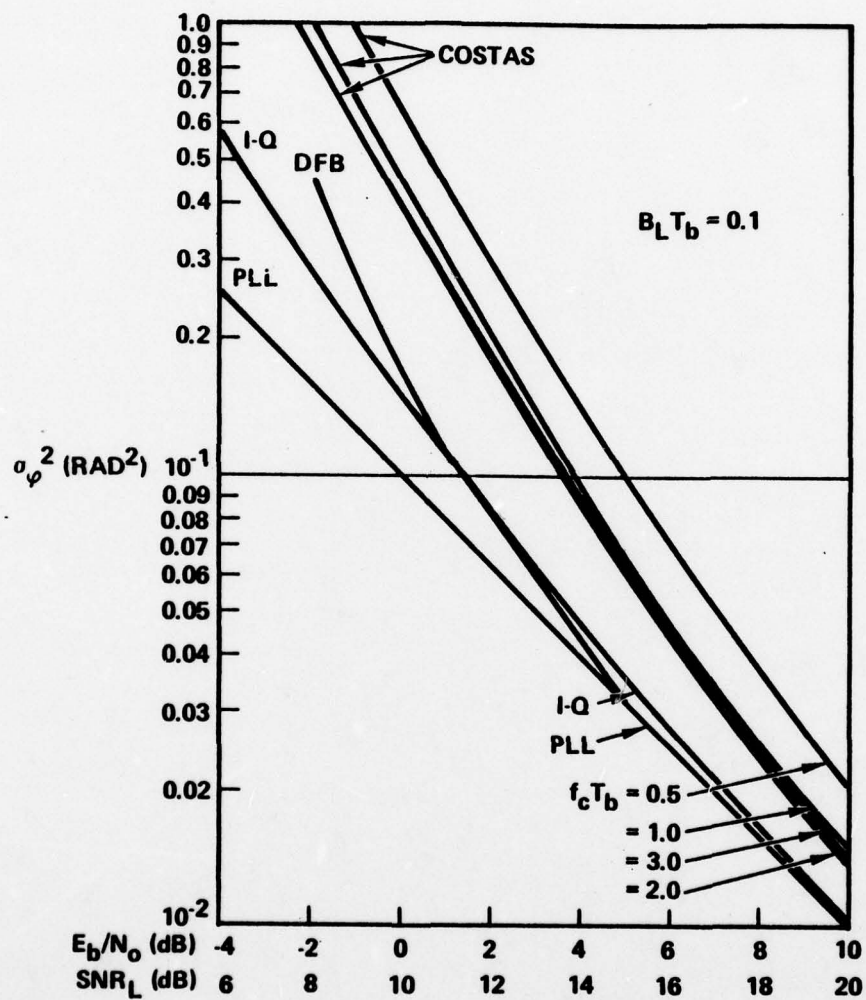


Figure 35. Bi-Phase Tracking Loop Comparison Phase Error Variance Versus Signal-to-Noise Ratio

The difference between the loop configurations become more apparent when they are modified to track signals which are quad-phase modulated. Figure 36 shows the 4-phase Costas loop. Four downconverters and filters are required along with a multiplier capable of handling four inputs. Figure 37 shows the 4-phase decision feedback loop. Note that the increase in complexity over a bi-phase loop is minimal. Basically, an additional modulation estimator and binary multiplier are required. The modulation estimator is simply an integrate and dump function followed by a threshold comparator. The additional downconversions are required. In terms of performance, the decision feedback loop exhibits superior performance over the other configurations as indicated in Figure 38.

2.5.5 Noncoherent Delay Locked Loop

The noncoherent delay locked loop shown in Figure 39 provides tracking of the PN code timing variations. The error signal is formed by taking the difference in magnitude between a $1/2$ chip early correlation and a $1/2$ chip late correlation. The error signal is filtered in the loop filter and the result controls the clock which drives the reference code generator.

Selection of the loop bandwidth for the delay locked loop involves considerations similar to those used in phase-locked loop analysis. The error due to signal dynamics is inversely proportional to loop bandwidth. The tracking error due to noise is directly proportional to the square root of loop bandwidth. An "optimum" bandwidth can be determined by setting the dynamic error equal to the RMS error due to noise. The result is shown in Figure 40 where loop bandwidth is plotted versus carrier-to-noise density ratio. The curves are parametrized by k , the code doppler. Using these bandwidths, the RMS tracking error, σ , (or dynamic error, ϵ) can be calculated and is shown in Figure 41. The error is normalized to the chip length, Δ . An acceptable level of performance is achieved when the RMS error is less than $1/10$ of a chip.

2.5.6 Algorithm Performance Simulation

The frequency and phase tracking algorithms described previously were simulated in order to demonstrate their validity and assess their performance. Some examples of the results obtained are shown in the following figures.

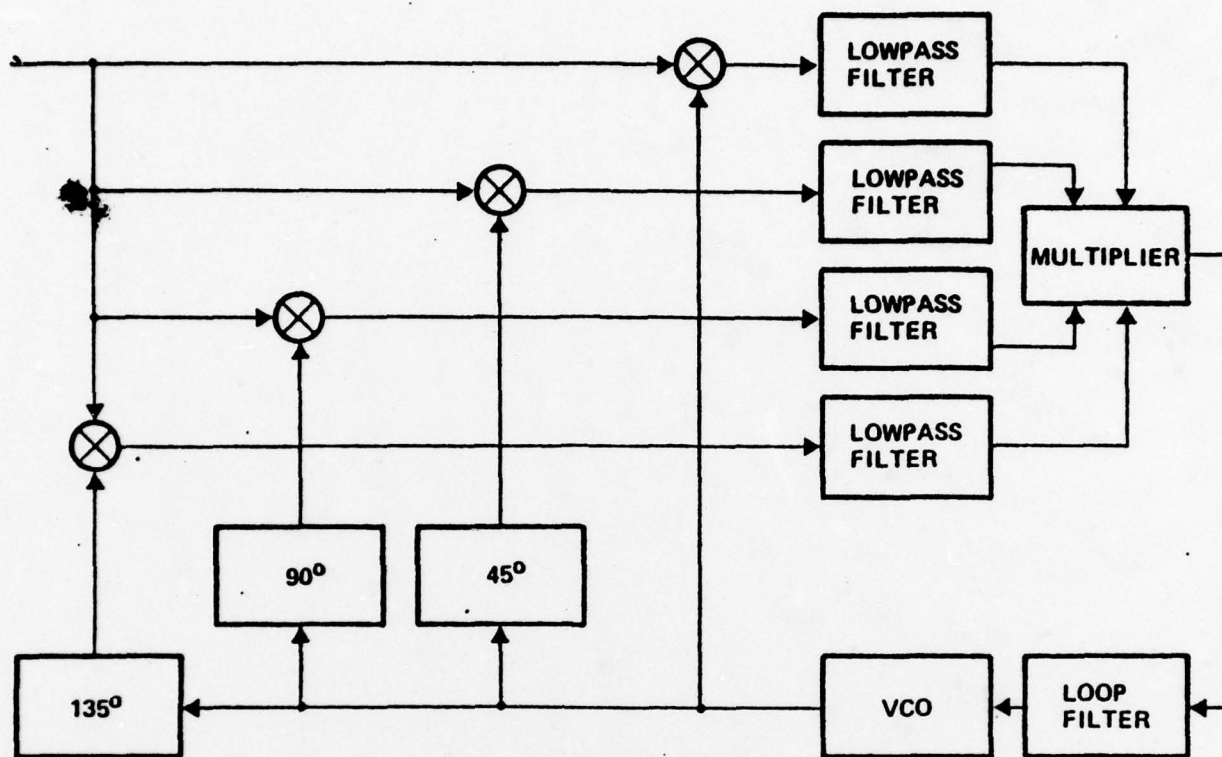


Figure 36. 4-Phase Costas Loop

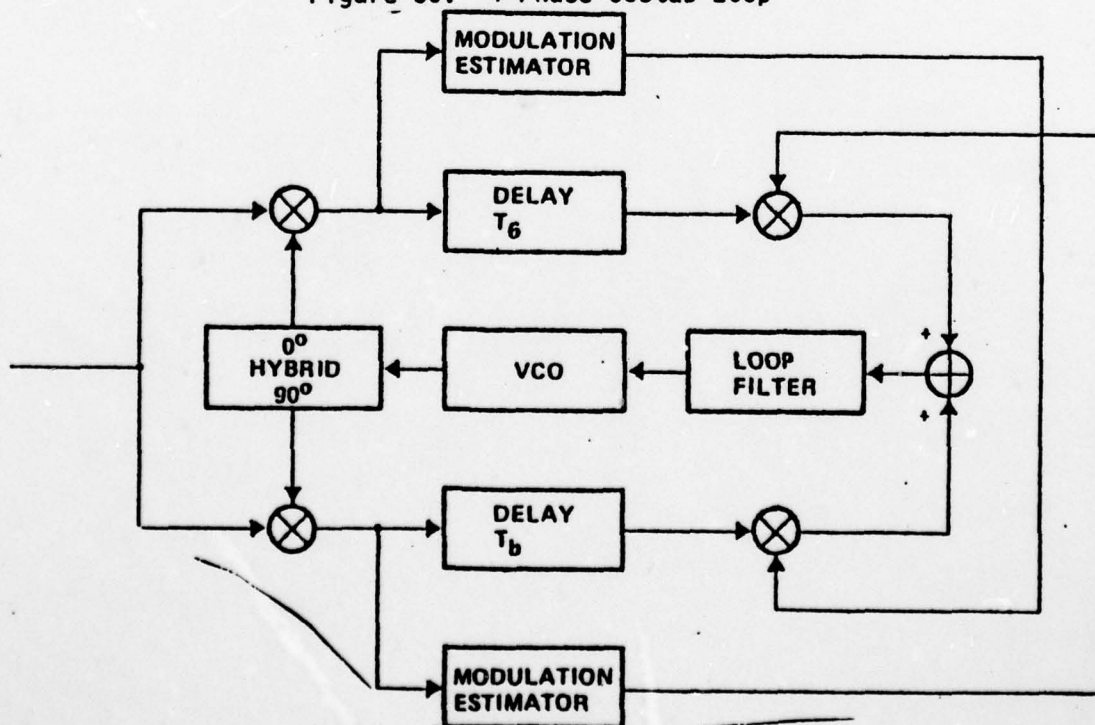


Figure 37. 4-Phase Decision Feedback Loop

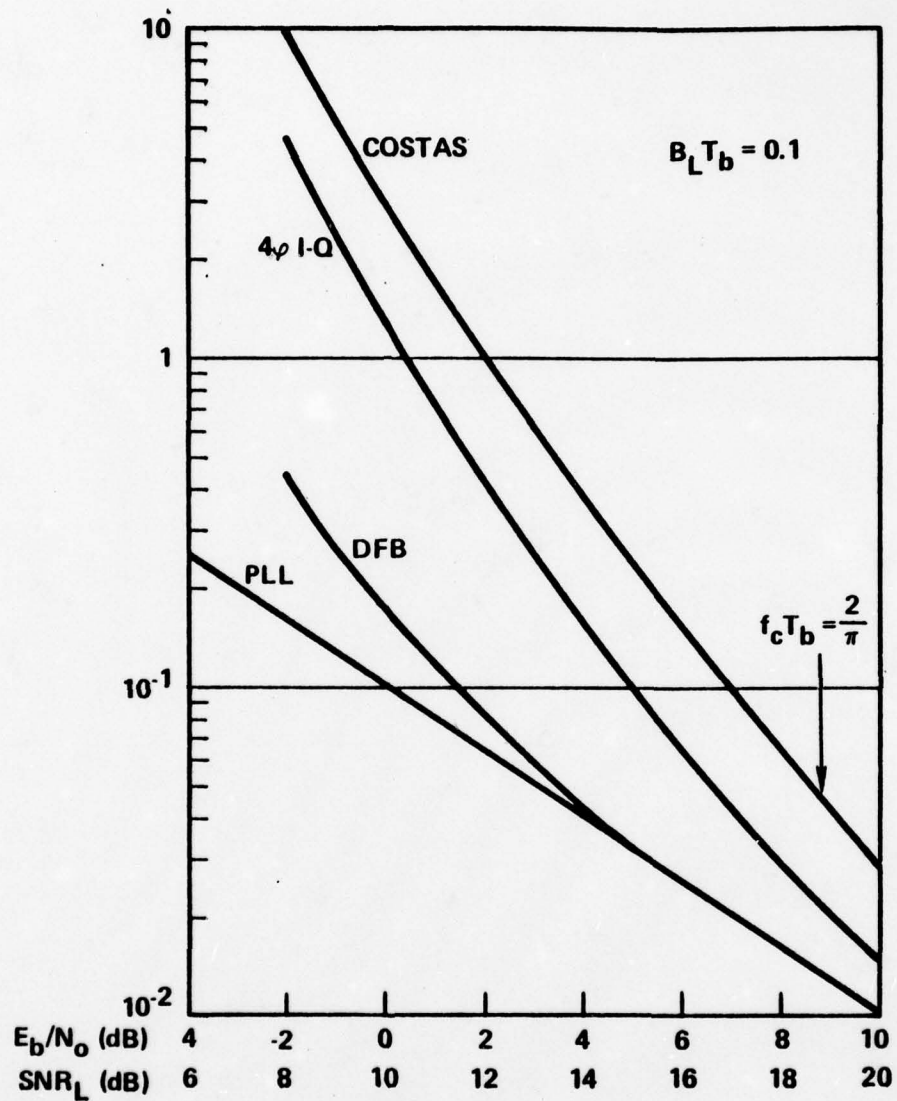


Figure 38. Quad-Phase Tracking Loop Comparison Phase Error Variance vs Signal-to-Noise Ratio

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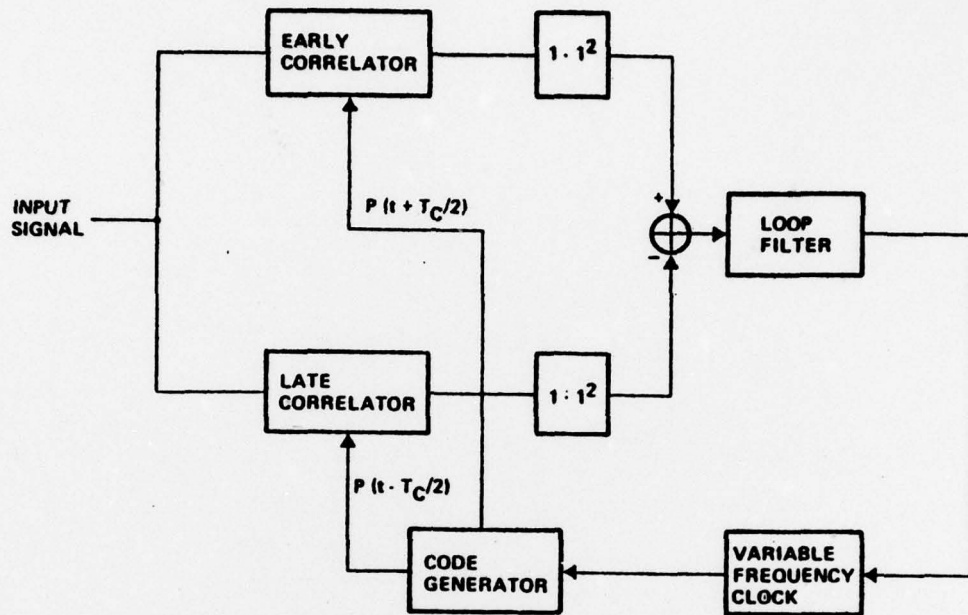


Figure 39. Noncoherent Delay Locked Loop

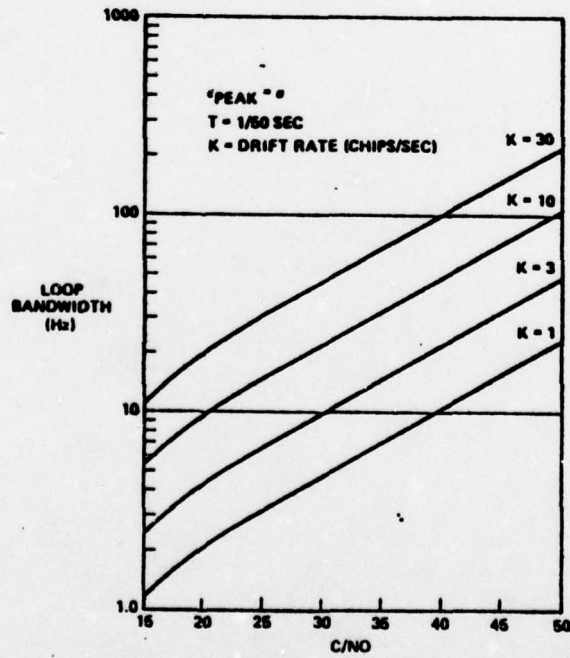


Figure 40. Delay Lock Loop Bandwidth

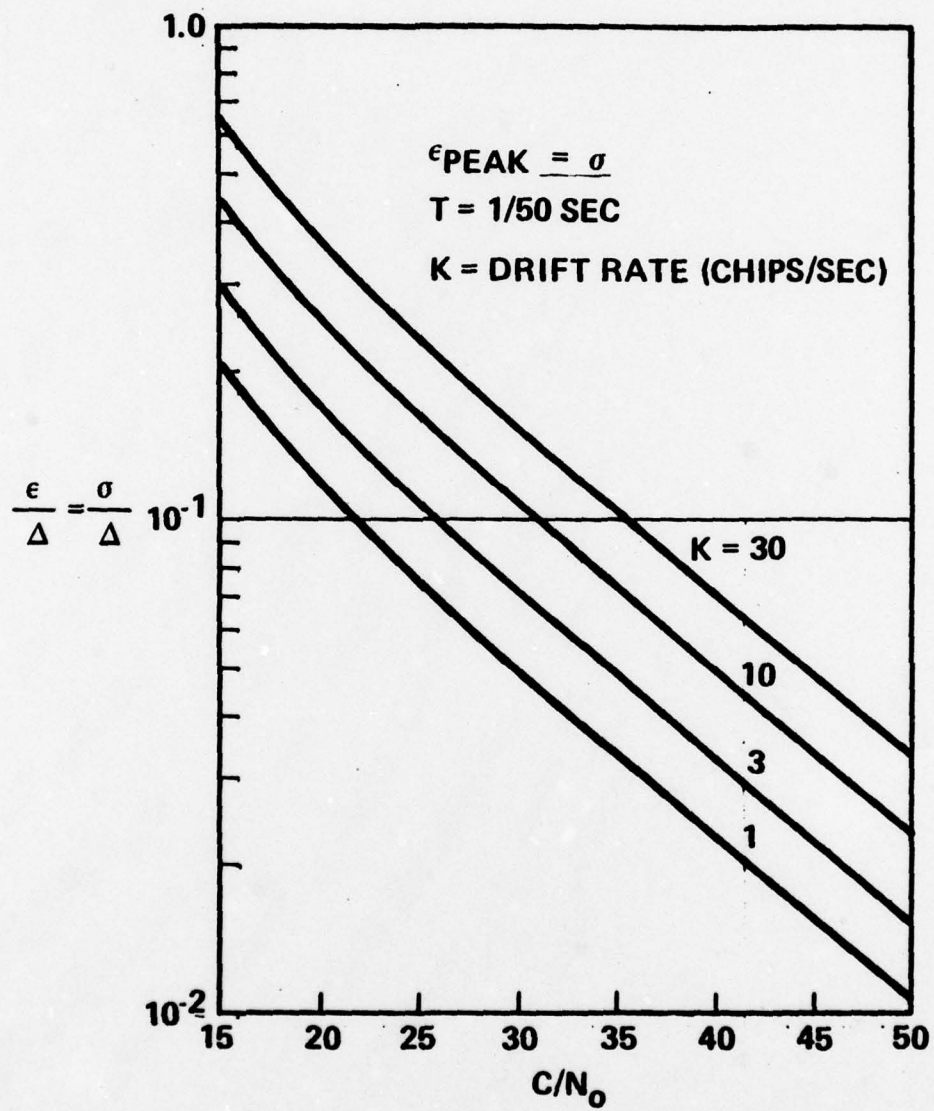


Figure 41. Delay Locked Loop Tracking Performance

Figures 42 and 43 show the frequency and phase tracking capability of the second-order FLL and PLL at high signal-to-noise ratio ($C/N_0 = 80$ dB-Hz). The mode notations at the bottom of the figures refer to the modes identified in the description of the algorithm. In mode 1, the FLL is operated with a wide loop bandwidth for fast acquisition. In mode 2 the bandwidth is reduced and in mode 3 both the FLL and PLL are operating simultaneously. The input signal has an initial frequency offset of 500 Hz with a frequency ramp of 100 Hz/sec and a frequency jerk of 50 Hz/sec².

Figures 44 and 45 show the simulation results at a lower signal-to-noise ratio ($C/N_0 = 30$ dB - Hz). Again the identical frequency offset is 500 Hz with a frequency ramp of 100 Hz/sec. As expected, the tracking accuracy is degraded, but the loops are capable of maintaining lock. The bit error rate was measured during mode 3 and found to be less than 10^{-3} . Figures 46 and 47 show the same curves except that the input signal dynamics included a frequency jerk component of 50 Hz/sec². Again the loops maintained lock and the measured bit error rate was less than 10^{-3} .

The purpose of this simulation effort was to validate the tracking algorithms and to examine the feasibility of operating the loops with variable bandwidths. It was also of interest to know the effect of operating both a FLL and PLL simultaneously. The proposed concepts appear workable based on the simulation results and provide the expected capability. For example, the second-order PLL was capable of tracking a frequency jerk when aided by a FLL. Theoretically, the second-order PLL alone cannot track a frequency jerk. The loop parameters were not necessarily optimized for these simulations so that some variations in the actual loop performance are to be expected. However, the gross capabilities should be as depicted here.

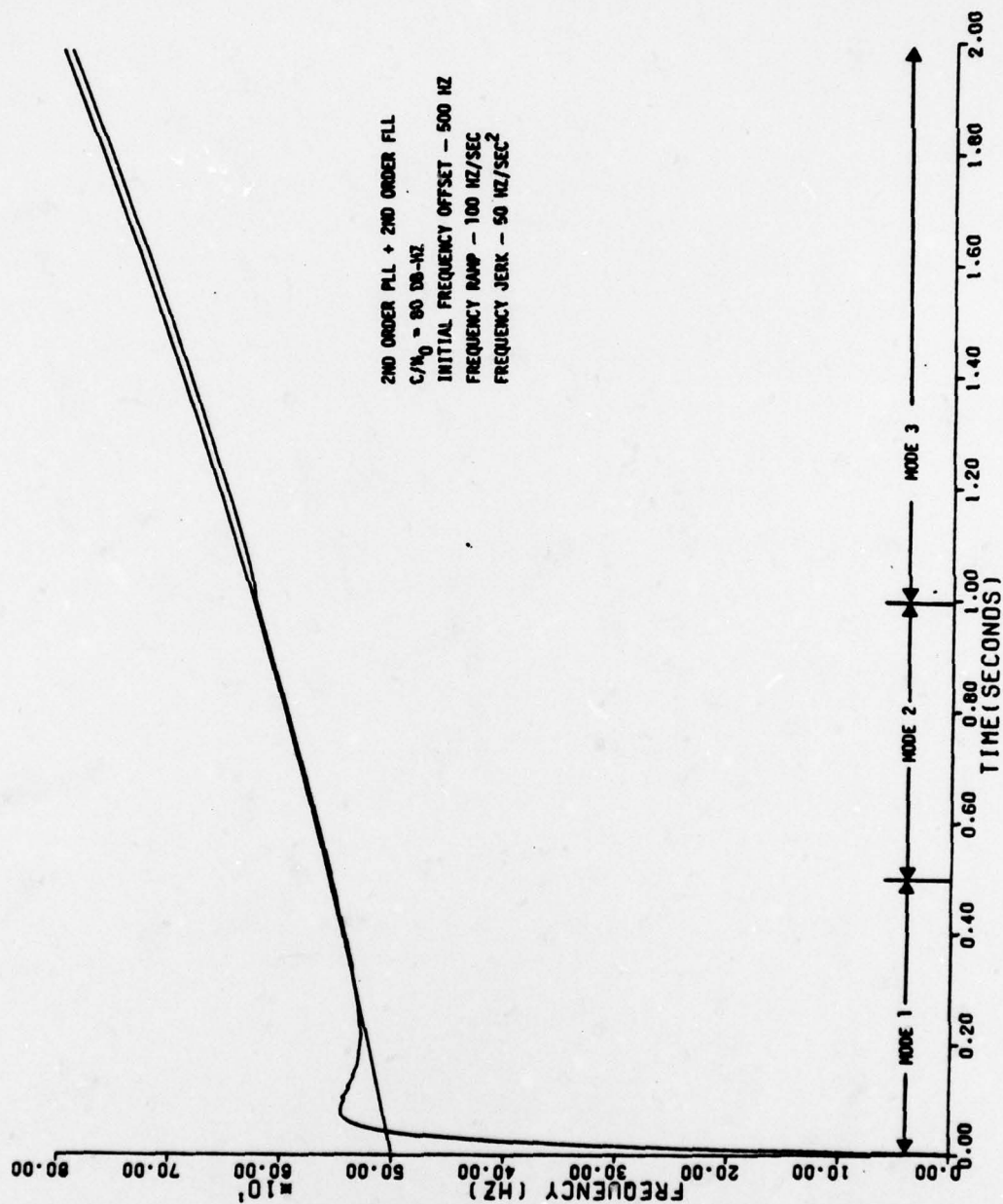


Figure 42. Frequency Tracking ($C/N_0 = 80 \text{ dB-Hz}$)

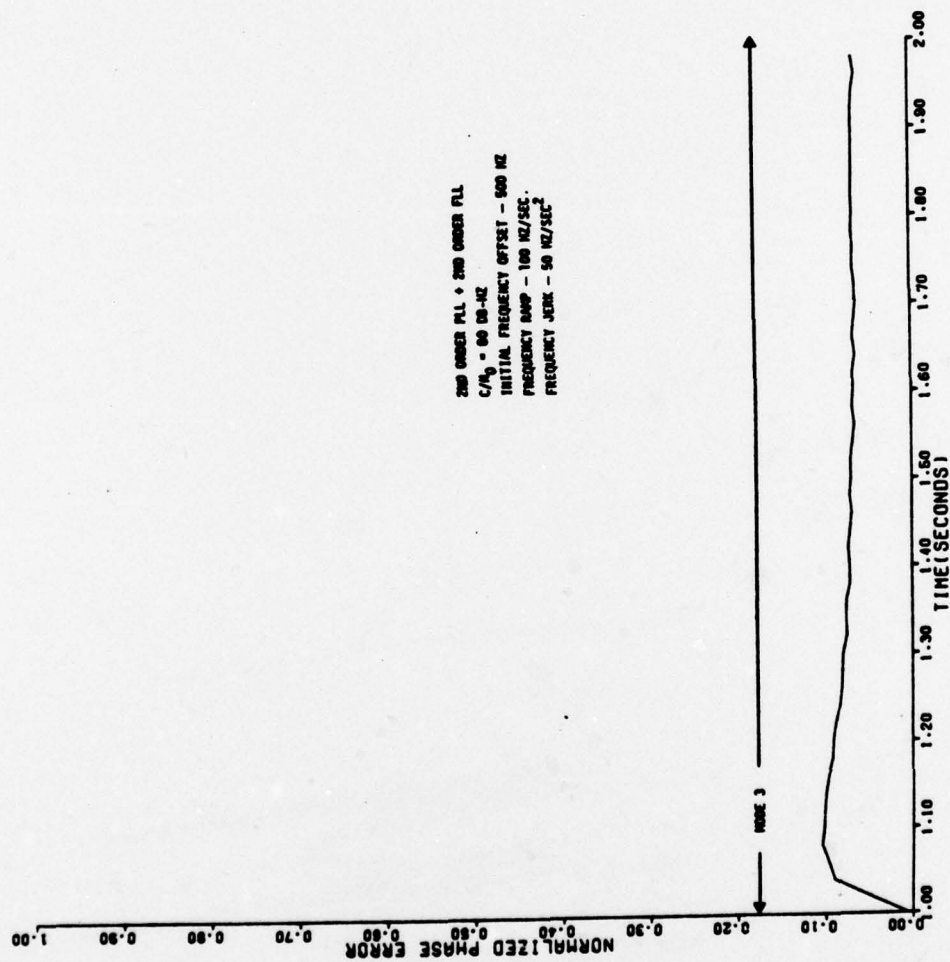


Figure 43. Phase Tracking

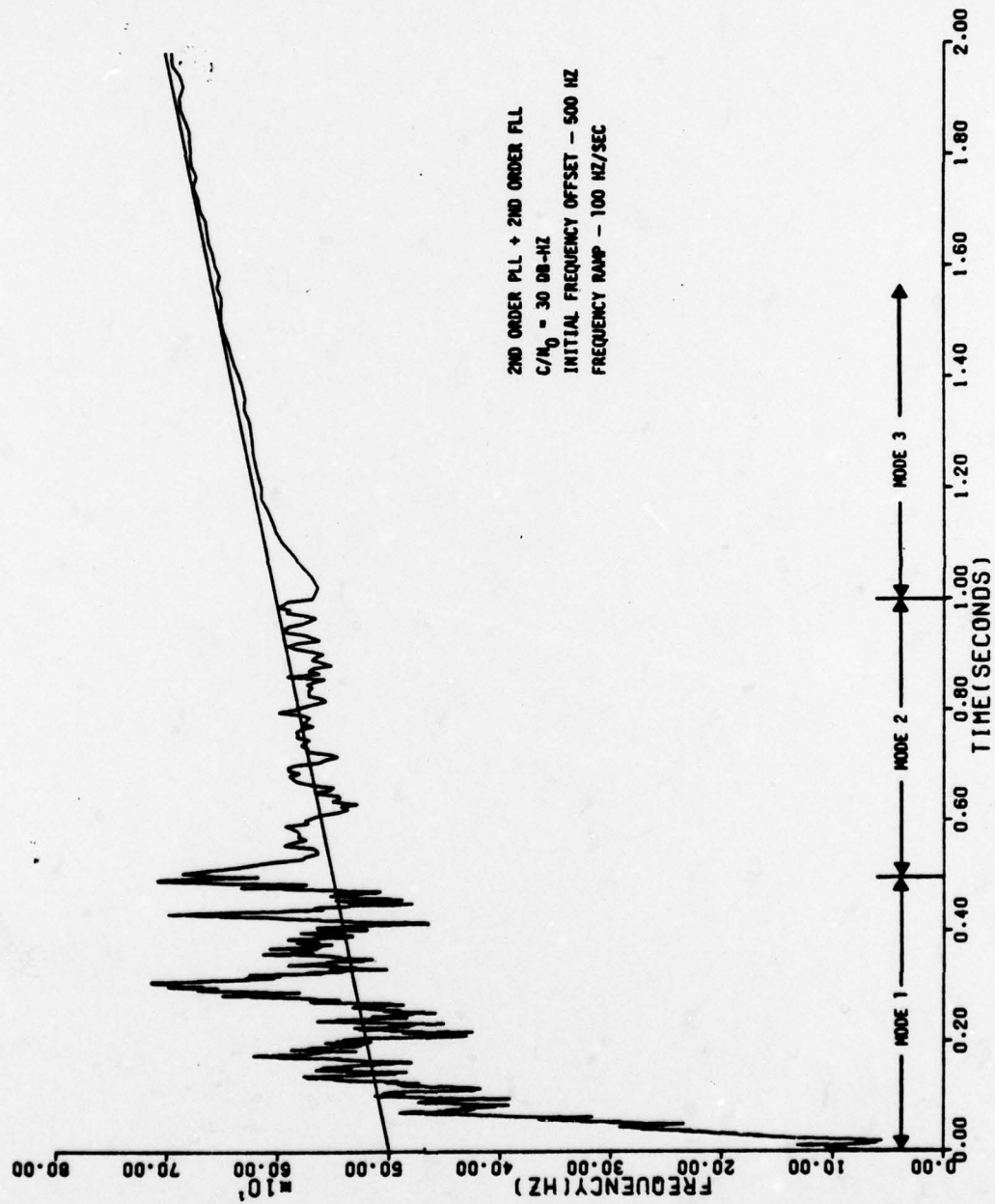


Figure 44. Frequency Tracking

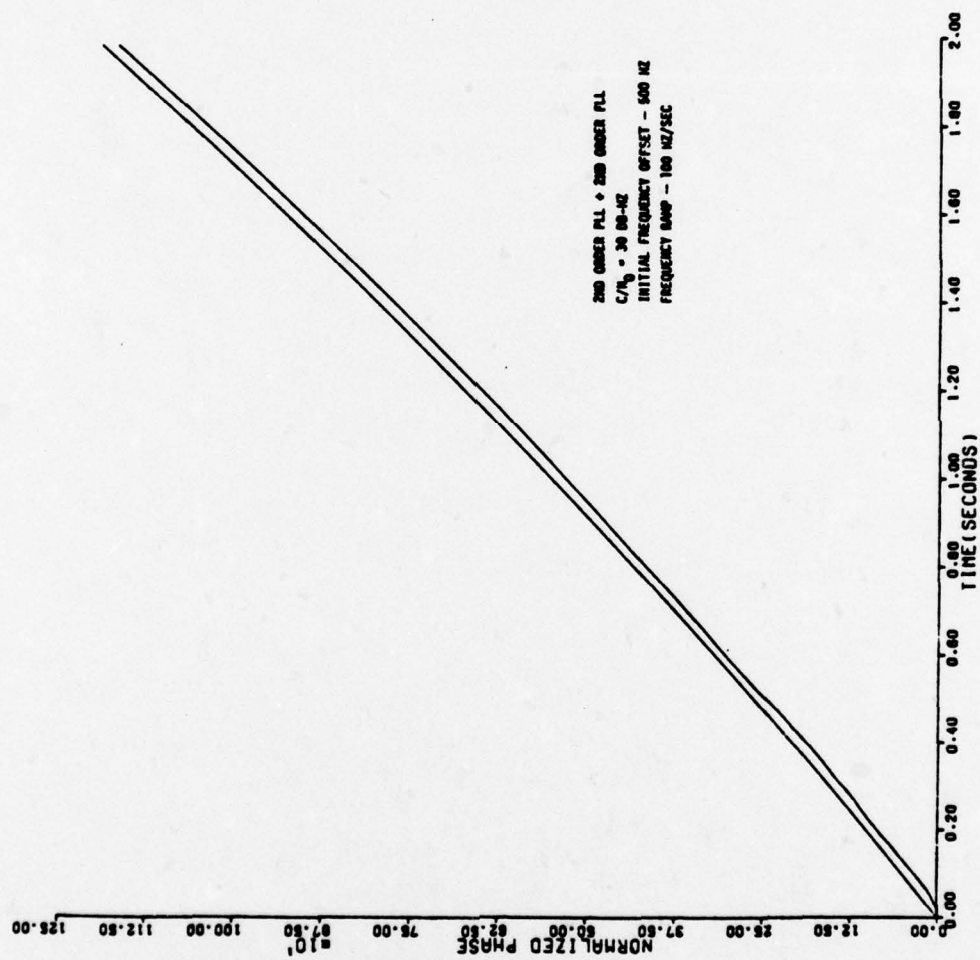


Figure 45. Frequency Tracking ($C/N_0 = 30 \text{ dB-Hz}$)

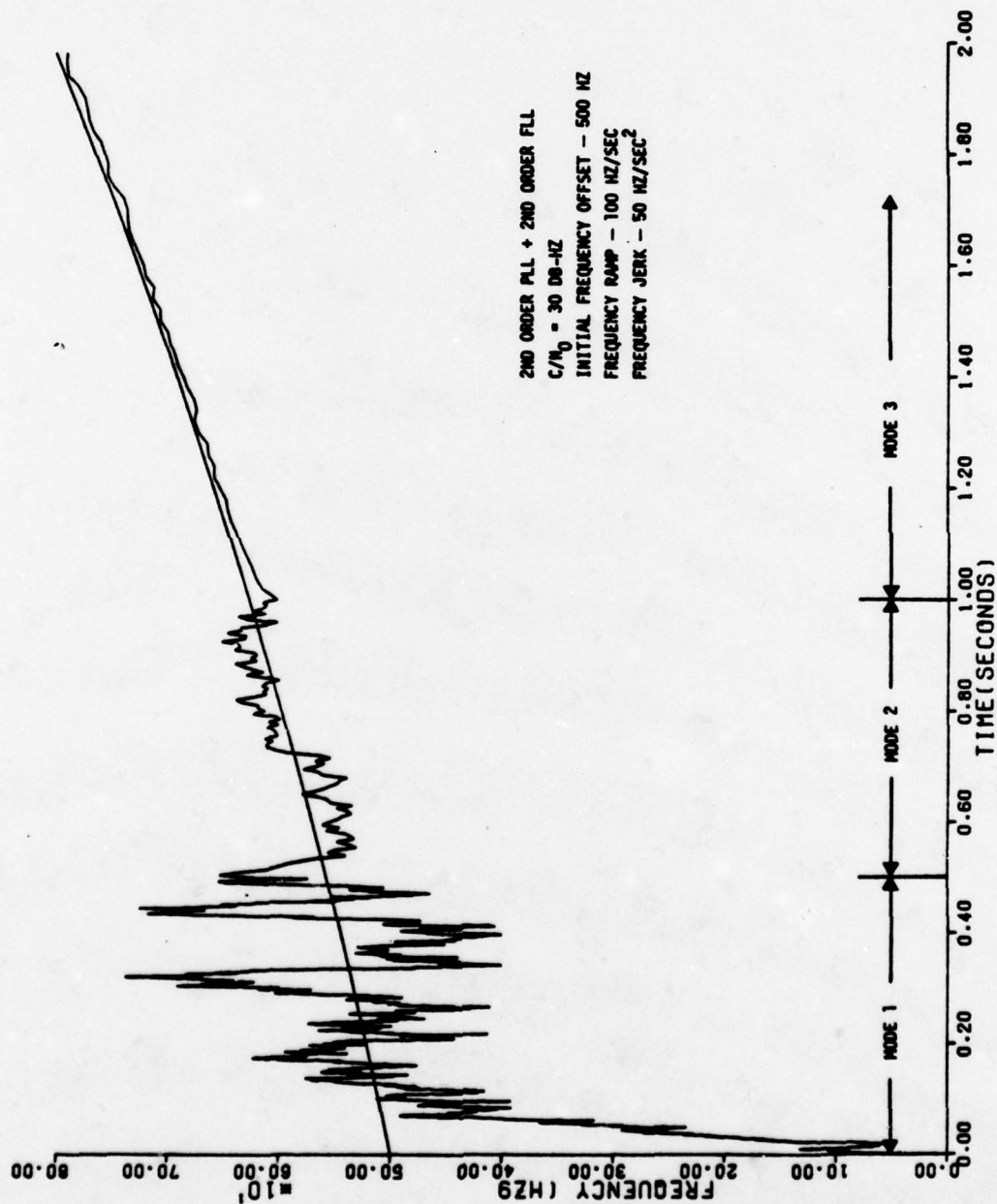


Figure 46. Frequency Tracking

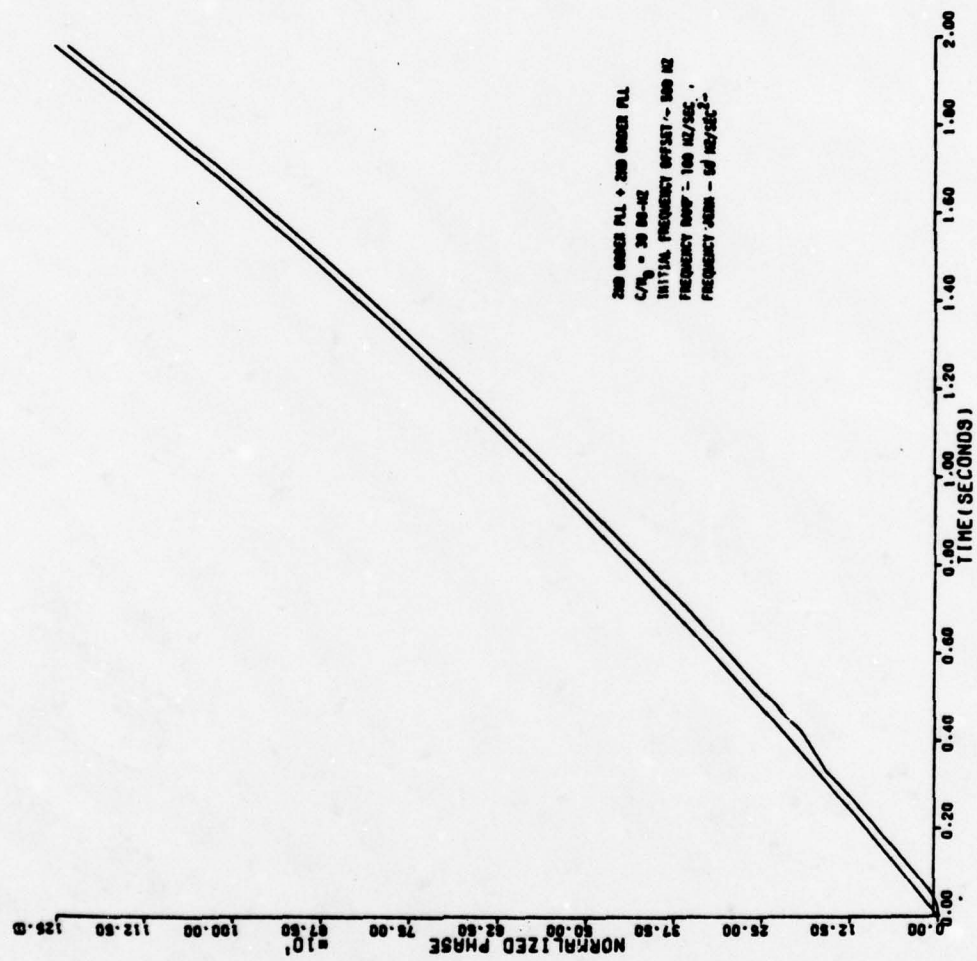


Figure 47. Phase Tracking

SECTION III SYSTEM DESIGN AND DEVELOPMENT

3.1 Introduction

The architecture of the SAM terminal is designed for flexibility and functional commonality in accommodating a variety of waveform processing requirements. Modular and common functions are emphasized especially in modem (modulator/demodulator) as RF front-ends are similar and digital computers at the other side are definitely general purpose. The more common functions imbedded in different terminals, such as GPS and JTIDS, the lower the acquisition costs through reduced design and development and a lower life cycle cost should result as fewer spares are necessary.

Inherent flexibility in meeting the different terminal requirements is a function of the degree digital processing is used. Digital processing offers the distinct advantages of being very stable and capable of being programmed, generally through firmware, to handle different waveform formats and data rates. A major element here is the use of a high-speed bipolar microprocessor based on the AMD 2901A central processing unit (CPU) chip. Its function encompasses most of the digital signal processing algorithms for acquisition, tracking and data demodulation. The microprocessor or the micro-signal-processor (MSP) has the advantage of versatility and ease of modification through firmware reprogramming. The MSP is very effective when processing multiple algorithms simultaneously as a centralized unit. Less hardware is required than if each algorithm had a dedicated processor.

In general, the SAM architecture was chosen to be compatible with a general class of waveforms; as such it was not tailored to any specific waveform structure or parameter. The generic PSK, GPS and JTIDS waveforms were considered representative of the general class of spread-spectrum waveforms, either of the direct-sequence or frequency hop/PN type. The terminal partitioning, spanning the above waveforms, into modules was based on functional characteristics rather than a physical basis. The modules, as defined, are a complete signal processing function and are capable of being used in a variety of different situations. Many modules are identified as being common functions within practically all spread-spectrum modems, thereby enhancing their use.

3.2 SAM Modules Detailed Descriptions

The SAM terminal, herein labeled SAM modem, has been partitioned into eleven modules and a test set. The eleven modules represents six standard or common modules, and five waveform unique modules. Commonality is basically a compromise between special purpose and general purpose processing and, due to constraints such as iterative high data rates or specialized functions such as PN sequences, unique modules are required. Refer to Figure 48. All of the modem modules and the three letter designators are listed in Table 18.

The modem interface is at a standard 70 MHz IF. The modulator (MOD) performs quadri-phase modulation of the 70 MHz intermediate frequency with in-phase and quadrature digital data inputs. The digital data is generated in the modem adapter (MAD). The input data is then combined with a PN code prior to being mixed with the quadrature frequencies. The PN code is provided by the transmit PN generator (TPN) which can be synthonized with the receive PN generator (GPN). A separate frequency generator is provided for the modulator for test purposes such as PN and 70 MHz offsets.

The simulated received 70 MHz IF signal at the demodulator, is first processed in the IF amplifier (IFA) which provides gain, gain control, and bandlimiting of the signal. The next function, the quadrature A-to-D converter (ADC), downconverters the I and Q baseband components. The signals are then sampled and quantized to two bits in the ADC. The IFA AGC control signal is derived from the signal energy of the I and Q channels. The down-conversion local oscillator, the doppler wipe-off (DWO) module, is a commandable digital frequency synthesizer. The synthesizer allows frequency coarse-tuning or frequency and phase tracking, and is controlled by the micro-signal-processor (MSP). The MSP generates the control signals (phase error) as an output from the firmware tracking algorithms.

The quantized signals are then processed by the digital correlator module (COR) which operates as a matched filter. The number of correlator modules required depends on the specific application such as GPS requiring four modules. The COR module uses a cascable bipolar LSI 32-bit digital correlator chip that has a digital output. The clock rate is in excess of 100 Msps while dissipating 400 to 500 mw and uses a 16-PIN DIP integrated

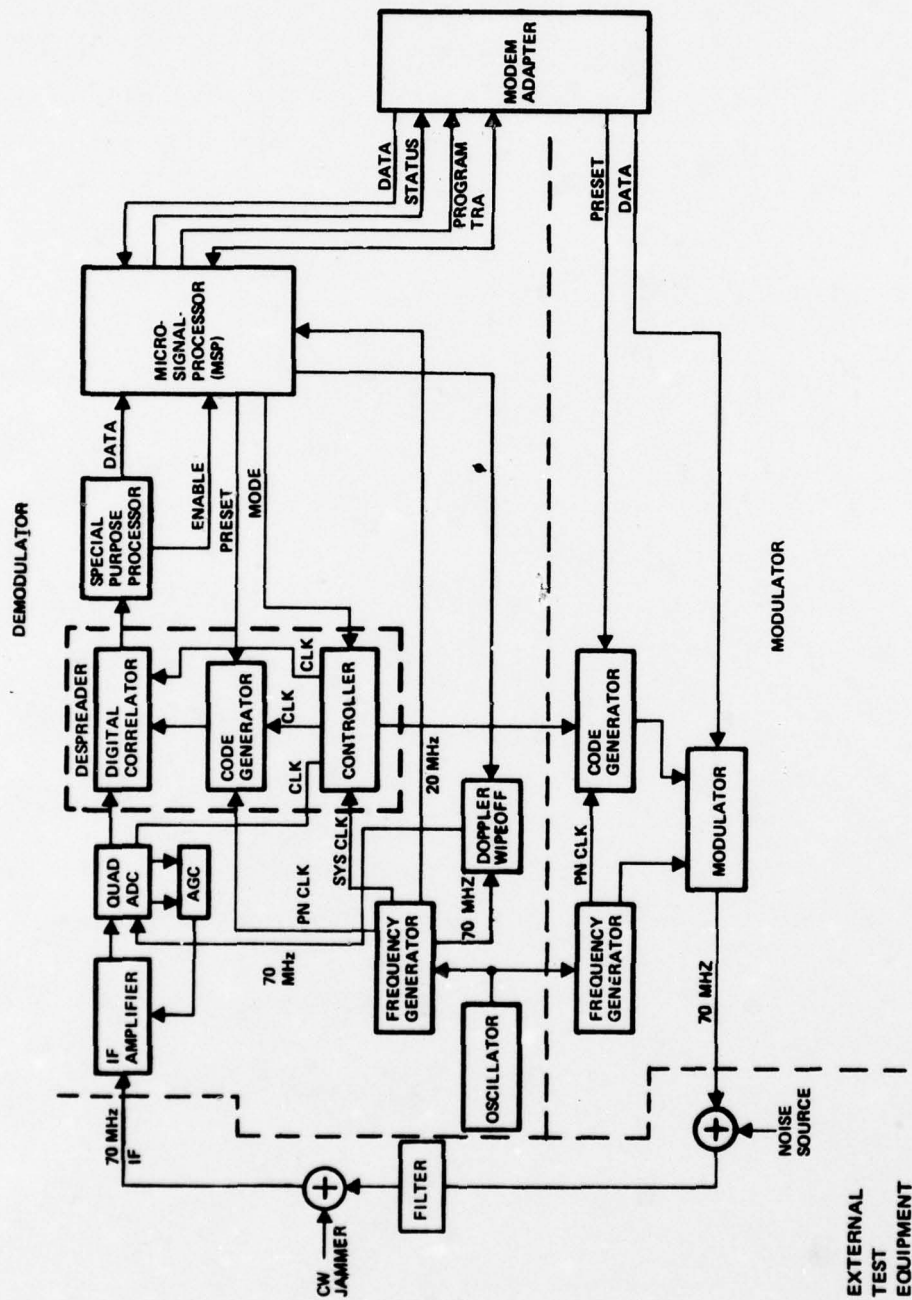


Figure 48. SAM/EM Functional Block Diagram

TABLE 18. SAM/EM MODULE DESIGNATORS

IF AMPLIFIER	IFA*
A TO D CONVERTER	ADC*
DOPPLER WIPE-OFF	DWO
CORRELATOR	COR*
CODE GENERATOR(GPS)	GPN
CONTROLLER	CTR
FREQUENCY GENERATOR	FGN*
SPECIAL PURPOSE PROCESSOR	SPP
MICRO SIGNAL-PROCESSOR	MSP*
MODULATOR	MOD*
CODE GENERATOR	TPN
MODEM ADAPTER	MAD
*STANDARD MODULES	

circuit package. External to the LSI chip is input gating to allow I-Q switching for JTIDS MSK applications. A code generator provides a PN data reference for the auto-correlation. This code generator is configured as a GPS generator (GPN), and is not a standard module as most are customized to the waveform. The controller (CTR) provides all the specialized clocks and timing required for the ADC, COR, GPN and the special purpose processor. Additionally, mode changes are also switched in the CTR, and are generated by the MSP. A frequency generator (FGN), identical to the modulator FGN, creates all the clock sources required by the demodulator from a 100 MHz oscillator. A VCO submodule in the FGN is changed to provide a slightly different set of demodulator frequencies.

The special purpose processor (SPP) module translates and buffers the COR output for the MSP input. Its function is to lower the COR output data rate by accumulating and threshold/comparing the data to a rate more compatible with the MSP processing capabilities. The COR outputs are in the ranges of 10 to 20 M samples/second. The SPP can also include specialized functions such as AGC multiplications and, at times, doppler wipe-off where high rate processing is required (greater than 5 M instructions per second) and functions are iterated such as multiply accumulate continuously. The desired/expected data rate into the MSP is in the range of 250 K words/seconds to 500 K words/second as a function of the algorithms required to be processed simultaneously. The SPP are unique modules and are anticipated to be different for each application.

The MSP (micro-signal-processor) is a core element in providing maximum flexibility and adaptability in the modem. By performing many of the signal processing functions in firmware, a standard module design can be programmed for a variety of tasks that conventionally would require a lot of special purpose hardware. Different programs would generally require only a simple read-only memory (ROM) integrated circuit substitution with no other hardware changes or modifications. The MSP is a bipolar micro-processor configured as a firmware controllable pipeline architecture operating up to 25 M instructions per second. The MSP mechanizes the acquisition, tracking and demodulation algorithms as well as some of the control functions of the modem. The MSP also interfaces with the modem adapter, a test set.

The modem adapter (MAD) is the operator's console for the MSP in addition to providing a data source for the modulator. As an MSP operator's console, the MSP control program containing the microinstructions can be either manually inserted through switches or loaded through a previously programmed EAROM (electrically-alterable ROM). An address and data display is also part of the console. The EAROM interface is compatible with most 8-bit MOS microprocessor development systems although input/output software drivers need to be developed.

A pictorial of the modem is illustrated in Figure 49a. The modulator is shown in Figure 49b as card RF enclosures mounted on small rectangular test fixtures. The high frequency or RF cards in the demodulator also use the same packaging. Printed circuit cards are part of the RF card packaging. The rest of the demodulator, SPP, CTR, GPN and COR, and MSP each have their own carousel test fixtures. The digital cards are mounted perpendicular to a cylinder test fixture as shown in Figure 49c containing the inter-card wiring as well as the input/output. The goal was to minimize inter-card lead lengths and the use of card extenders. At the frequencies of operation, 20 MHz to 100 MHz, stray capacitances can have a major impact. There was sufficient open area for debugging and probing. The modem adapter was a standard wire-wrap card chassis and panel.

3.3 SAM PACKAGING

The SAM packaging for a modem began by developing a criteria for functional partitioning. This is part of the basic task flow which generated the selected SAM card definition, and is depicted in Figure 50. The requirements for the modem were reviewed and an architecture synthesized. The multi-wave form architecture was then evaluated for functional modularity. The waveforms considered were GPS, JTIDS and generic PSK modulation. Considerations such as adaptability and shared processing to minimize hardware resulted in the selection of digital signal processing and high-speed microprocessing. The latter not only allowed processing but is programmable within a broad class of applications.

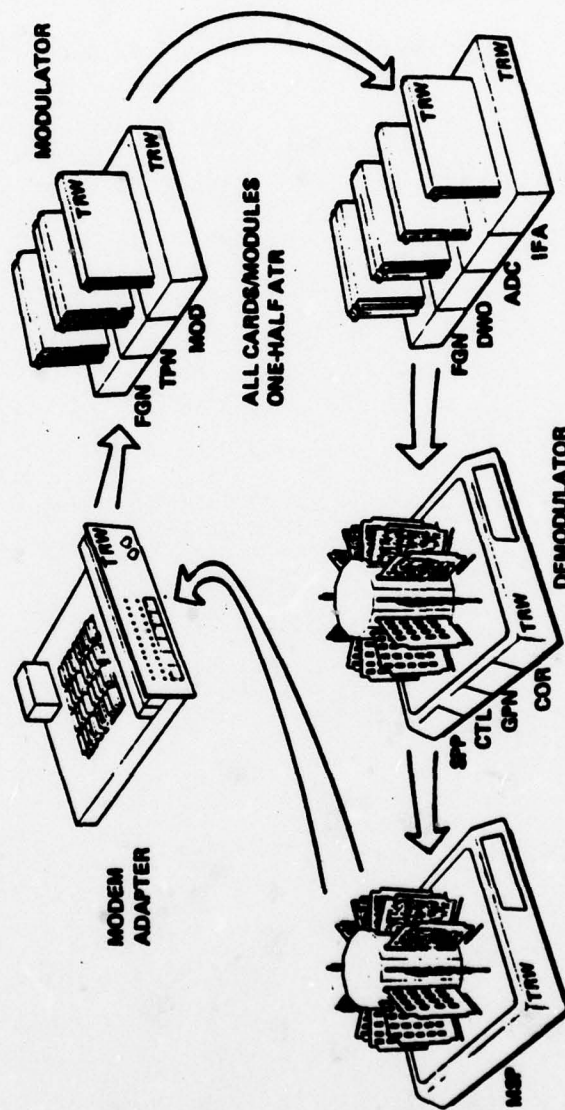


Figure 49a. Demonstration SAM/EM System

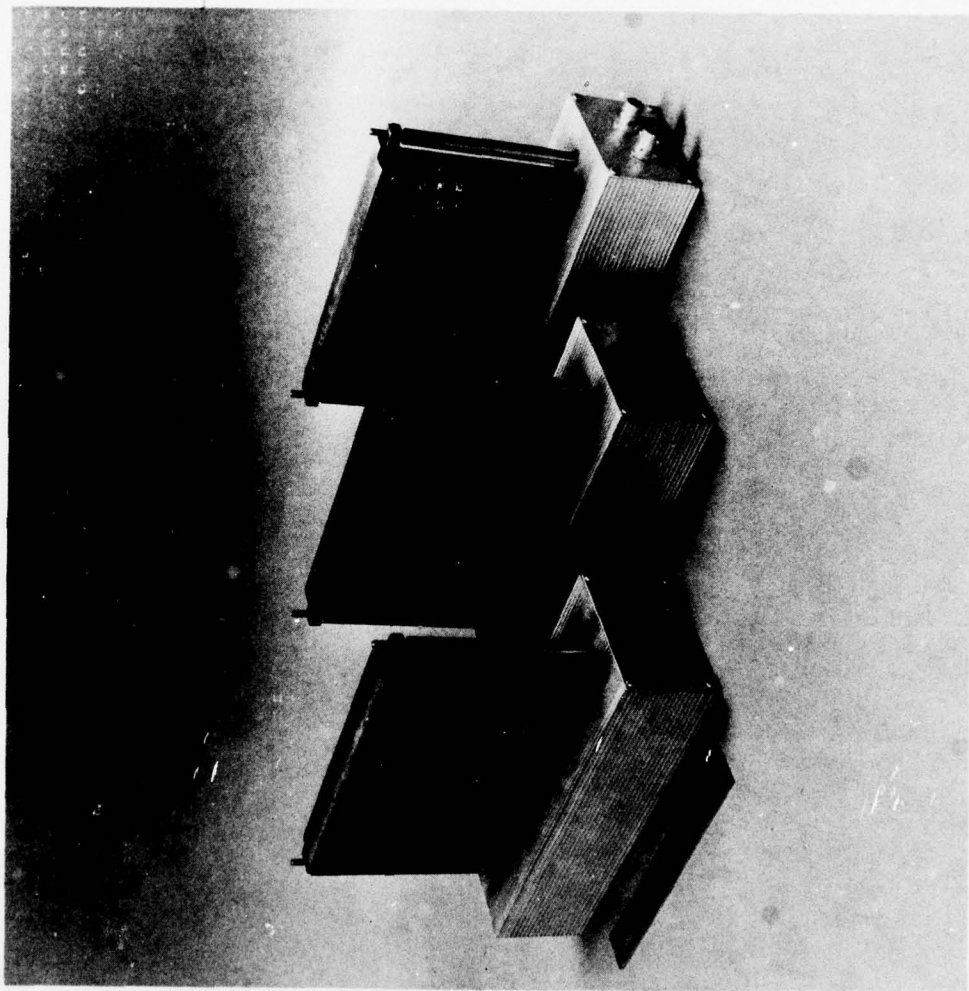


Figure 49b. RF Card Enclosures

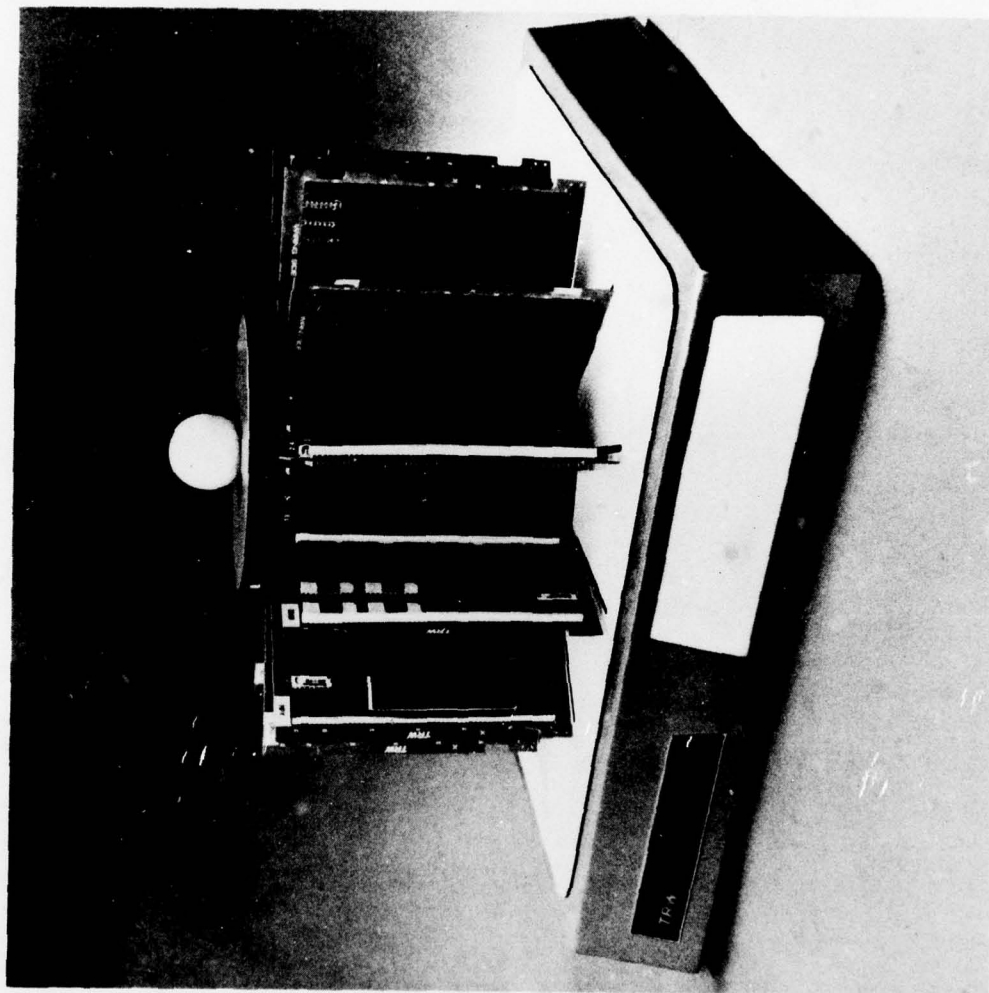


Figure 49c. SAM Test Fixture

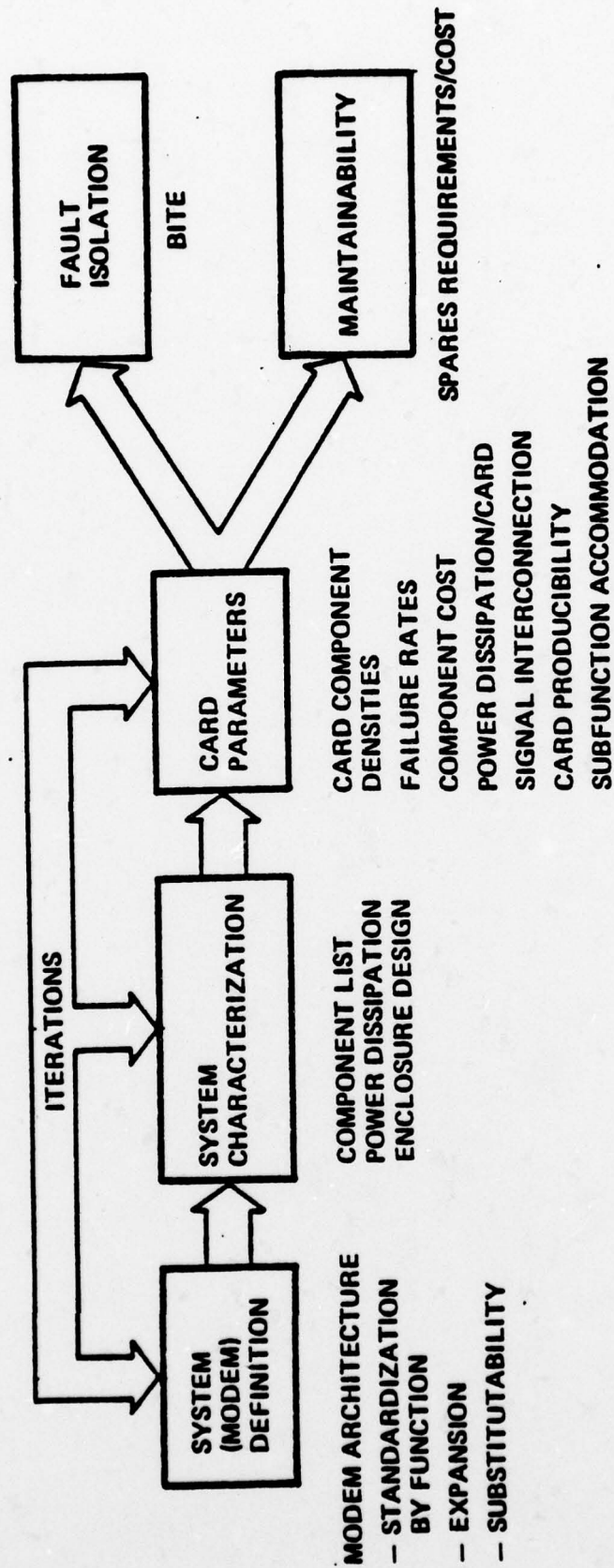


Figure 50. SAM Partitioning Criteria

The system characterization task then took the modem architecture and determined the associated performance and hardware/software parameters. The intent was to define all the pre-determined functions in terms of hardware complexity and real-time firmware operation. A basic concern was matching technology to the required data processing. The ATR enclosure design placed an upper constraint on total power dissipation and so was related to technology.

The card design used the system hardware information to select a card configuration that had high integrated circuit densities and large number of signal interconnections for digital processors (both special purpose and microprocessors), and had the capability to accommodate relatively high power dissipations from digital memory and correlator arrays, and high-speed timing and control logic. Modularity by card per function was another requirement. This would enhance hardware flexibility when using common modules within universal terminal applications where capability spans minimum to maximum configurations. Other factors in card design included card producibility such as minimizing the number of circuit interconnect layers, and the card economics. The estimated card component costs through assembly and test, and the card total reliability in terms of failure rates impacted maintainability and ultimately the deployed costs. The emphasis herein was primarily in terms of technical feasibility with further analysis required to completely bound the modem life-cycle costs.

A basis for card design comparison was the proposed AFAL ATR card standards. A one-half ATR card was selected that met all the requirements for modularity by function and hardware partitioning, and the minimum parts density necessary for low cost complete cards and low power dissipations. A comparative card listing is shown in Table 19. Major differences between the proposed AFAL card and the SAM card are in the maximum power dissipation, only 15 watts in the SAM card, and the 144 signal pins used in the SAM card. A thermal analysis based on projected integrated circuits used, the MIL-E-5400 specification, and the assumed airflow within the one-half ATR enclosure, showed that 15 watts was the card's thermal design

TABLE 19. SAM MODEM PACKAGING TRADEOFFS

	<u>PROPOSED AFAL STANDARD</u>	<u>TRW SAMS</u>
ENCLOSURE SIZE	7.62 X 4.88	7.62 X 4.88
POWER CAPABILITY	30 WATTS MAX	15 WATTS MAX
THERMAL MANAGEMENT	AIR COOLED	AIR COOLED
PARTS DENSITY	30 DIPS 14 LEAD	25 DIPS 16 LEAD
CONNECTOR TYPE	NAFI	NAFI
NUMBER TACTICAL PINS	100 MAX	144 MAX
PIN SPACING	0.1"	0.1"
CONTACT KEYING	YES	YES
TEST CONNECTOR	YES	YES
NUMBER OF TEST POINTS	50	60
MODULE SPACING	0.5"	0.5"

limit. The 144 pins, along the long side of the card (7.6 inch side), is necessary for many digital processors and especially high-performance parallel and/or pipeline microprocessors. Internal data buses of 16 bits parallel or wider, with as many as 8 operating simultaneously (require 128 pins) makes greater than 100 pins a requirement.

Table 20 is a summary of the typical SAM one-half ATR card. Note the card densities can be as many as 40 16-pin dual-in-line integrated circuits and the card design includes both standard printed circuit board and stitch-wire board construction. The latter is for cost-effective low volume production such as prototypes. An assembly drawing of the card is illustrated in Figure 51. A 25-integrated circuit layout allowing for discretes and de-coupling capacitors is shown in Figure 52.

A projected single channel GPS receiver was configured using the one-half ATR cards and the partitioned functions based on digital processing. All functions except the RF front end will be described in the next section. The estimated size is a one-half ATR long enclosure and the power dissipation is in the order of 175 watts (Table 21). The micro-signal-processor is assumed to be capable of handling the navigation computations. Any command and control displays are external to the ATR enclosure. Figure 53 is an artist's conception of the GPS receiver illustrating the SAM one-half ATR cards with the connector on the long side. The air plenum chambers on the top and bottom with the motherboard on the opposite side from the cover plate.

TABLE 20. SAM LOGIC/CIRCUIT CARD CHARACTERISTICS

- PROJECTED USE: ALL DIGITAL APPLICATIONS
- INPUT/OUTPUT PINS • 144 CONTACTS (3 ROWS)
- CONNECTOR TYPE • STANDARD NAFI BLADE AND TUNING FORK
- TEST CONNECTOR • 60 CONTACTS
- POWER CAPABILITY • MAXIMUM 12 WATTS
- PARTS DENSITY • 25 TO 40 16-PIN DUAL-IN-LINE (DIPS) IC'S
- CARD CIRCUITRY • STITCH WIRE OR PWB
- CARD SIZE • 3.69 X 6.25 (1/2 ATR) INCHES
- ENCLOSURE • 4.46 X 6.57 INCHES
- OPTIONS
 - CAM TYPE CARD EXTRACTORS
 - INTERNAL BOARD RESISTORS
 - WEDGE LOCK THERMAL TRANSFER
- DESIGN SPECIFICATION • MIL-E-5400
- CARD TYPES • 25 16-PIN DIP'S FIXED PATTERN OR 40 TO 50 16-PIN DIP'S
UNIVERSAL PATTERN (0.100 INCH CENTERS)

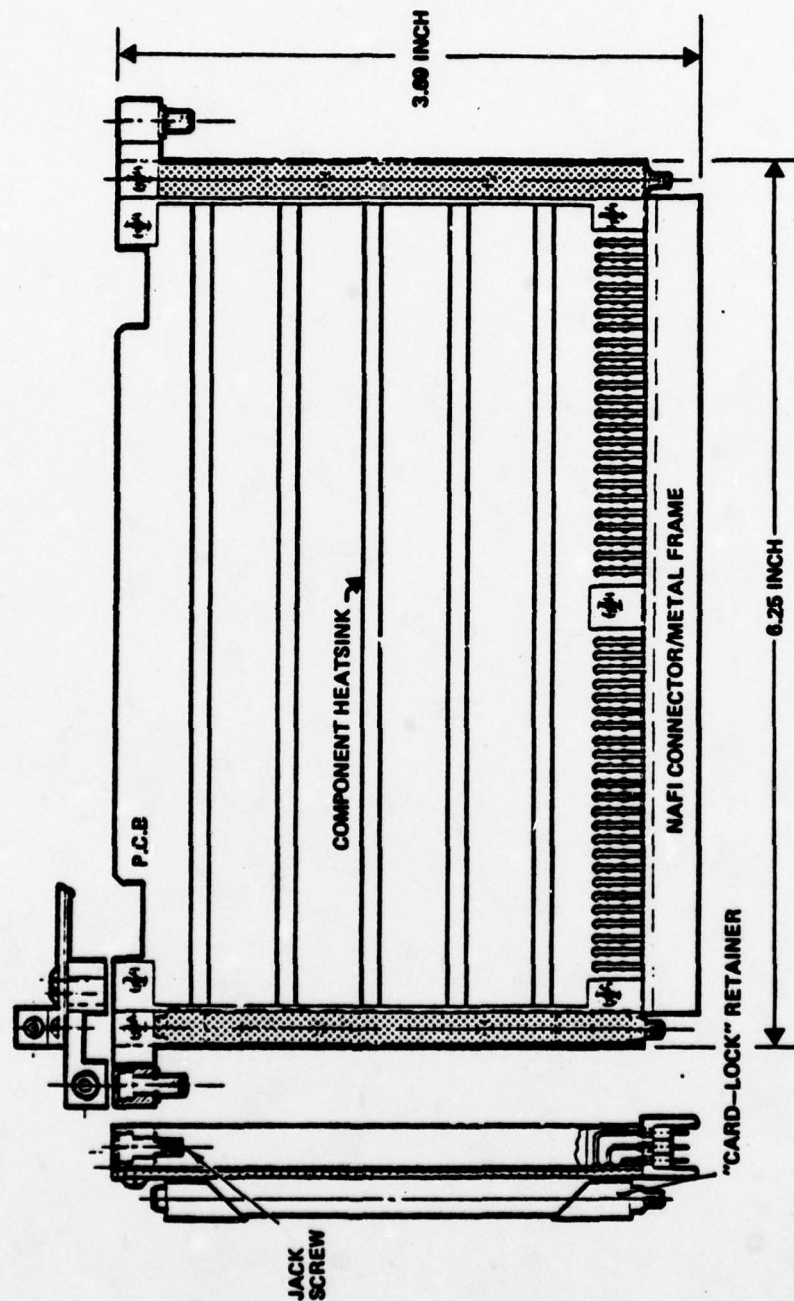


Figure 5i. SAM One-Half ATR Card Assembly

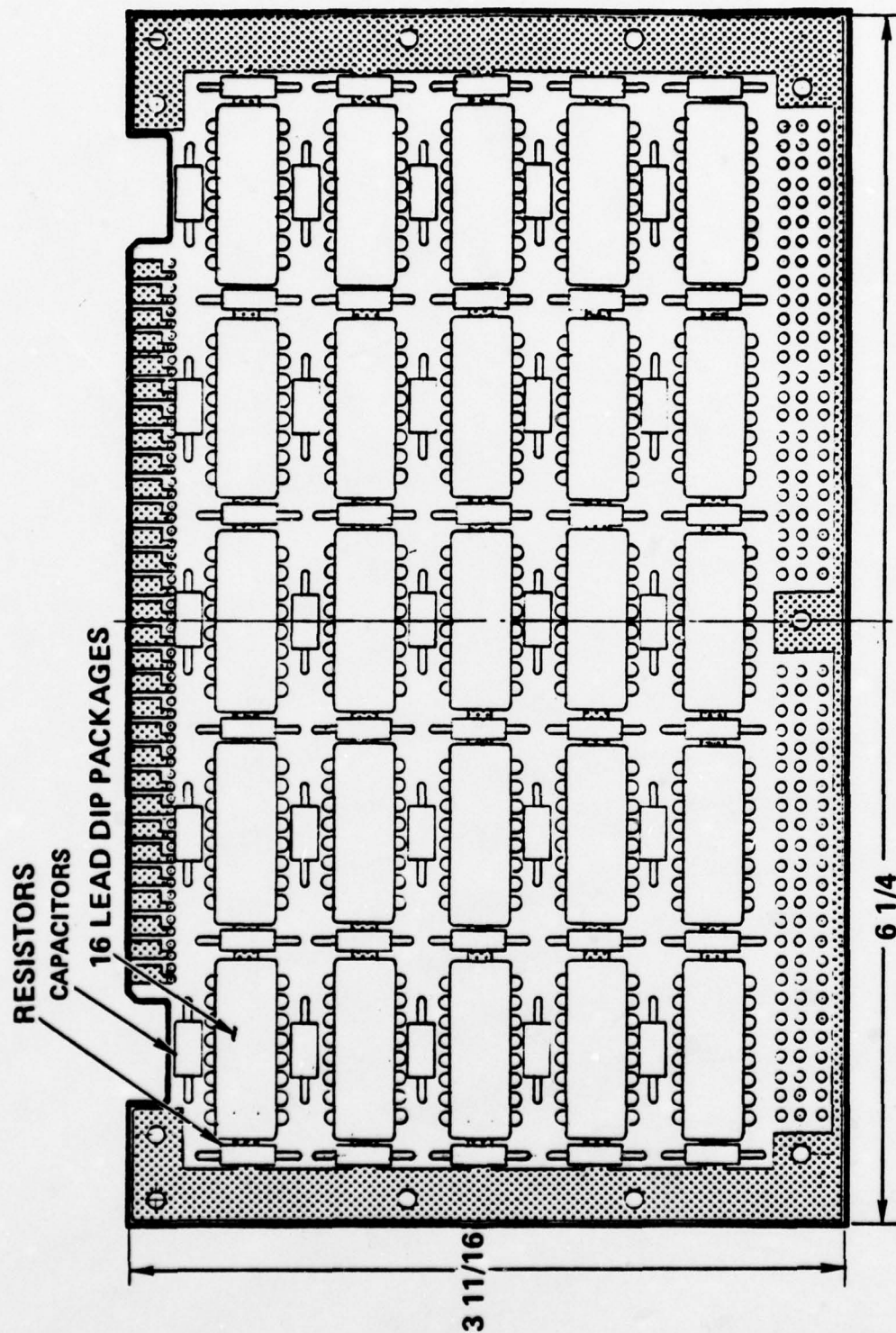


Figure 52. Card Integrated Circuit Layout

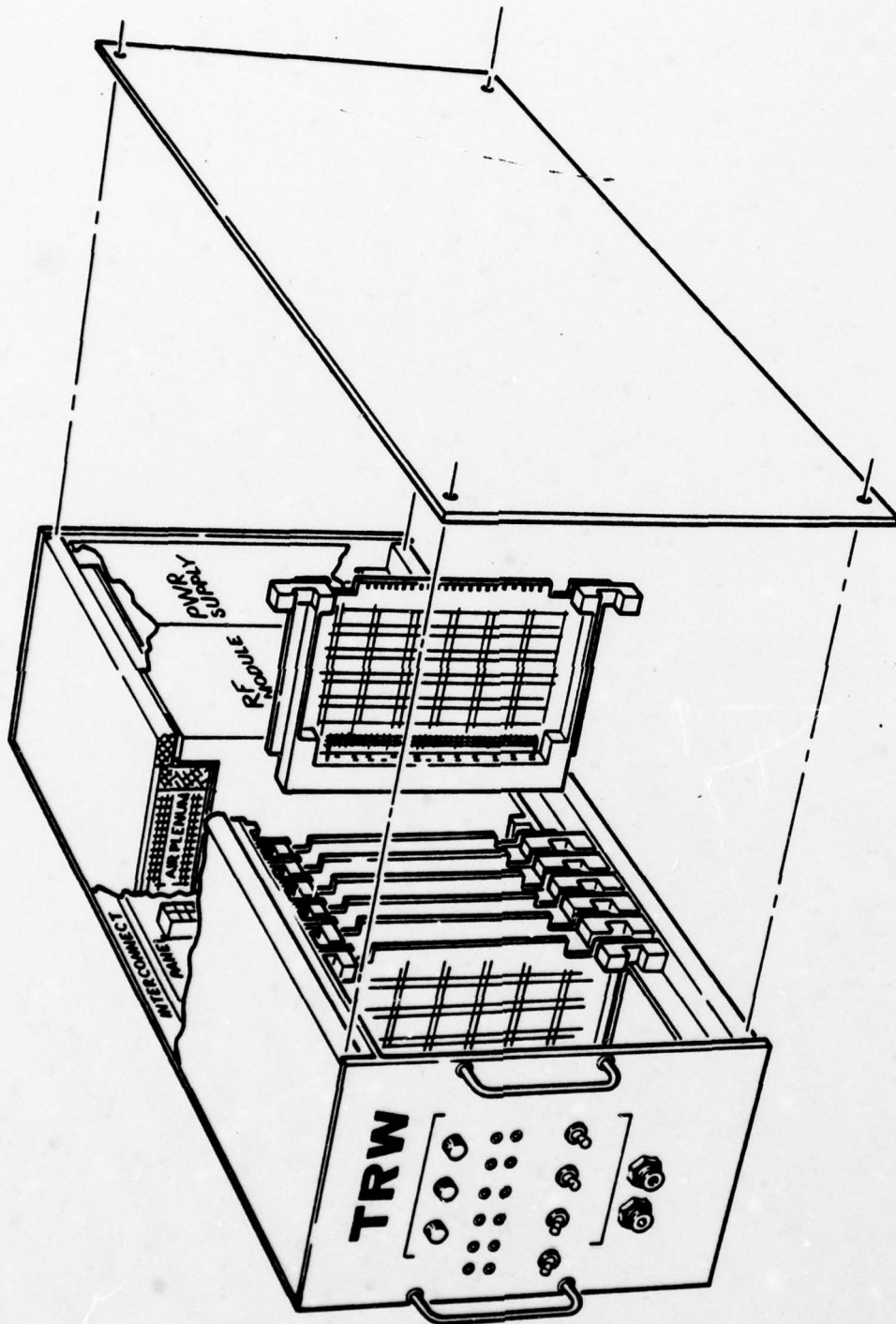


Figure 53. Potential GPS Enclosure One-Half ATR Long

TABLE 21. POTENTIAL GPS SINGLE CHANNEL RECEIVER

<u>FUNCTIONS</u>	<u>CARDS</u>	<u>MODULES</u>
RF FRONT END		2 *
IF AMPLIFIER		1
QUAD A/D CONVERTER		1
CORRELATOR	2	
CODE GENERATOR DESPREADER	3	*
CONTROLLER	1	
SPECIAL PURPOSE PROCESSOR	4	
MICRO-SIGNAL-PROCESSOR	8	
FREQUENCY GENERATOR	2	
POWER SUPPLY		1 *
OSCILLATOR	<hr/>	<hr/> 1 *
	20	6

ESTIMATED CHARACTERISTICS

26 CARDS/MODULES

ONE-HALF ATR LONG (19") ENCLOSURE

NON-MODULE IC COUNT - 485

POWER DISSIPATION - 175 WATTS WITH 75% POWER SUPPLY EFFICIENCY

3.4 Module Functional Descriptions

3.4.1 IF Amplifier Module

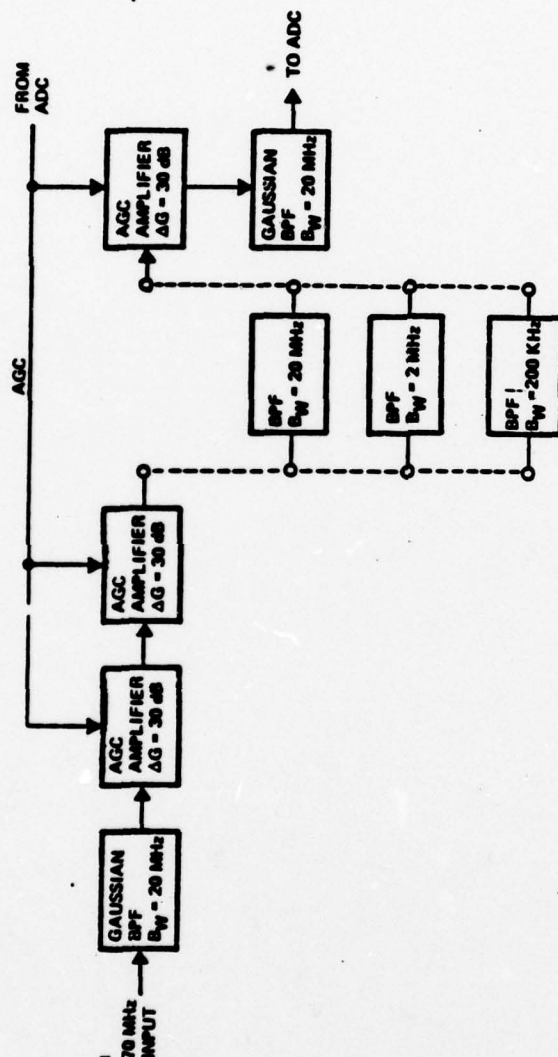
The IF amplifier specified in Figure 54a and shown in Figure 54b processes the 70 MHz input signal and supplies a filtered and normalized signal to the quadrature A/D converter. The specified input signal to this module is not only low level, but also has a large dynamic range (-120 to -50 dBm). Therefore significant processing gain is required for signal amplification and a tracking of automatic gain control (AGC) is also needed to prevent saturation of the amplifier stages and signal distortion and to provide proper loading for the A/D converters.

Four amplifier stages are utilized to realize a maximum gain of 80 dB, and the first three of these are gain controlled by an analog signal supplied from the A/D converter. (Refer to Figure 55). This analog signal is the buffered output of an amplitude detector in the A/D converter, so the gain of the three stages is adjusted to normalize the signal level at the A/D converter. Over 100 dB of gain control range is provided by the IF amplifier to suppress changes in signal level. A plug-in band-pass filter as shown pictorially in Figure 56 provides selectivity to signals passing through the module. The bandwidth is selected to match the signal spectrum. Bandwidths as low as a few tens of kilohertz (crystal filters) up to 20 MHz (lumped constant filters) can be accommodated.

3.4.2 Quadrature A/D Converter

The Quadrature A/D Converter (Figure 57) converts the filtered 70 MHz signal from the IF amplifier into baseband in-phase and quadrature channels and digitizes the resulting signals. The 70 MHz signal is power split and

THE IF AMPLIFIER RECEIVES AN INPUT AT 70 MHZ AND PROVIDES A FILTERED FIXED LEVEL SIGNAL TO THE QUADRATURE A/D CONVERTER BY GAIN-CONTROLLED AMPLIFICATION AND FILTERING.



REQUIREMENTS

- PROVIDES VARIABLE GAIN FROM -15 DB TO +90 DB
- SIGNAL DYNAMIC RANGE (70 DB) TRACKED BY SLOW AGC
- BANDPASS FILTER SELECTABLE BY PLUG-IN SUBMODULE FILTER
- LINEAR OPERATION (1 DB COMPRESSION) AT J/S = 40 DB
- PHYSICAL PARAMETERS
ONE 1/2 ATR MODULE ENCLOSURE 3/4 INCH THICK
LESS THAN 1.5 WATTS POWER DISSIPATION

Figure 54a. IF Amplifier Specification

INTERFACES

INPUT RF FREQUENCY	70 MHZ
BANDWIDTH	20 MHZ
SIGNAL LEVEL	-123 TO -53 DBM
MAX JAMMER LEVEL	SIGNAL LEVEL +40 DB
INPUT IMPEDANCE	50 Ω
INPUT-ADC	
AGC CONTROL VOLTAGE	0-10 VOLTS
AGC CONTROL CURRENT	0-60 mA
LOOP BANDWIDTH	<4 KHZ
OUTPUT-ADC	
FREQUENCY	70 MHZ
BANDWIDTH	SELECTED BY PLUG-IN FILTER SUBMODULE
SIGNAL LEVEL	-33 DBM
OUTPUT IMPEDANCE	50 Ω

Figure 54a. IF Amplifier Specification (Continued)

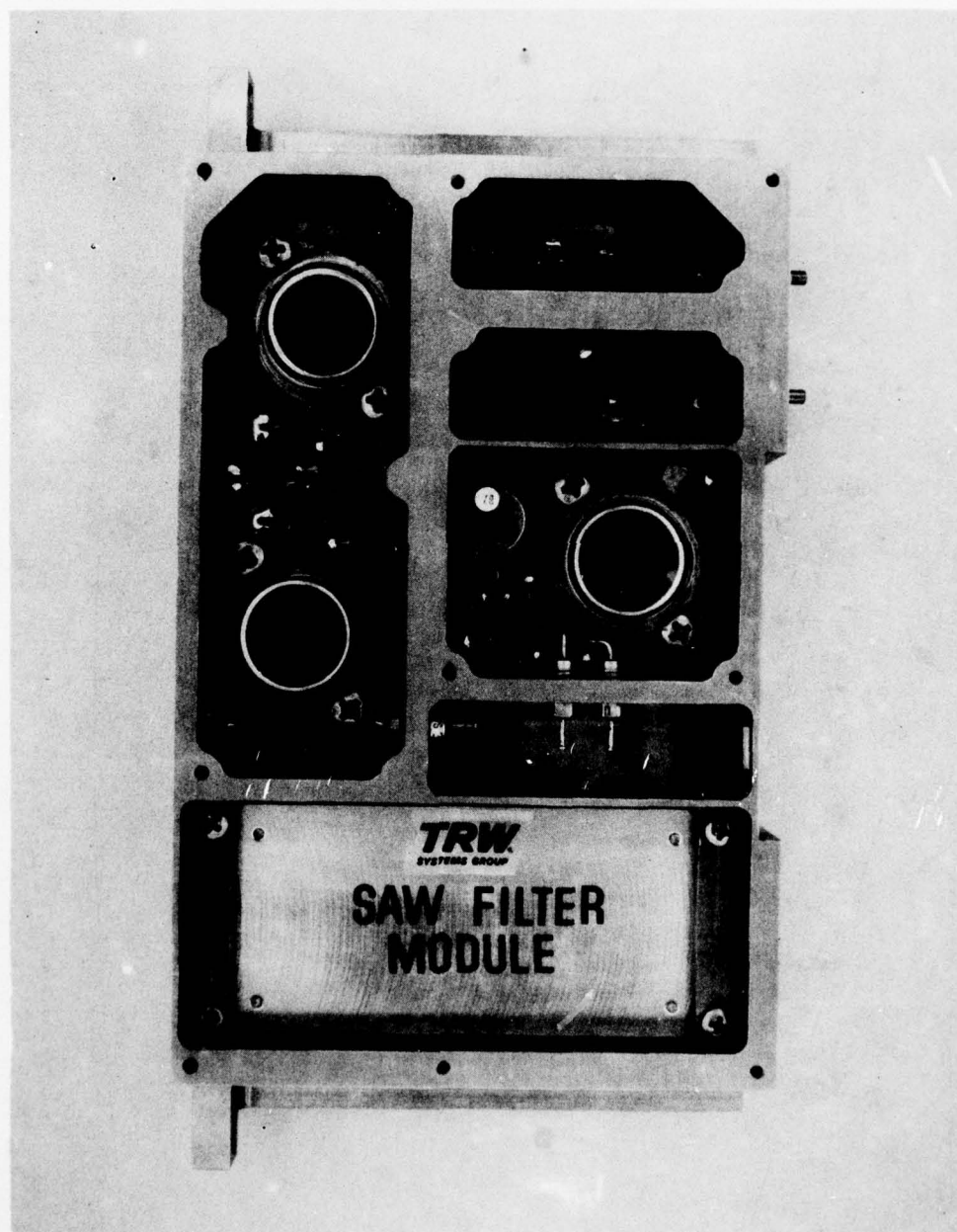
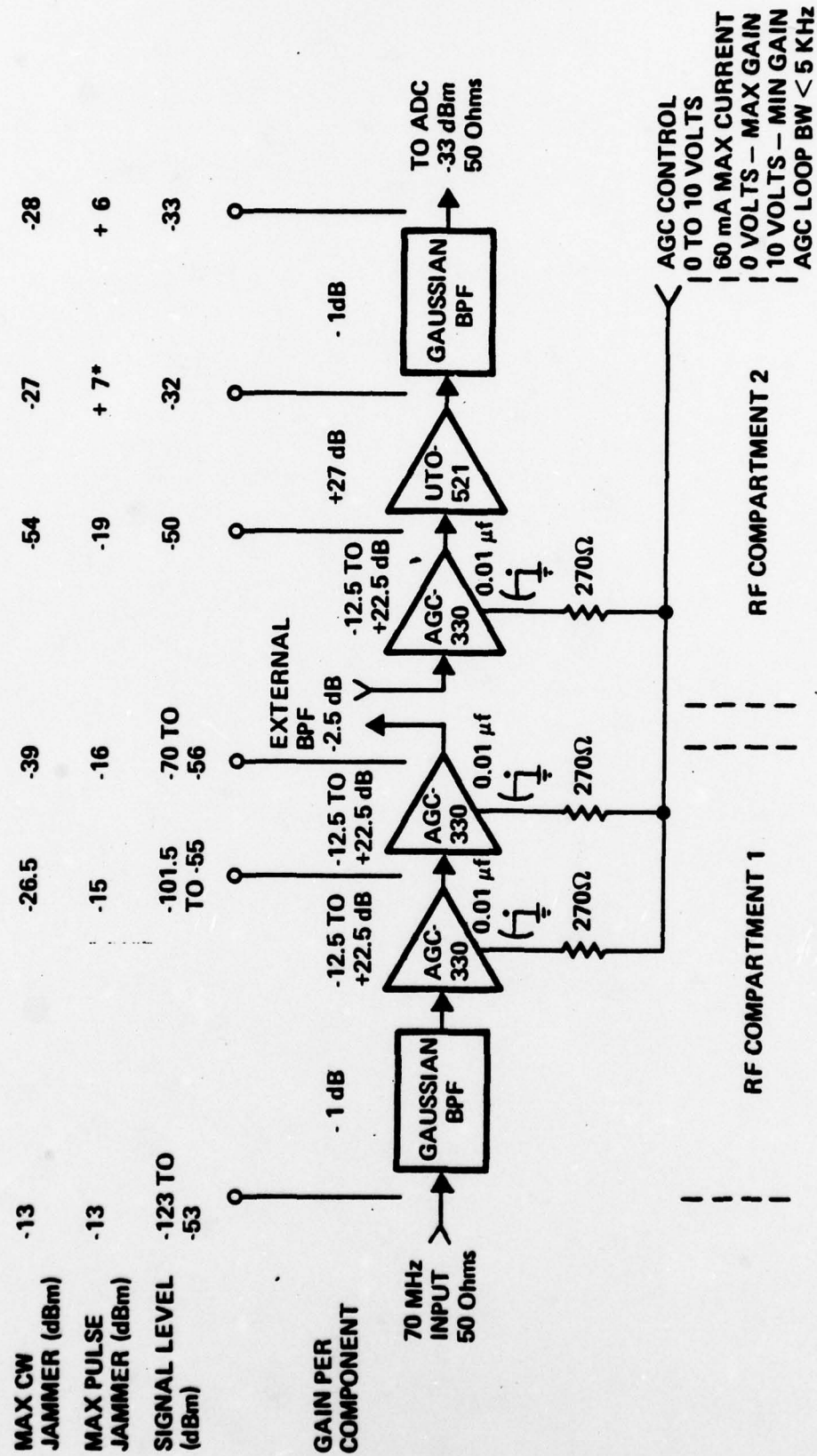


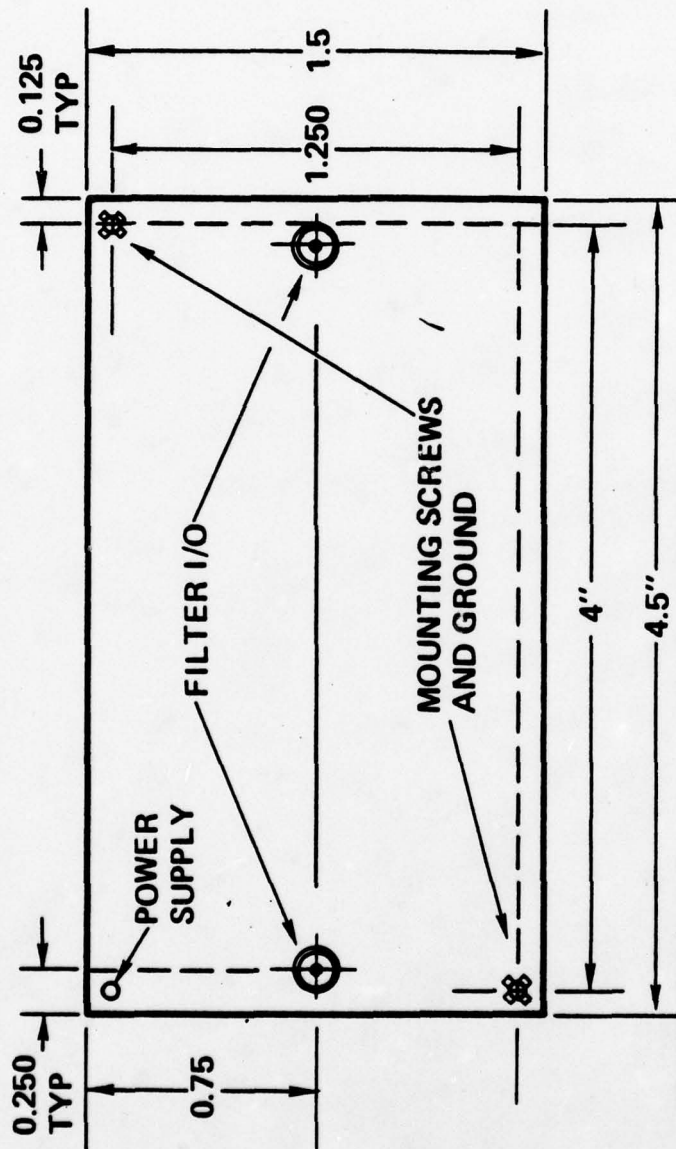
Figure 54b. IF Amplifier Module



*THIS STAGE IS 1 dB IN COMPRESSION FOR PULSE JAMMER

Figure 55. IF Module

- BREADBOARD FILTER BANDWIDTHS FOR PROCESSING: 20 MHz
2 MHz
500 KHz
- STANDARD SAM IF WILL HAVE MODULARIZED PLUG-IN FEATURES



- 70 MHz SIGNALS - 2.5 dB π ATTENUATOR
- 2 MHz FILTER - TELONIC TSC FILTER, OFF-THE-SHELF
- 500 KHz FILTER - 500 KHz SAW FILTER WITH 14 dB GAIN
AMPLIFIER BUILT-INTO FILTER MODULE
- LOWER BW's - CRYSTAL FILTERS

Figure 56. Plug-In Filter

THE QUADRATURE A/D CONVERTER TRANSLATES THE FILTERED 70 MHZ IF SIGNAL INTO BASEBAND INPHASE AND QUADRATURE COMPONENTS, AND DIGITIZES THE RESULTING SIGNAL INTO A BINARY REPRESENTATION.

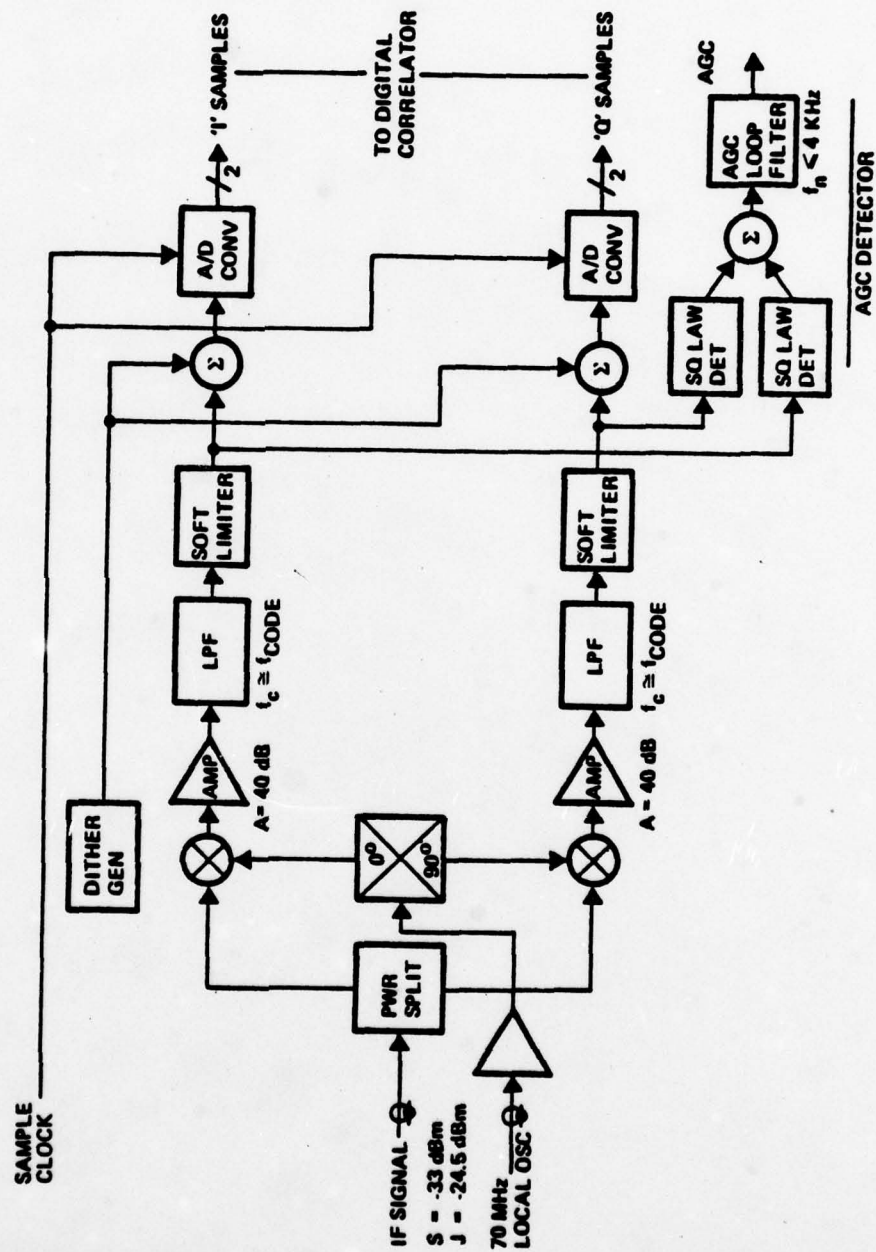


Figure 57. Quadrature A/D Converter Specification

REQUIREMENTS

- I AND Q DOWNCONVERSION AND BASEBAND SAMPLING
- A/D CONVERTER INPUT DITHER SIGNAL: 100×10^3 HZ TRIANGLE
- I AND Q CHANNELS LOWPASS FILTERED AT PN CODE RATE BY SELECTABLE PLUG-IN FILTER
- A/D CONVERTER: 20×10^6 SAMPLES/SEC AND 2 BITS/SAMPLE
- PHYSICAL PARAMETERS
- ONE 1/2 MODULE 3/4 INCH THICK
- LESS THAN 5.0 WATTS POWER DISSIPATION

INTERFACES

INPUTS

INPUT — IFA

CENTER FREQUENCY
BANDWIDTH
LEVELS SIGNAL
CW JAMMER

70 MHZ
SELECTABLE BY PLUG-IN FILTER
-33 +1 DBM
-24.5 DBM MAX

INPUT — DMO

FREQUENCY
LEVEL

70 MHZ
+2 +1 DBM

INPUT — SAMPLE CLOCK

FREQUENCY
LEVEL

2 X PN RATE 20.46×10^6 HZ
ECL COMPATIBLE

OUTPUT — AGC (IFA)

RANGE
POLARITY

0 TO 10 VOLTS/RL = 100 FOUT = 60 MA
0 V FOR LOW SIGNAL/10 V FOR HIGH SIGNAL

OUTPUT — I, Q SAMPLES

SAMPLE
RATE
LEVEL

2 BITS/SAMPLE
 20.46×10^6 SAMPLES/SEC
ECL COMPATIBLE

Figure 57. Quadrature A/D Converter Specification (Continued)

downconverted to baseband using quadrature 70 MHz L.O.s which are derived from the Doppler Wipeoff module. The resulting in-phase and quadrature signals are filtered to remove the double frequency term and buffered to drive the A/D converters. Each channel contains a soft limiter, which saturates on large inputs to prevent the A/D converter from saturating. The dither signal is added in just prior to the A/D converter. Also, prior to the A/D converter, a detection of the total signal power is made and a filtered version is fed back to the IF amplifier for gain control.

3.4.3 Digital Correlator

The digital correlator module performs matched filtering of the received PN coded signal for sync acquisition and data demodulation. Eight LSI correlator chips each 32 bits in length are provided for the MSB and LSB of the in-phase and quadrature channels. Correlation of code patterns longer than 64 bits (as for GPS) are performed through post detection accumulation of successive 64-bit correlations.

A diagram of the correlator is shown in Figure 58. The input multiplexer allows the I channel to be cross-connected to the Q channel. This is of value in situations where the I and Q channel resources can be time-shared. It is also useful in demodulating the MSK form modulation, which is used on JTIDS. The Mod-2 adders prior to the correlators allow the PN code to be stripped off, if desired, prior to correlation. Again, this is necessary for JTIDS processing.

The correlator chips compare the reference code to the received code and generates a digital output proportional to the degree of correlation. These outputs are weighted and summed to form the correlated I and Q outputs to the Special Purpose Processor.

3.4.4 Special Purpose Processor

The Special Purpose Processor (Figure 59) is not a SAM and must be designed for each specific application. For the SAM terminal, which is targeted for demonstration of GPS and generic PSK processing the Special Purpose Processor functions primarily as a post detection accumulator. Correlation values from the correlator module are integrated further in the Special Purpose Processor to effect a longer correlation than is possible in the correlator alone. Concurrently the data rate into the MSP is reduced.

THE DIGITAL CORRELATOR PERFORMS MATCHED FILTERING OF THE RECEIVED DIGITIZED CODED SIGNAL FOR INITIAL SYNC ACQUISITION. ADDITIONALLY, DATA DEMODULATION WITH CYCLIC-CODE-SHIFT KEYED MODULATION CAN BE ACCOMMODATED BY USING A REFERENCE PATTERN RECIRCULATED FOR MAXIMUM-LIKELIHOOD DETECTION.

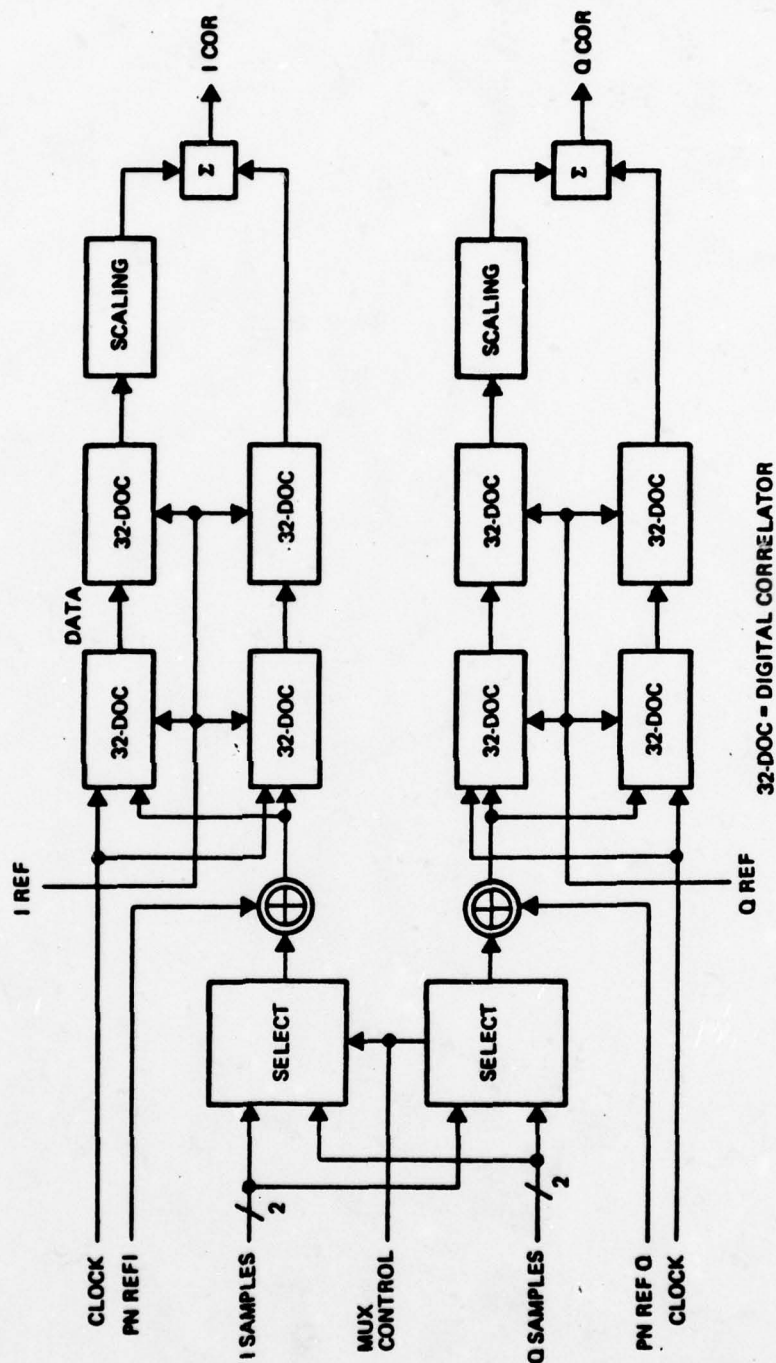


Figure 58. Digital Correlator Specification

REQUIREMENTS

- INITIAL SYNC ACQUISITION FOR GPS/DATA DEMODULATION FOR JTIDS
- BASIC ELEMENT: 32-BIT DIGITAL CORRELATOR WITH AN 8-BIT BINARY OUTPUT REPRESENTATION/100 X 10⁶ BPS OPERATION
- CASCADABLE IN 2 BITS PER I AND Q CHANNEL BY EITHER 32 OR 64 BITS OF CORRELATION
- PHYSICAL PARAMETERS
 - TWO 1/2 ATR DIGITAL CARDS
 - POWER DISSIPATION LESS THAN 12 WATTS

INTERFACES

INPUT — ADC	2 BITS/SAMPLE
SAMPLE RATE LEVEL	2 BITS/SAMPLE
	20.46 X 10 ⁶ SAMPLES/SEC
	ECL COMPATIBLE
INPUT — GPN	
DATA RATE PN REF/I,Q REF	20 X 10 ⁶ BPS MAXIMUM
CLOCK LEVELS	COINCIDENT WITH DATA
	ECL COMPATIBLE
OUTPUT	
DATA I, Q COR RATE LEVEL	8-BIT BINARY REPRESENTATION OF COR VALUES
	PN CODE RATE (UP TO 20 MBPS)
	TTL COMPATIBLE

Figure 58. Digital Correlator Specification (Continued)

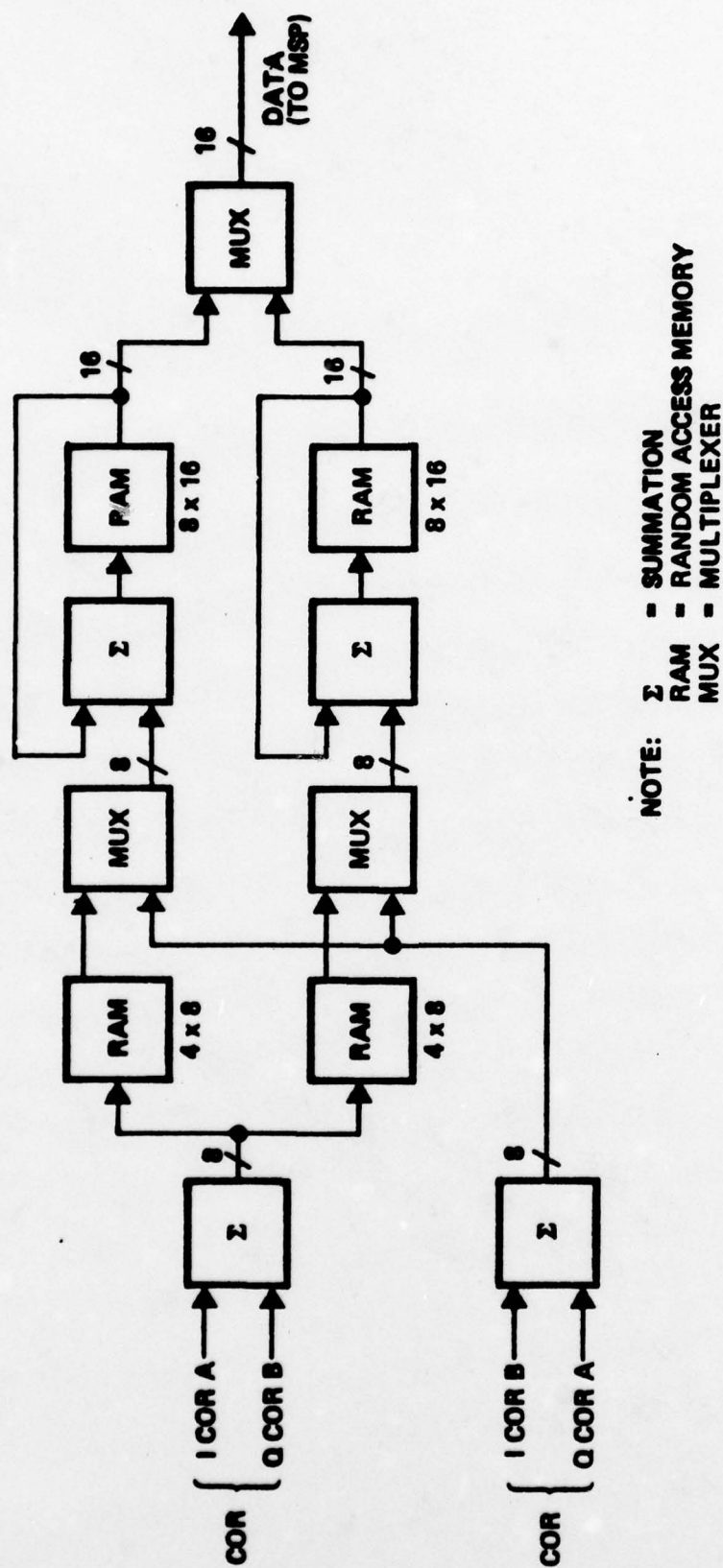


Figure 59. Special Purpose Processor Block Diagram

The special purpose processor provides preintegration to reduce the input data rate to the micro-signal-processor. Additionally data buffering and formatting is done as part of the preintegration.

REQUIREMENTS

- Accommodate input rates at two times the PN chip rate (20 MHz maximum).
- For the given application, GPS and generic PSK, reduce the data rate to less than 256K words/second, using a 5M word/sec 16 word block transfer.
- Physical parameters
 - Four 1/2 ATR cards
 - Less than 22 watts power dissipation

INTERFACES

Input - COR	
Data	8-bit parallel word
Rate	2 x PN code rate (up to 20 Mbps)
Level	TTL compatible
Output	
Data	1 word x 16
Word rate	5×10^6 words/sec
Block rate	256×10^3 blocks/sec
Clock	16 per block
Sync	1 pulse coincident with first word

Figure 59. Special Purpose Processor Block Diagram (Continued)

3.4.5 Controller

The Controller (CTR) is not a SAM in that it provides all the applications unique required timing, clock and control signal for the DWO, GPN, COR, SPP, and the MSP. The Controller consists of multiple clock countdown logic chains and special control signals derived from the master oscillator and special command signals. Refer to the block diagram and specification in Figure 60.

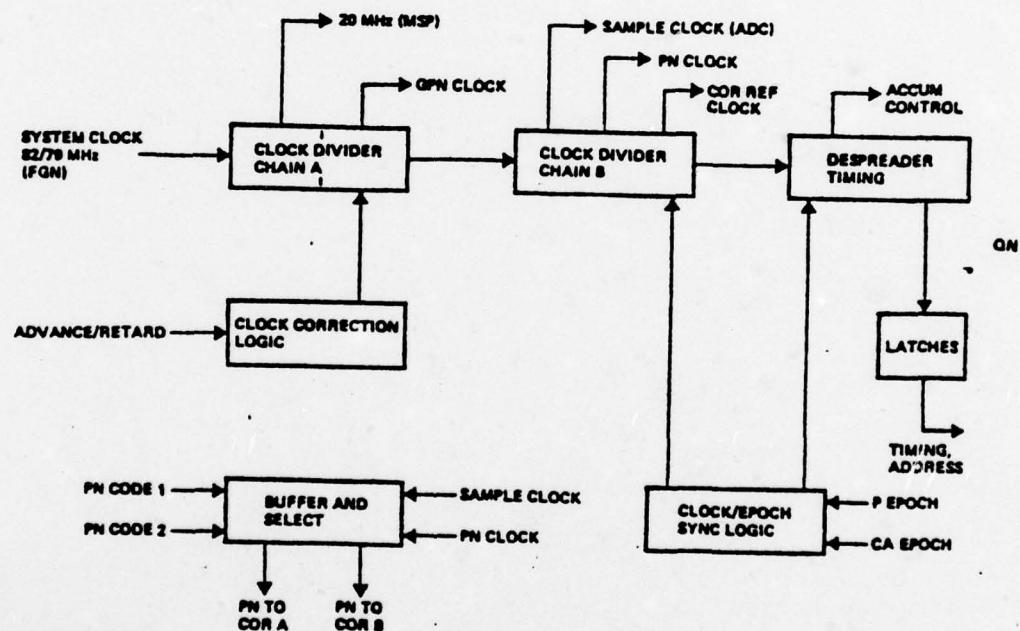


Figure 60. Controller Block Diagram

The controller provides all the required clock and control signals, fully synchronous from a centralized point.

REQUIREMENTS

- Provide clock and control signals to the GPN, ADC, and COR modules.
- Generate the 20 MHz clock for the MSP.
- Provide select and mode control for GPS or generic PSK.
- Physical parameters

Two 1/2 ATR cards and less than 13 watts power dissipation.

INTERFACES

<u>INPUT - FGN</u>	82/79 MHz / 2 +1 DBM
Frequency	
<u>INPUT - MSP</u>	Advance/retard control word - 16-bits parallel with clock
Data	
<u>INPUT - GNP</u>	Pn Code 1;2 / TTL compatible with clock
Data	
<u>OUTPUT</u>	
MSP	20 MHz
GPN	Clock
COR	Clock, PN data, Logic Control/TTL compatible
SPP	Logic / TTL compatible

Figure 60. Controller Specification (Continued)

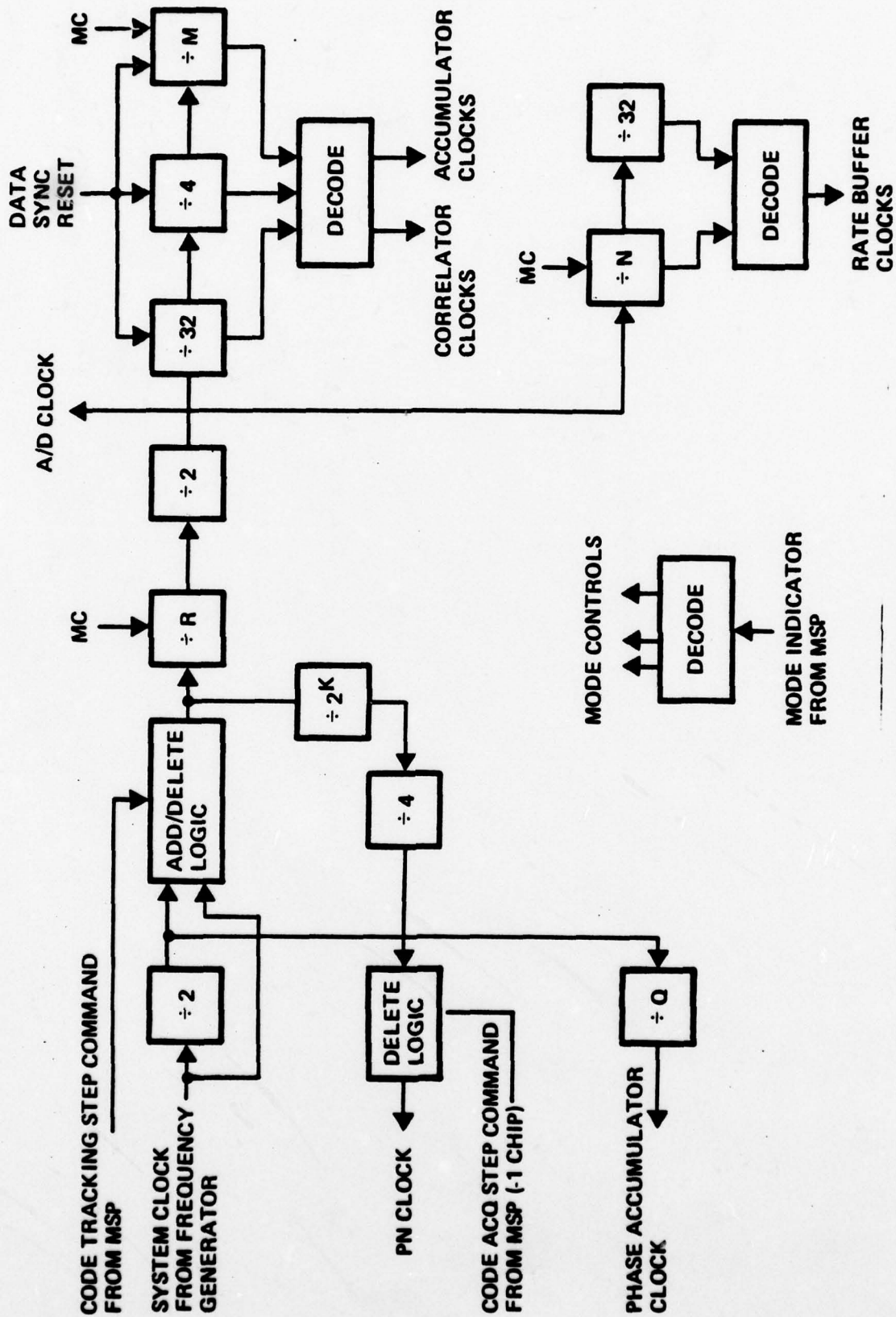


Figure 60. Controller Specification (Continued)

The Special Purpose Processor for the SAM terminal consists of a bank of 16 word accumulators. The 16 word accumulator is necessary for mechanizing the GPS code acquisition algorithm, which essentially searches over 16 time hypotheses simultaneously.

3.4.6 Micro-Signal Processor Module

The Micro-Signal Processor (MSP) performs code and frequency acquisition, code tracking, frequency and phase tracking and bit sync. It is based on the JTIDS RSED microprocessor and is referred to as a "pipeline" microprocessor. The "pipeline" results from the interrelationship of the central processing unit and the hardware multiplier and the separation of the main memory into an input/output memory (see Figure 61a). These central processor elements can then be serially connected in a time division multiplex operation, each simultaneously processing a part of an algorithm. Figure 61b shows the micro-signal-processor module.

The central processing unit performs all the computational and logic operations. The hardware multiplier is interconnected with the CPU through the data transfer network, allowing data interchanges for add-multiply operations in a pipeline mode. Other functions include the input and output random-access memories for temporary data storage and general working registers, and the programmable ROM for nonvolatile storage. The control ROM provides the facility to systematically execute the sequences of micro-instructions.

Microprocessors are a relatively new but rapidly advancing class of digital elements. A microprocessor can be a very small computer-like module where all basic computer functions (data storage, input/output, computations, and control) are packaged in a single logic plane or printed circuit board. Microprocessors have inherent flexibility through a read only memory containing microprograms, data bus interconnection network, and functional modularity. Microprocessors, presently considered as the next generation digital system building block, offer lower cost through time shared multiple program operation using the same hardware, resulting in parts reduction and shorter design time.

Microprocessors for signal processing or micro-signal-processors (MSPs) perform all the post-correlation digital signal processing. This includes the functions of acquisition, synchronization, tracking, modulation, demodulation, encoding, decoding, doppler processing, data routing and

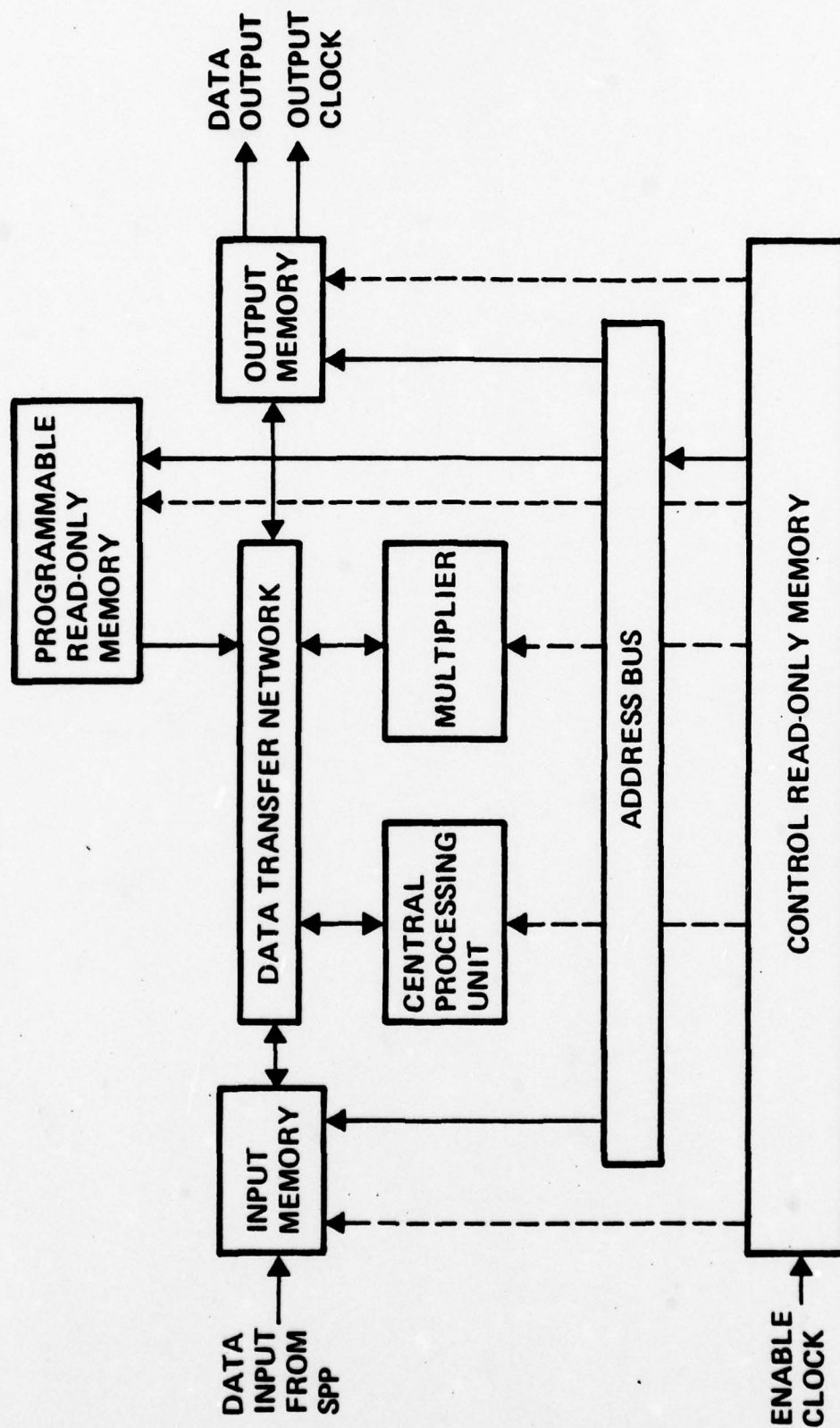


Figure 61a. Micro-Signal-Processor Module Block Diagram

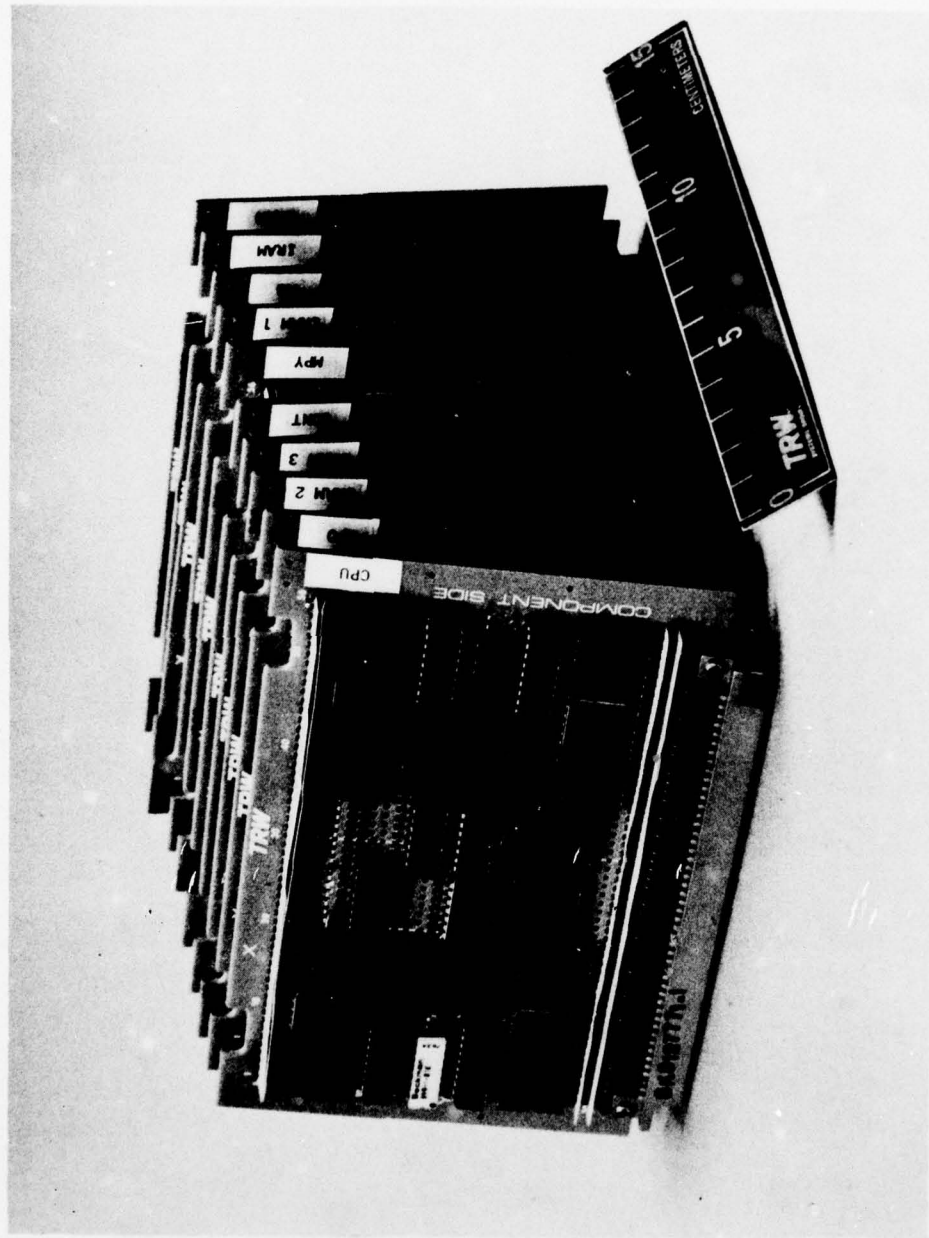


Figure 61b. Micro-Signal-Processor Module

formatting, and data flow control. The MSP also provides the data interface control and buffering for the control displays and other processors.

The basic microprocessor design philosophy, given the data processing requirements, has been to use functional modularity for hardware expansion, microprogrammed control for flexible orderly control logic, simultaneous parallel instruction processing, and high execution rates to minimize total firmware development. Alternately, firmware (software) sophistication has been traded for straightforward hardware implementation.

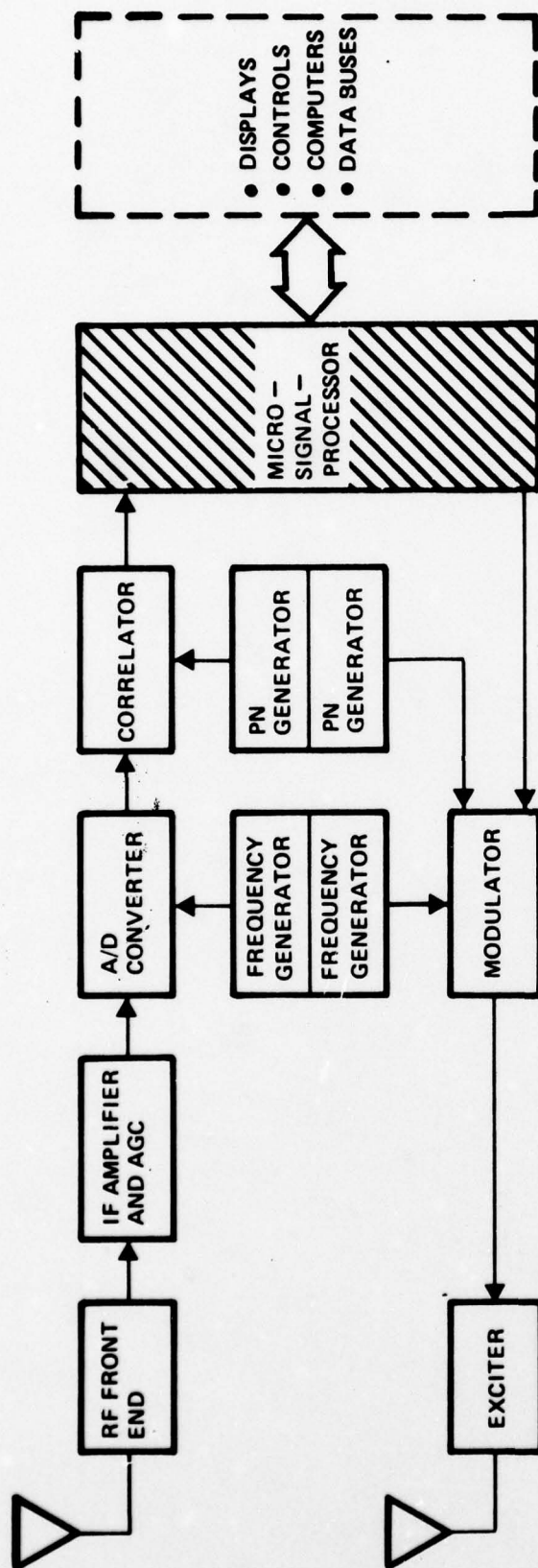
Digital Signal Processing Requirements

Signal processing algorithms generally require: realtime response, continuous digital input/output data (as opposed to a burst), simultaneously processing multiple algorithms especially for multiple functions and waveforms, many algorithmic sequences with iterative sums-of-products (recursions), and fast basic operations such as multiplication, accumulation and test and branch.

Sorting through the aforementioned characteristics indicates that a signal processor must be flexible and modular enough to meet realtime throughput rates of spread spectrum processors in the range of 50 to 100 kwps using intradependent computational functions (multiply-add), high speed internal data transfer networks and user data interface exchanges, microprogrammable control for maximum flexibility with a processor word size of 12 to 16 bits per word. In addition, the processor must be modular by element (memory, CPU) and complete unit as an MSP for multiprocessor configurations, and meet all applicable MIL-E-5400 requirements. The MSP meets the given requirements and is selected for the candidate design. The micro-signal-processor application for the SAM modem is shown in Figure 62. This is a typical spread spectrum digital receiver architecture. The MSP functions tabulated cover all the post-correlation data/signal processing. A micro-signal-processor specification is listed in Figure 63.

3.4.7 Modulator Module

The Modulator block diagram is shown in Figure 64a and performs quadriphase modulation of the 70 MHz carrier with the in-phase and quadrature digital data inputs. The Modulator module is shown in Figure 64b. The input data is first combined with the PN code prior to being mixed with the quadrature carriers. The result is then summed, amplified and filtered to



FUNCTIONS PERFORMED

- ACQUISITION
- TRACKING
- DEMODULATION
- SYNCHRONIZATION
- ENCODER/DECODER
- ERROR CORRECTION/DETECTION
- DATA FORMATTING
- TERMINAL MODE CONTROL
- BUILT-IN-TEST
- PERIPHERAL CONTROL/TRANSFERS

Figure 62. System Requirements

THE MICRO-SIGNAL-PROCESSOR (MSP) PERFORMS ALL OF THE POST-CORRELATION DIGITAL SIGNAL PROCESSING IN A SPREAD-SPECTRUM MODEM USING A MICROPROCESSOR IMPLEMENTATION. THIS PROCESSING INCLUDES THE COMPLETE ALGORITHMS FOR DATA ACQUISITION AND SIMULTANEOUSLY THE PHASE TRACKING LOOP, CODE TRACKING LOOP, DATA DEMODULATION, BIT SYNCHRONIZATION, AND SEQUENCE CONTROLLER FOR MODULE INTERACTIONS.

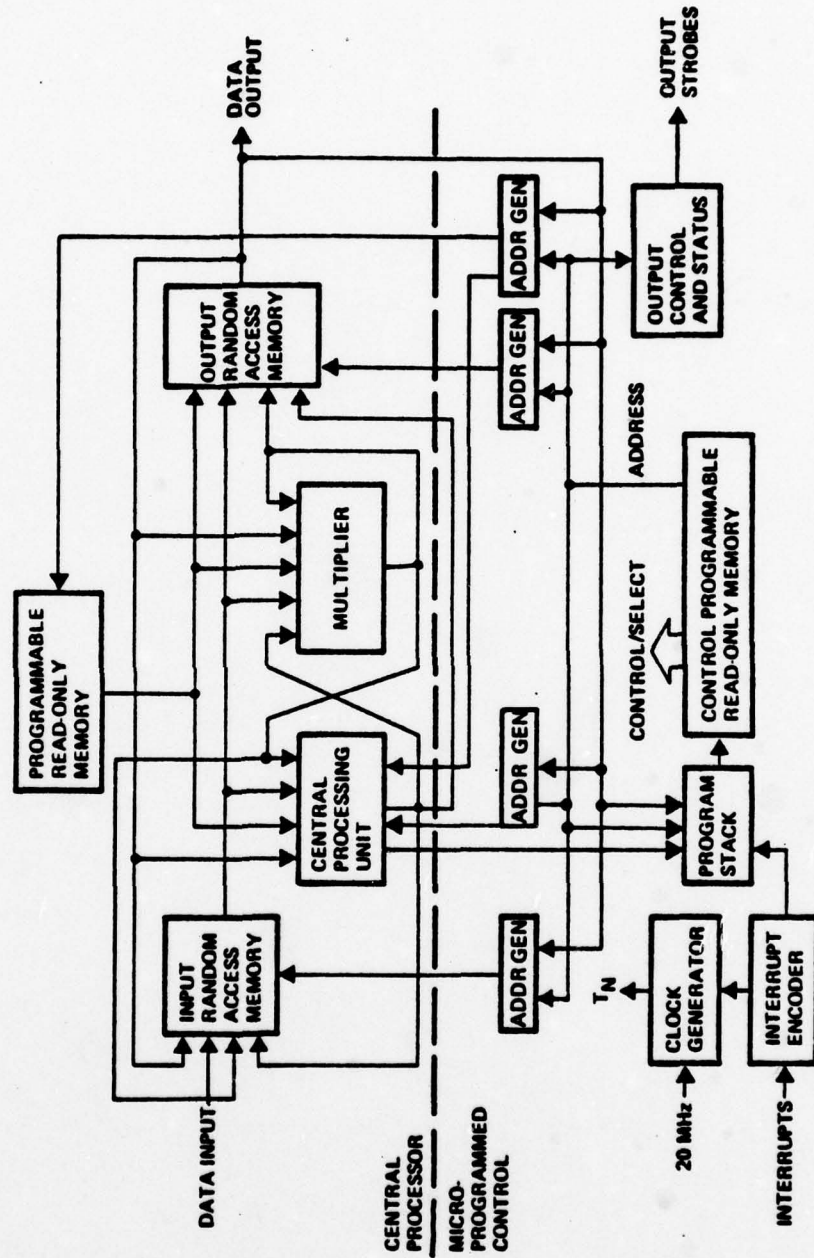


Figure 63. Micro-Signal-Processor Specification

REQUIREMENTS

- DATA PROCESSING OF THE FOLLOWING PSK ALGORITHMS AFTER DIGITAL CORRELATION AT A MAXIMUM OF 38.4K.BPS REALTIME DATA RATE

ACQUISITION OR
PHASE TRACKING LOOP
CODE TRACKING LOOP
DATA DEMODULATION
BIT SYNCHRONIZATION

- MICRO-SIGNAL-PROCESSOR HARDWARE

MICROPROGRAMMABLE CONTROL — HORIZONTALLY ENCODED
INTRADEPENDENT MULTIPLICATION AND ACCUMULATION

DIRECT-MEMORY-ACCESS: 5×10^6 WORDS/SEC WITH INTERRUPT
SAVE/RESTORE CYCLE $< 2 \mu\text{SEC}$ EACH

CENTRAL PROCESSING UNIT: AMD 2901 OR EQUIVALENT

DATA WORD SIZE: 16 BITS/WORD

HARDWARE BINARY MULTIPLIER: 16 BITS X 16 BITS IN 200 NSEC
BASIC MACHINE CYCLE: 400 NSEC

INSTRUCTION EXECUTION RATES: UP TO 20×10^6 INSTR/SEC

PROGRAM MEMORY CAPACITY: LESS THAN 512 WORDS

DATA MEMORY CAPACITY: UP TO 4096 WORDS

PHYSICAL PARAMETERS: SIX TO EIGHT 1/2 ATR CARDS IN A DIP IC CONFIGURATION
LESS THAN 40 WATTS POWER DISSIPATION

INTERFACES

ALL DATA WORDS 16-BITS IN PARALLEL TTL COMPATIBLE
EACH PULSE 50 PERCENT DUTY CYCLE TTL COMPATIBLE

Figure 63. Micro-Signal-Processor Specification (Continued)

INTERFACES (CONTINUED)

SPECIAL PURPOSE PROCESSOR

INPUT: DATA BLOCK — 1 WORD X 16
CLOCK — 16 PER BLOCK
SYNC — 1 PULSE COINCIDENT WITH FIRST WORD
WORD RATE — 5×10^6 WORDS/SEC
BLOCK RATE — 256×10^3 BLOCKS/SEC

CONTROLLER

OUTPUT: DATA WORD — 1 WORD
DATA STROBE — 1 PULSE COINCIDENT WITH WORD

PN GENERATOR — GPS

OUTPUT: DATA WORD X2
DATA STROBE — 1 PULSE X2 COINCIDENT WITH WORDS
ENABLE — 1 PULSE FOLLOWING WORD BLOCK

MODEM ADAPTER

INPUT: DATA WORD — 1 WORD
DATA STROBE — 1 PULSE COINCIDENT WITH WORD
SYNC — 1 PULSE COINCIDENT WITH WORD
WORD RATE — 100×10^3 WORDS/SEC

OUTPUT: DATA WORD (TWO PORTS EACH) — 4 WORDS
DATA STROBE — 1 PULSE COINCIDENT WITH WORD
WORD RATE — 100×10^3 WORDS/SEC

DOPPLER WIPEOFF

OUTPUT: DATA WORD — 1 WORD X2
DATA STROBE — 1 PULSE X2 COINCIDENT WITH WORDS

20 MHZ CLOCK

INPUT: 2N5515 RECEIVER COMPATIBLE
FREQUENCY: 20×10^6 HZ ± 5 PERCENT WITH 50 PERCENT DUTY CYCLE

Figure 63. Micro-Signal-Processor Specification (Continued)

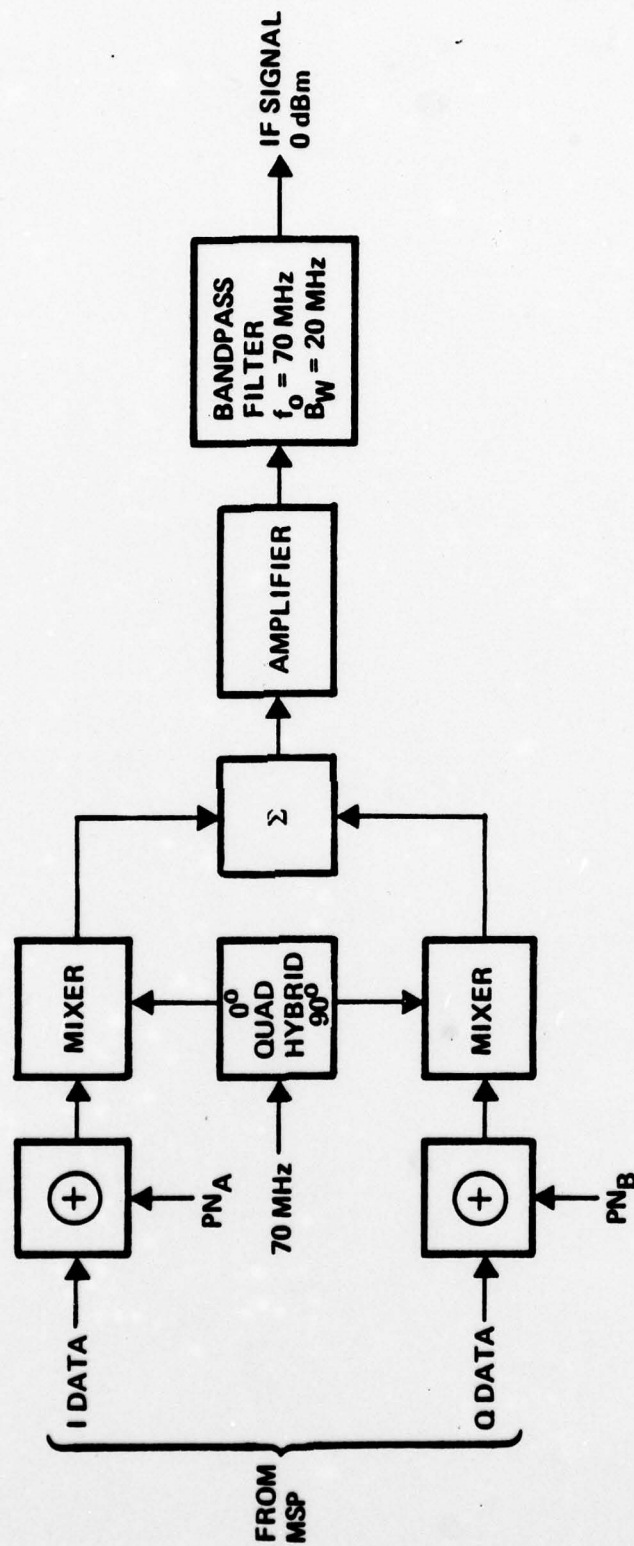


Figure 64a. Modulator Module Block Diagram

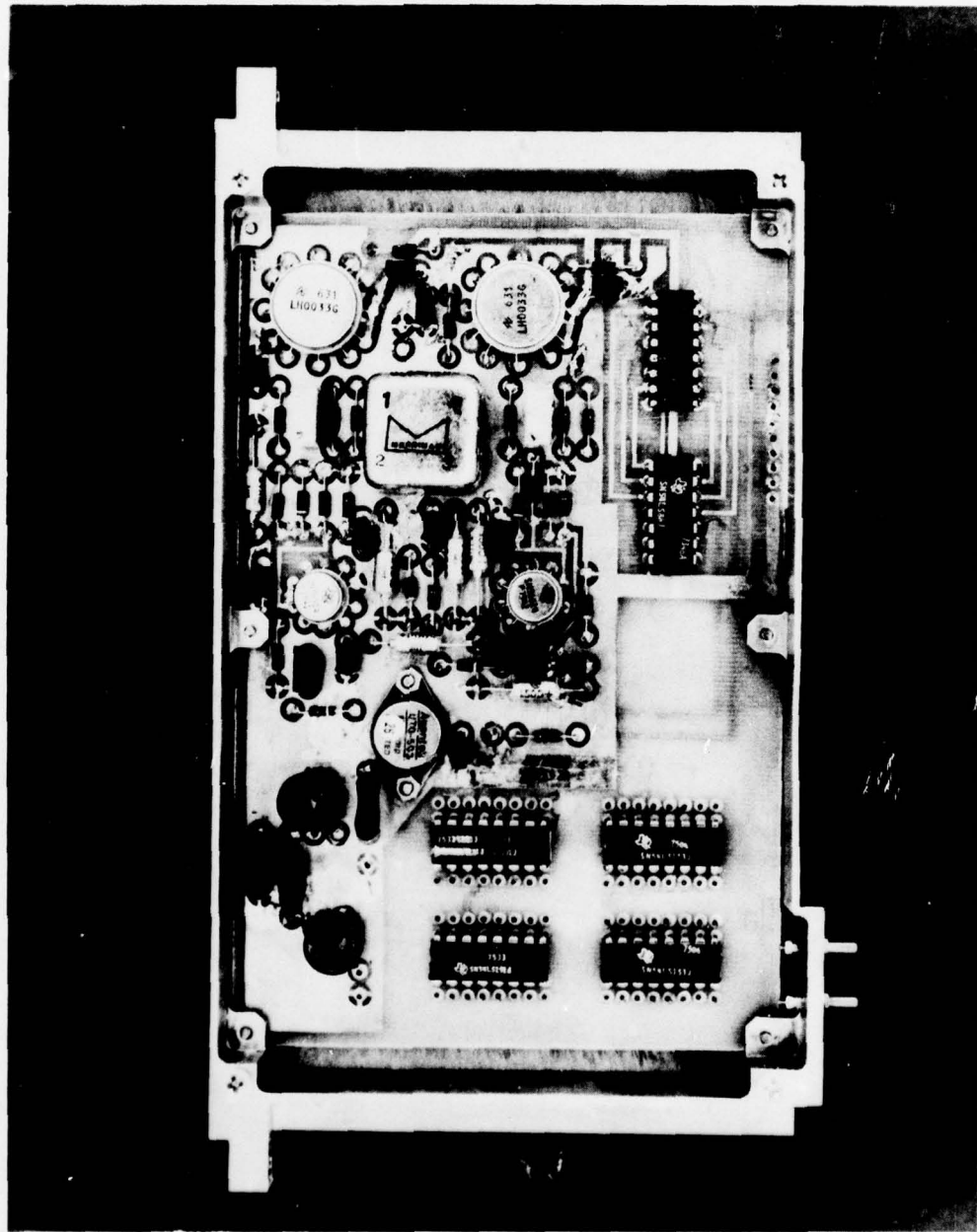


Figure 64b. Modulator Module

remove out-of-band products. Sufficient amplification is provided to bring the output level up to 0 dBm.

The mixers are linear AM modulators which would allow the generation of other forms of modulation where the input pulse is shaped, as in the JTIDS MSK modulation. Therefore, the input data pulses are half-sine shaped rather than square. A modulator specification is given in Figure 65.

3.4.8 PN Generator

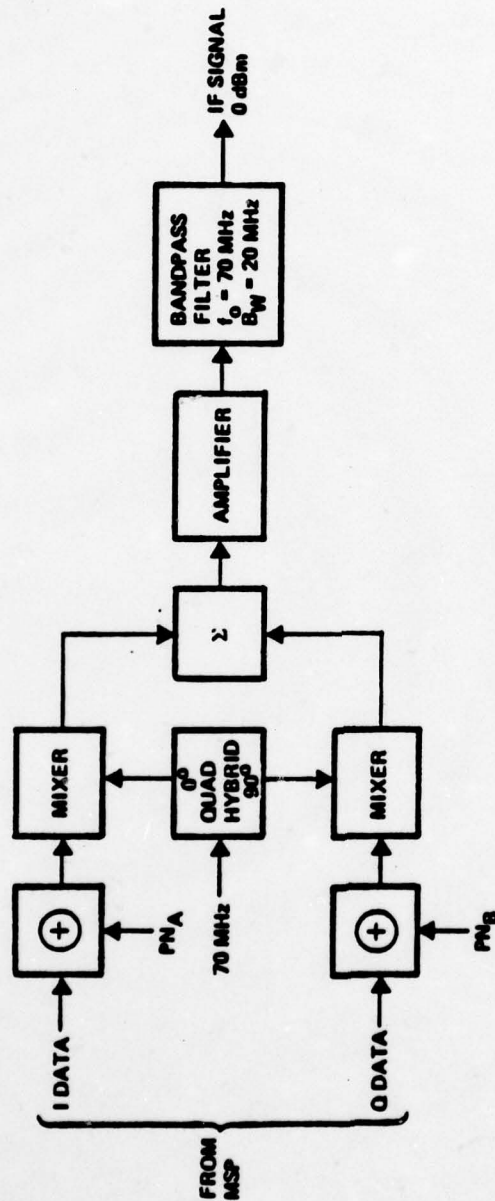
The PN Generator approach selected for the SAM terminal (Figure 66) is designed to provide a simulation of the GPS code which can also be used for the generic PSK class of waveform. For the GPS application a maximal length 1023 code is used as the C/A code and a maximal length 1023 code is used as the C/A code and a maximal length $2^{25}-1$ code is used as the P code. The latter code is also used for the generic PSK application.

The code generators, GPN and TPN, are capable of GPS operation, and generates a long code ($2^{25}-1$) and a short code ($2^{10}-1$). Data and manchester sync are derived from the short code epoch. These PN generators also have code tracking and initialization capability. The initialization mode also allows selectable code preset states. Note that there is no GPS handover capability - from the P code to the C/A code.

3.4.9 Frequency Generator

The Frequency Generator provides a set of fixed output frequencies which are coherent with a reference input frequency. The generator is constructed from basic building block submodules as shown in Figure 67a and specified in Figure 67b. Each submodule uses a VCO in a phase block configuration. The reference input is first buffered, then divided by a selectable modulus (M) to form a loop sample frequency. The VCO output frequency is divided by a selectable modulus (N) and compared with the loop sample frequency in the phase/frequency detector. The resulting error signal is filtered by the loop filter and fed to the VCO. The VCO is buffered for multiple outputs. The unique frequency for each application is realized by programming the proper divider moduli and by inserting a submodule containing a VCO with the desired frequency coverage and the proper loop filter components for the correct loop natural frequency. Because of this flexibility, this module has been designated as a standard module.

THE MODULATOR PROVIDES THE CAPABILITY TO UPCONVERT, AMPLIFY, AND FILTER TO 70 MHZ FROM QUADRIPHASE MODULATED BASEBAND DATA. THE BASEBAND (INPUT) DATA, BOTH I AND Q, IS EXCLUSIVE-ORED WITH PSEUDORANDOM (PN) SEQUENCES TO PRODUCE THE QPSK SIGNAL.



REQUIREMENTS

- ACTIVE MODULATORS SUCH AS SN56514
- CAPABLE OF ACCOMMODATING BPS, QPSK, MSK, FSK, OR AM
- PHYSICAL PARAMETERS

ONE 1/2 ATR MODULE ENCLOSURE 3/4 INCH THICK
LESS THAN 2.5 WATTS POWER DISSIPATION

Figure 65. Modulator Specification

INTERFACES

OUTPUT SIGNALS	
OUTPUT CENTER FREQUENCY	70 MHZ
OUTPUT IMPEDANCE	50 Ω
OUTPUT LEVEL	0 DBM \pm 1 DB
INPUT SIGNALS	
MODEM ADAPTER	
DATA INPUT	TTL COMPATIBLE
DATA RATE	100K BPS
TRANSMIT PN GENERATOR	
PN INPUT	TTL COMPATIBLE
PN RATE	10.23 MBPS MAX SYNCHRONOUS WITH DATA INPUT
FREQUENCY GENERATOR (TX)	
LOCAL OSCILLATOR FREQUENCY	70 MHZ
LOCAL OSCILLATOR LEVEL	+4 DBM
LOCAL OSCILLATOR INPUT IMPEDANCE	50 Ω

Figure 65. Modulator Specification (Continued)

The PN generators consists of the receive PN generator (GPN) and the transmit PN generator (TPN) using basically the same logic configuration. The difference is in the clock generator for GPS in the GPN and some additional clock buffering in the TPN.

REQUIREMENTS

- Provide the GPS PN code for the MOD (exclusive-ored) and the COR for code acquisition.
- Each will consist of two maximal length sequence generators with the following sequences: $P = X^{25} + X^{24} + 1$ and $P = X^{10} + X^7 + 1$.
- Physical parameters

GPN one 1/2 ATR card and less than 4 watts

TPN two 1/2 ATR cards and less than 5 watts

INTERFACES

INPUTS - GPN

CTL CLOCK

OUTPUTS - GPN

SPP

MSP

CTL

INPUTS - TPN

FGN Clock

OUTPUTS - TPN

MAD

MOD

MAD

10 MHz/TTL compatible

Sync pulses TTL

P, C/A epoch pulse

Code 1/2 TTL

10 MHz

C/A Code Sync Pulse, TTL

Code 1/2 TTL

Manchester Clock/Data Clock

Figure 66. PN Generator Specification

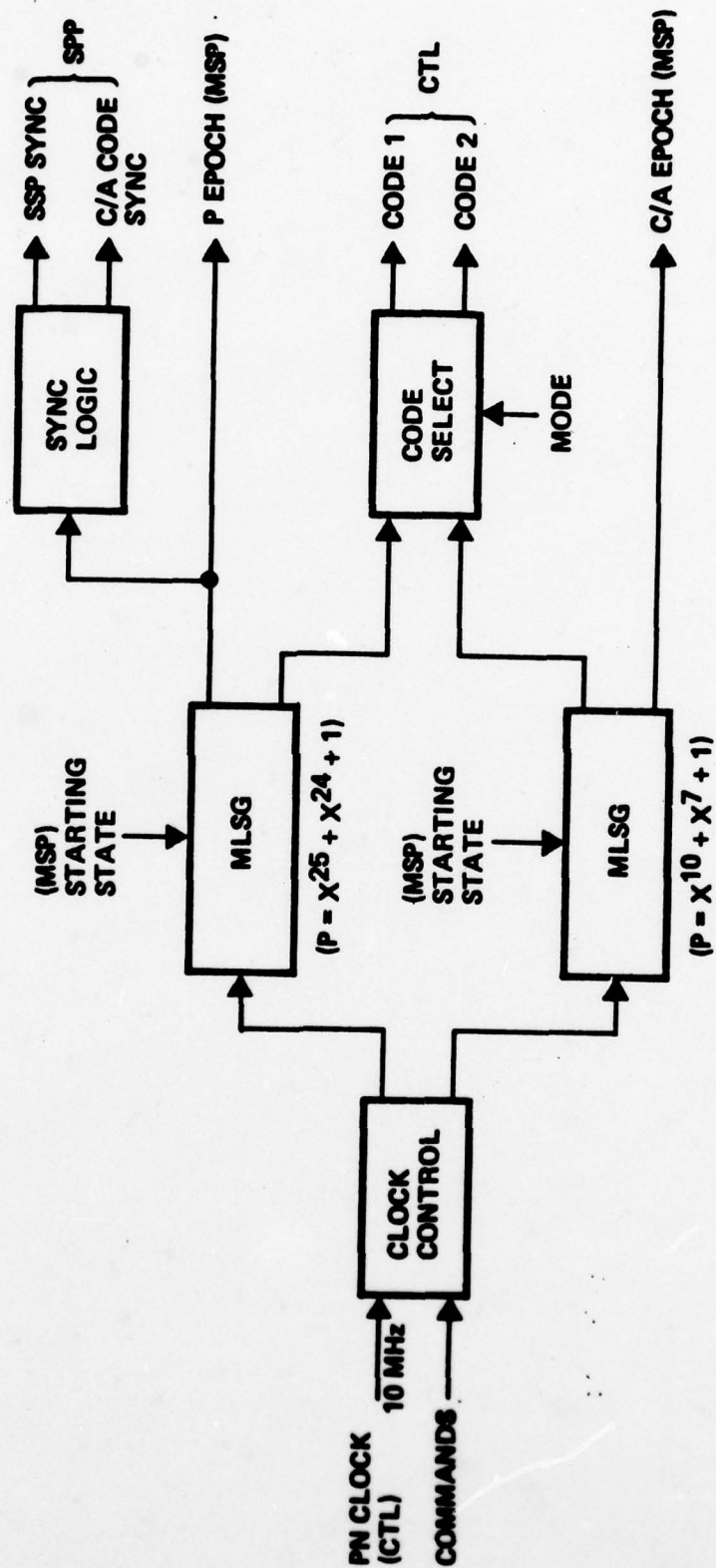


Figure 66A. Receive PN Generator (GPN) Block Diagram

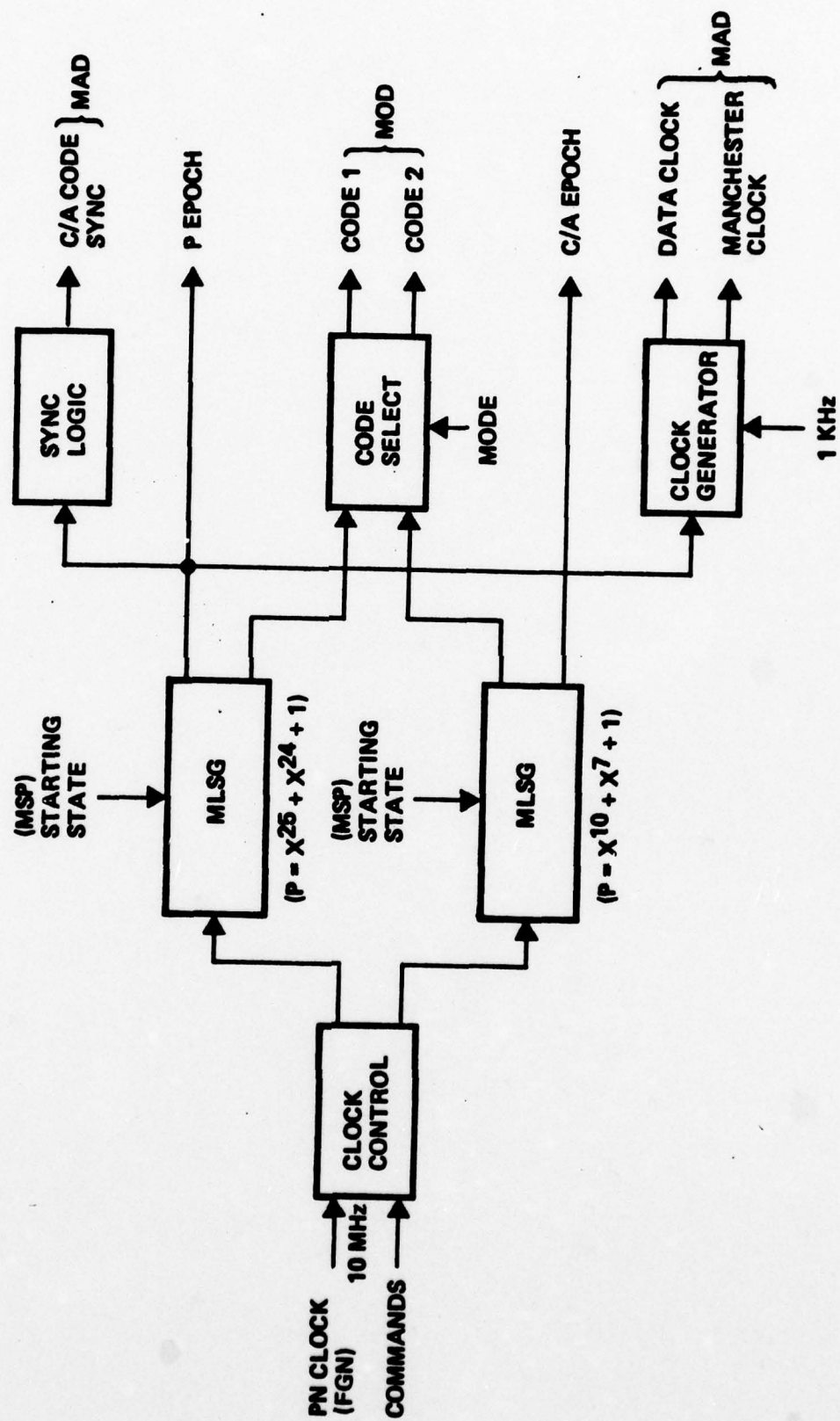


Figure 66B. Transmit PN Generator (TPN) Block Diagram

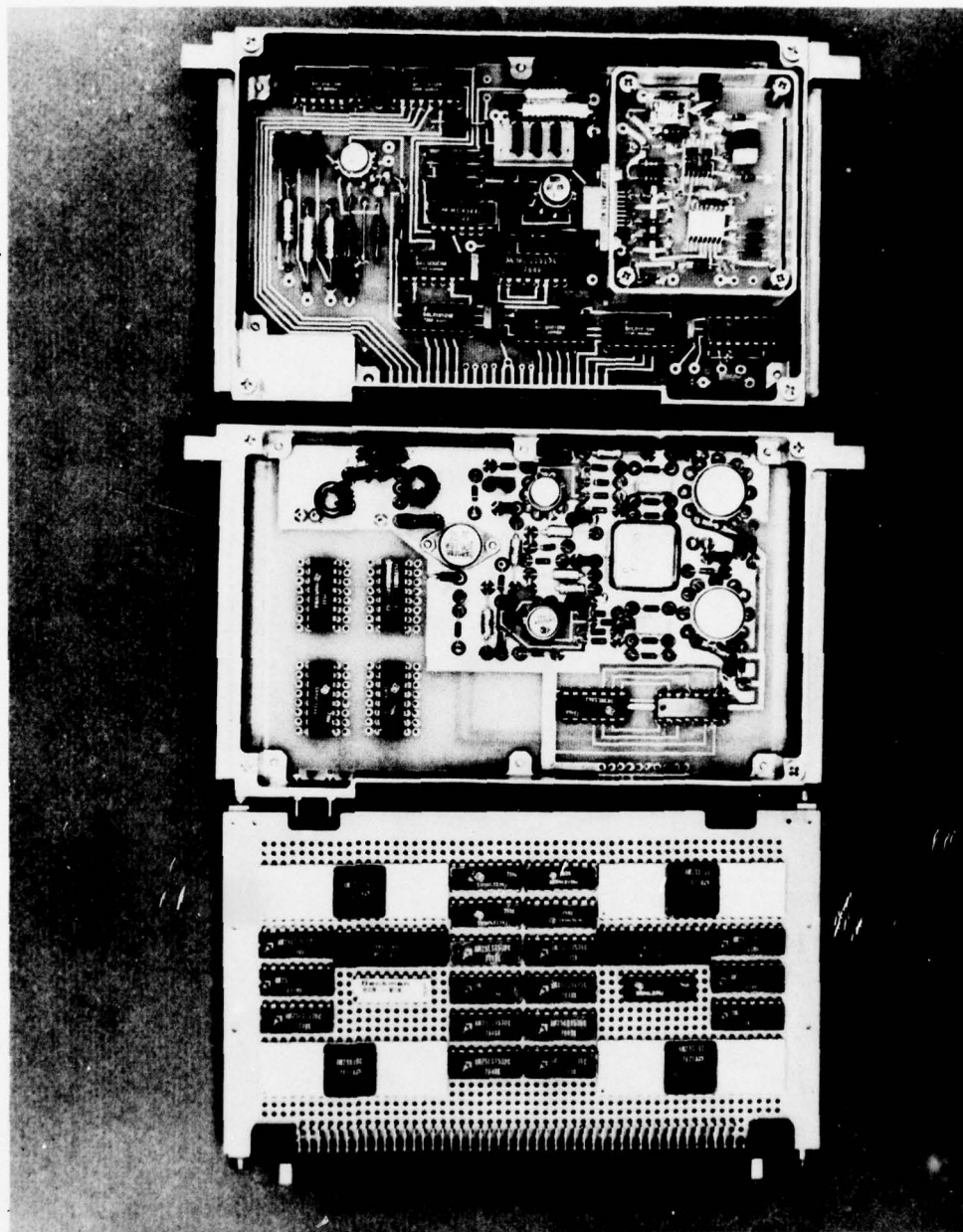


Figure 67a. Frequency Generator Submodule (Module at top of page)

OTHER REQUIREMENTS

● PROGRAMMABILITY BASED ON:

PROGRAMMABLE VCO DIVIDER
LOOP FILTER COMPONENT SELECTABLE
PLUG-IN VCO FUNCTION

● PHYSICAL PARAMETERS

SUBMODULE — ONE 1/2 ATR CARD 3/4 INCH THICK
— LESS THAN 2.5 WATTS POWER DISSIPATION
DEMODULATOR — TWO SUBMODULES
MODULATOR — TWO SUBMODULES

INTERFACES

INPUT FREQUENCY	10 MHZ (5 MHZ, 1 MHZ OPTIONAL)
INPUT LEVEL	0 +3 DBM (INTO 50 Ω) 0 DBM +3 DB
OUTPUT FREQUENCIES	81.84 MHZ/+2 +1 DBM +2 DBM +1 DB 70 MHZ/+2 +1 DBM +2 DBM +1 DB

Frequency 67b. Frequency Generator Specification (Continued)

3.4.10 Doppler Wipeoff Module

The Doppler Wipeoff Module (Figure 68) is a digital direct frequency synthesizer which generates the 70 MHz L.O. used in the A/D Converted Module to mix the IF signal down to baseband quadrature components. The input to the module is a 16-bit frequency command word from the MSP which is integrated in a 24-bit phase accumulator. The accumulator is clocked at 5 MHz, which provides a frequency resolution of 0.6 Hz. The tuning range is therefore $+0.6 \times 2^{15} = +19.7$ KHz. The phase accumulator output addresses a 1024 point ROM which contains amplitude value for a quarter cycle of a sine wave. Both the sine and cosine value of the phase are derived from this ROM and stored in 8 bit registers. These quadrature values are then converted to analog form and used to modulate quadrature 70 MHz carriers. This effectively phase modulates the 70 MHz carrier resulting in a 70 MHz L.O. which is offset in frequency by an amount determined by the input frequency command word. The advantages of this approach are that the frequency accuracy is determined by the accuracy of the clock driving the phase accumulator, and, when used in a phase-locked arrangement, a measurement of frequency is obtained directly from the frequency control word.

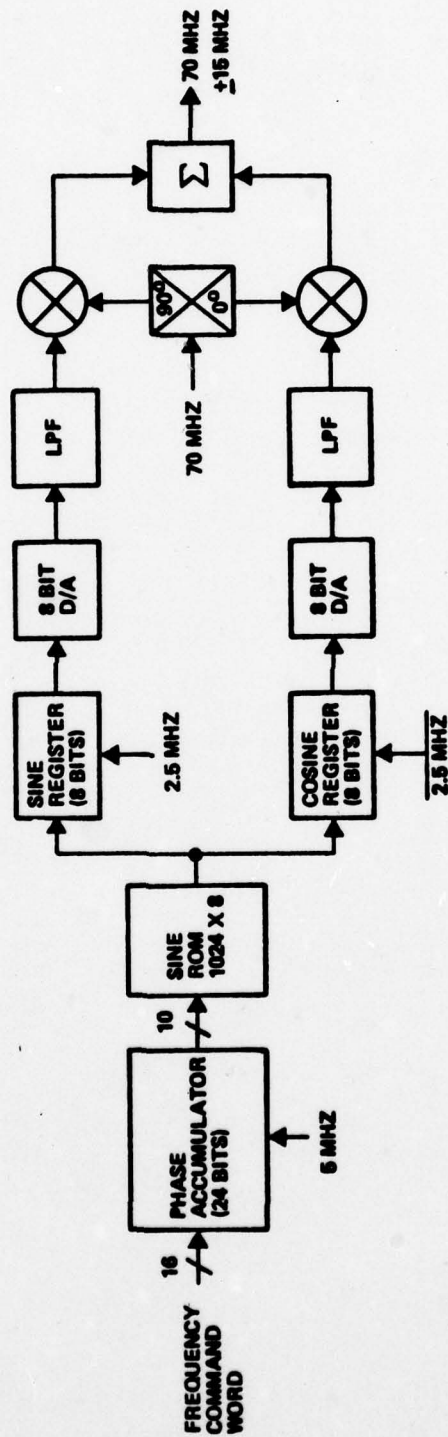


Figure 68. Doppler Wipeoff Module

The doppler wipe-off combines a direct digital synthesizer with a single sideband modulator. Its function is to remove the doppler frequency from the IF signal during the down-conversion process in the ADC module.

REQUIREMENTS

- Magnitude and direction of doppler shift controlled by a 16-bit digital command word.
- Output LO signal is 70 MHz ± 0 to 15 KHz.
- Physical parameters
 - One 1/2 ATR card enclosure 3/4 inch thick
 - Less than 3.0 watts power dissipation

INTERFACES

Input MSP	
Data	One 16-bit parallel word with coincident clock pulse
Input FGN	
Frequencies	70 MHz/ ± 2 ± 1 DBM ± 2 DBM ± 1 DB 10 MHz/TTL compatible
Output	
Frequency	70 MHz/ ± 2 ± 1 DBM ± 2 DBM ± 1 DB

Figure 68A. Doppler Wire-Off Specification

APPENDIX A
SAMPLED MSK WAVEFORM DISTORTION

If a digital processing modulator is used to generate MSK signals, the output will suffer degradation from both quantization in amplitude and time. This memo determines a measure of the degradation due to finite time quantization of the sinusoidally-shaped pulses that arise in the quadrature channels of an MSK modulator. The sampled signal is filtered to reduce the MSE (i.e. increase the signal-to-time quantization noise ratio). It is found that with only 4 samples per pulse and appropriate filtering the SNR may be as high as 21 dB.

Sampled MSK Spectrum

This section determines the spectrum of one of the sampled quadrature components of an MSK waveform.* Each sample of the waveform is held for the duration of the sampling time. The quadrature component of the continuous MSK waveform (either the inphase or the orthogonal channel) is assumed to be given by $|\sin \omega_0 t|$. The spectrum of this signal will then be the envelope of an MSK waveform with random data modulation. Figure A-1 shows the sampled signal for 4 samples per pulse. The coefficients of the Fourier series expansion of $x^S(t)$ will be the amplitudes of the frequency components of the sampled signal. The expansion is

$$x^S(t) = \frac{1}{2} a_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega_0 t + b_n \sin n\omega_0 t) \quad (A-1)$$

where

$$\begin{aligned} a_0 &= \frac{2}{T} \int_0^T x^S(t) dt \\ a_n &= \frac{2}{T} \int_0^T x^S(t) \cos(n\omega_0 t) dt, & n = 1, 2, 3, \dots \\ b_n &= \frac{2}{T} \int_0^T x^S(t) \sin(n\omega_0 t) dt, & n = 1, 2, 3, \dots \end{aligned}$$

The sampled MSK waveform may be written as

$$x^S(t) = \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \text{rect}\left(\frac{t-(k-1/2)\tau}{\tau}\right), \quad \tau = \frac{2T}{N} \quad (A-2)$$

where

$$\begin{aligned} N &= \text{Number of Samples/Pulse} \\ \text{rect}(s) &= 1 & |s| \leq \frac{1}{2} \\ &= 0 & \text{Otherwise} \end{aligned}$$

*These results are used in the mean-square-error derivation; however, they may also be useful in determining the spectral occupancy of the sampled MSK waveform.

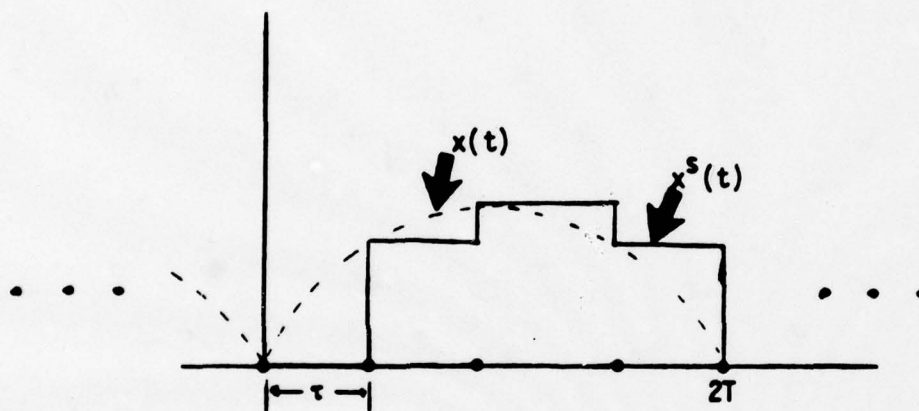


Figure A-1. Sampled MSK Pulse

The series coefficients may then be determined as

$$\begin{aligned}
 a_0^s &= \frac{1}{T} \int_0^{2T} x^s(t) dt = \frac{1}{T} \int_0^{2T} \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \cdot \text{rect}\left(\frac{t-(k-\frac{1}{2})\tau}{\tau}\right) dt \\
 &= \frac{1}{T} \sum_{k=1}^N \int_{(k-1)\tau}^{k\tau} \sin\left\{\frac{(k-1)\pi}{N}\right\} dt = \frac{1}{T} \left(\sum_{k=1}^N \tau \cdot \sin\left\{\frac{(k-1)\pi}{N}\right\} \right), \tau = \frac{2T}{N} \\
 &= \frac{2}{N} \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \quad (A-3)
 \end{aligned}$$

$$\begin{aligned}
 a_n^s &= \frac{1}{T} \int_0^{2T} x^s(t) \cos(n\omega_0 t) dt, \quad \omega_0 = 2\pi\left(\frac{1}{2T}\right) = \frac{\pi}{T} \\
 &= \frac{1}{T} \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \int_{(k-1)\tau}^{k\tau} \cos(n\omega_0 t) dt \\
 &= \frac{1}{n\pi} \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} [\sin(\frac{nk \cdot 2\pi}{N}) - \sin(\frac{n2\pi}{N} (k-1))] \quad (A-4)
 \end{aligned}$$

$$\begin{aligned}
 b_n^s &= \frac{1}{T} \int_0^{2T} x^s(t) \sin(n\omega_0 t) dt \\
 &= \frac{1}{T} \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \int_{(k-1)\tau}^{k\tau} \sin(n\omega_0 t) dt \\
 &= \frac{1}{n\pi} \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} [\cos(\frac{n2\pi}{N} (k-1)) - \cos(\frac{n2\pi}{N} k)] \quad (A-5)
 \end{aligned}$$

The waveform may also be expanded in a complex Fourier series as

$$x^s(t) = \sum_{n=-\infty}^{\infty} c_n^s e^{jn\omega_0 t} \quad (A-6)$$

where

$$c_n^s = \frac{1}{2} (a_n^s - jb_n^s) \quad (A-7)$$

MSE Derivation

An equation will be derived for the MSE of the sampled and filtered MSK waveform (one of the quadrature channels). Figure A-2 shows the case that was considered.

$$\text{MSE} = \frac{1}{2T} \int_0^{2T} [x(t) - \hat{x}(t)]^2 dt = \sum_{n=-\infty}^{\infty} |c_n'|^2 \quad (\text{A-8})$$

$$\begin{aligned} c_n' &= \frac{1}{2T} \int_0^{2T} [x(t) - \hat{x}(t)] e^{-jn\omega_0 t} dt \\ &= \frac{1}{2T} \int_0^{\pi} x(t) e^{-jn\omega_0 t} dt - \frac{1}{2T} \int_0^{2T} \hat{x}(t) e^{-jn\omega_0 t} dt \\ &= c_n - \hat{c}_n \end{aligned} \quad (\text{A-9})$$

The second equality in Equation (A-8) is a result known as Parseval's theorem. It can be shown that

$$\begin{aligned} x(t) &= \frac{-2}{\pi} \sum_{n=-\infty}^{\infty} \left(\frac{1}{4n^2-1} \right) e^{j2\pi n t} \\ \therefore c_n &= \frac{-2}{\pi} \left[\frac{1}{4n^2-1} \right] = \frac{1}{2} (a_n - jb_n) \\ \rightarrow b_n &= 0, \quad a_n = \frac{4}{\pi} \left[\frac{1}{1-4n^2} \right] \end{aligned} \quad (\text{A-10})$$

The second term in (A-9) is

$$\begin{aligned} \hat{c}_n &= c_n^s \cdot H_F^*(n) = |c_n^s| e^{j\phi_n^s} |H_F(n)| e^{-j\phi_F(n)} \\ &= |c_n^s| \cdot |H_F(n)| e^{j(\phi_n^s - \phi_F(n))} \end{aligned} \quad (\text{A-11})$$

$H_F(n)$ is the filter transfer function and is here considered to be a low-pass all pole function. Therefore

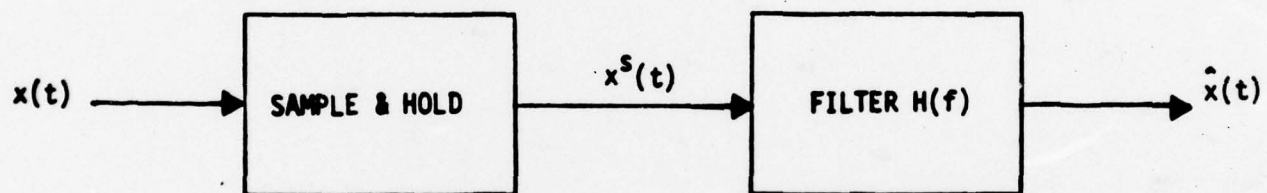


Figure A-2. MSK Distortion Model

$$|H_F(j\omega)| = \frac{K}{\prod_{i=1}^m \sqrt{\sigma_i^2 + (\omega - \omega_i)^2}} \quad (A-12)$$

$$\phi_F(j\omega) = - \sum_{i=1}^m \tan^{-1} \left(\frac{\omega - \omega_i}{-\sigma_i} \right) \quad (A-13)$$

where

$s_i = \sigma_i + j\omega_i$ are the normalized pole locations

$\omega = (\text{Normalized Freq}) = \omega(\text{Actual})/\omega(\text{Cutoff})$

$= nf_0/zf_0 = n/z$

$m = \text{Number of Filter Poles}$

Equation (A-9) becomes

$$\begin{aligned} c'_n &= c_n - |c_n^s| \cdot |H_F(n)| e^{j(\phi_n^s - \phi_F(n))} \\ &= \frac{1}{2} a_n - |c_n^s| \cdot |H_F(n)| \cos(\phi_n^s - \phi_F(n)) - j |c_n^s| \cdot |H_F(n)| \sin[\phi_n^s - \phi_F(n)] \quad (A-14) \end{aligned}$$

$$\therefore |c'_n|^2 = \frac{1}{4} a_n^2 - a_n |c_n^s| \cdot |H_F(n)| \cos[\phi_n^s - \phi_F(n)] + \{|c_n^s| \cdot |H_F(n)|\}^2$$

or

$$\begin{aligned} |c'_n|^2 &= \frac{1}{4} a_n^2 - a_n (1/2) [(a_n^s)^2 + (b_n^s)^2]^{1/2} \cdot |H_F(n)| \cos[\phi_n^s - \phi_F(n)] \\ &\quad + \frac{1}{4} \{(a_n^s)^2 + (b_n^s)^2\} \cdot |H_F(n)|^2 \quad (A-15) \end{aligned}$$

Then

$$\text{MSE} = |c'_0|^2 + 2 \sum_{n=1}^{\infty} |c'_n|^2$$

where

$$c'_0 = \frac{1}{2} a_0 - \frac{1}{2} a_0^s |H_F(0)|$$

Results

A computer program was written which evaluates Equation (16). The infinite sum is truncated and the final term is printed so that it can be made small enough to give the desired MSE accuracy. The program listing is included in the last section. The MSE vs number of samples per pulse is shown in Figure A-3. Three cases are shown: MSE without filtering, MSE with a 3-pole Butterworth filter, and MSE using a 3-pole Chebyshev filter. The figure also gives the SNR. This is defined as

$$\text{SNR} = \frac{\text{CONTINUOUS WAVEFORM ENERGY}}{\text{MEAN-SQUARE ERROR}} = \frac{0.5}{\text{MSE}}$$

The filtering was not chosen so as to minimize SNR, therefore, the curves may be interpreted as upper bounds, i.e. SNR's at least as good as there may be obtained.

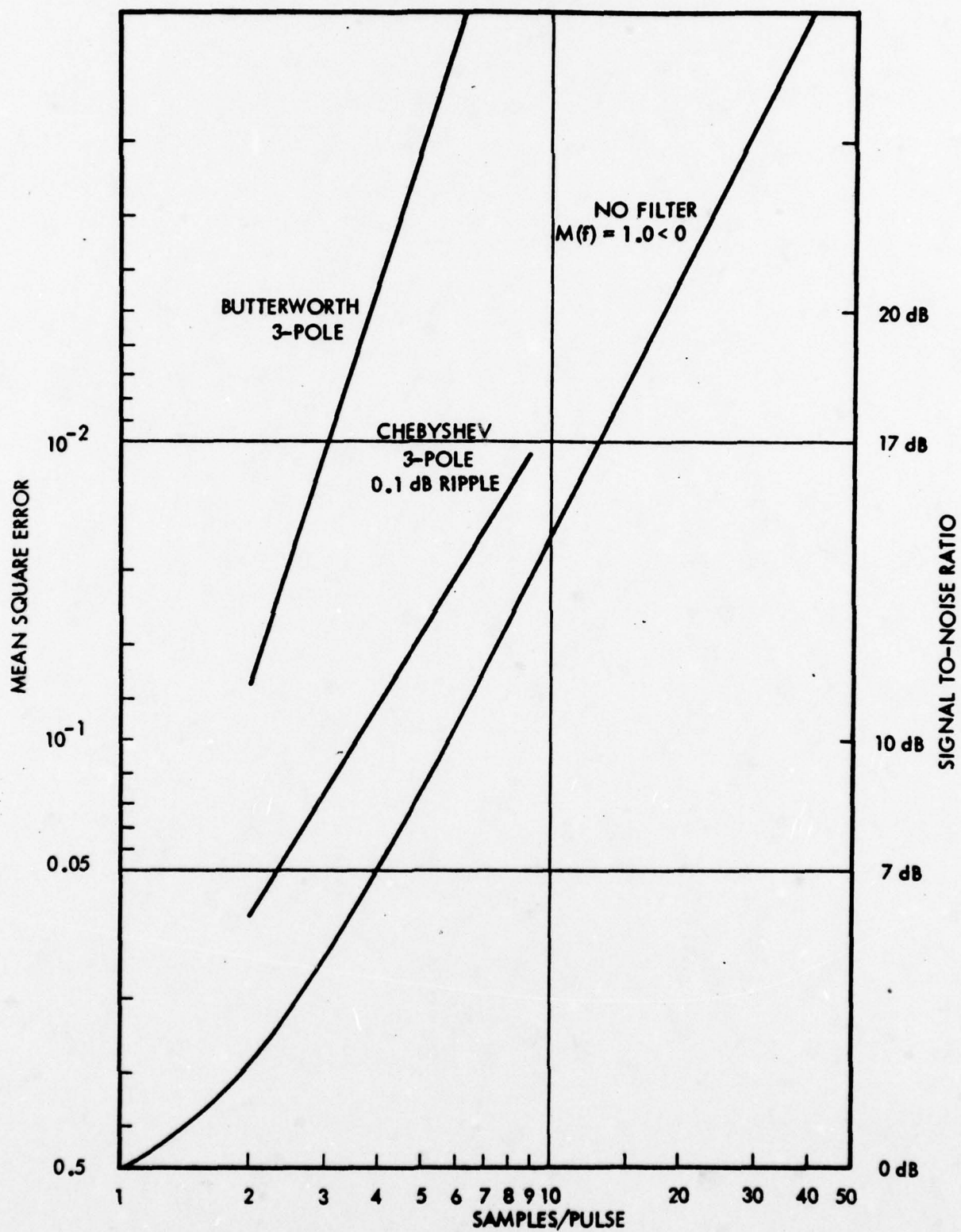


Figure A-3. MSK Waveform Distortion

APPENDIX B

DIGITAL MODULATOR

This appendix derives additional results to be used in conjunction with the analysis results given in a previous memo.* The previous memo gave an expression for MSK waveform distortion, in terms of mean square error, arising in a digital processing modulator. It was found that this MSE may be reduced by scaling and time shifting the digitally-produced MSK pulse in relation to the ideal MSK pulse. This appendix derives expressions for the optimum scale factor and time shift which will, therefore, insure that the MSE is a meaningful measure of distortion.

Using these results, it was found that the ideal signal power-to-distortion power ratio (SNR) after filtering with a 3 pole Butterworth was increased from 11 dB to 17 dB at 2 samples/pulse and 21 dB to 21.5 dB at 4 samples/pulse and the improvement was negligible at greater sampling rates.

*Campbell, M. R., "Sampled MSK Waveform Distortion," TRW Memo 76-7131.53-13
October 11, 1976.

MINIMUM MEAN SQUARE ERROR

In order for mean square error to be used as a measure of waveform distortion, the error should be minimized with respect to amplitude scaling and constant time delay. These two parameters will result in a mean square error; however, in a communication system, they are not error sources. This analysis determines the relative amplitude scale factor and relative time delay between the continuous MSK pulse and its discrete version (output of sample and hold device) which give minimum mean square error (MMSE).

The MSK pulse and its sampled approximation are shown in Figure B-1.

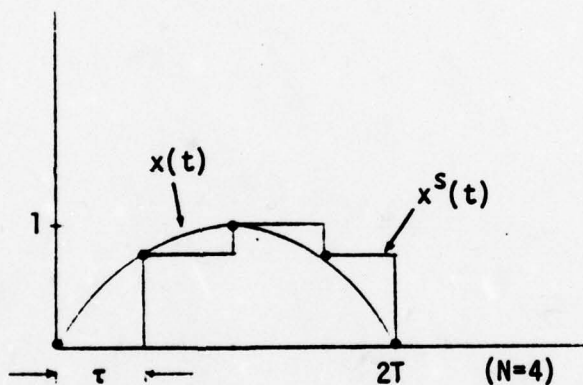


Figure B-1. MSK Pulse

The scaled and delayed version are shown in Figure B-2.

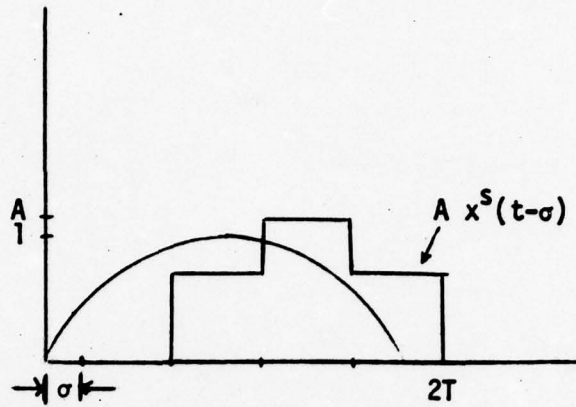


Figure B-2. Scaled and Delayed MSK Pulse

These waveforms may be expressed as

$$x(t) = \sin \frac{\pi}{2T} t \quad t \in (0, 2T) \quad (B-1)$$

$$x^S(t) = \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \cdot \text{rect}\left(\frac{t-(k-1/2)\tau}{\tau}\right)^* \quad t \in (0, 2T) \quad (B-2)$$

$$A x^S(t-\sigma) = A \sum_{k=1}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \text{rect}\left(\frac{t-\sigma-(k-1/2)\tau}{\tau}\right) \quad t \in (\sigma, 2T+\sigma) \quad (B-3)$$

where

$$\tau = \frac{2T}{N}, \quad N = \text{No. Samples/Pulse}$$

and are considered to be zero outside of the intervals given. The MSE is defined as

$$\begin{aligned} \text{MSE}(A, \sigma) &= \frac{1}{2T} \int_0^{2T} [x(t) - A x^S(t-\sigma)]^2 dt \\ &= \frac{1}{2T} \int_0^{2T} \{[x(t)]^2 - 2A x(t) x^S(t-\sigma) \\ &\quad + A^2 [x^S(t-\sigma)]^2\} dt \end{aligned} \quad (B-4)$$

*This is defined as $\text{rect}(s) = 1 \quad |s| \leq \frac{1}{2}$
 $= 0$ otherwise

The minimum mean square error is

$$\text{MMSE} = \min_{A, \sigma} (\text{MSE} (A, \sigma)) \quad (\text{B-5})$$

and is found by setting

$$\frac{\partial}{\partial A} \text{MSE} (A, \sigma) = 0 \quad \text{and} \quad \frac{\partial}{\partial \sigma} \text{MSE} (A, \sigma) = 0 \quad (\text{B-6})$$

and solving for A and σ .

$$\therefore \frac{\partial}{\partial A} \text{MSE} (A, \sigma) = \frac{1}{2T} \int_0^{2T} -2x(t) x^S(t-\sigma) dt + \frac{1}{2T} \int_0^{2T} 2A[x^S(t-\sigma)]^2 dt = 0$$

$$\rightarrow A = \frac{\int_0^{2T} x(t) x^S(t-\sigma) dt}{\int_0^{2T} [x^S(t-\sigma)]^2 dt} \triangleq \frac{B}{C} \quad (\text{B-7})$$

Note that for large N, $x^S(t-\sigma) \approx x(t)$ and $A \rightarrow 1$. Expressions for the numerator, B, and denominator, C, of Equation (B-7) will be formed. Using Equations (B-1) and B-3 gives

$$\begin{aligned} B &= \int_{\tau+\sigma}^{2T+\sigma} \sin\left(\frac{\pi}{2T} t\right) \sum_{k=1}^N \sin \frac{(k-1)\pi}{N} \cdot \text{rect}\left(\frac{t-\sigma-(k-1/2)\tau}{\tau}\right) dt \\ &= \sum_{k=2}^N \sin\left(\frac{\pi}{2T} t\right) \int_{(k-1)\tau+\sigma}^{k\tau+\sigma} \sin\left(\frac{\pi}{2T} t\right) dt \\ &= \frac{2T}{\pi} \sum_{k=2}^N \sin\left\{\frac{(k-1)\pi}{N}\right\} \left\{\cos\left((k-1)\frac{\pi}{N} + \frac{\sigma\pi}{2T}\right) - \cos\left(\frac{k\pi}{N} + \frac{\sigma\pi}{2T}\right)\right\} \quad (\text{B-8}) \end{aligned}$$

This equation was derived assuming the optimum σ must be ≤ 0 . Likewise,

$$\begin{aligned}
C &= \int_{\tau+\sigma}^{2T+\sigma} [x^s(t-\sigma)]^2 dt = \int_{\sigma+\tau}^{2T+\sigma} \left\{ \sum_{k=1}^N \sin\left(\frac{(k-1)\pi}{N}\right) \cdot \sqrt{\left(\frac{t-\sigma-(k-1/2)\tau}{\tau}\right)} \right\}^2 dt \\
&= \int_{\tau+\sigma}^{2T+\sigma} \sum_{k=1}^N \sin^2\left(\frac{(k-1)\pi}{N}\right) \cdot \sqrt{\left(\frac{t-\sigma-(k-1/2)\tau}{\tau}\right)} dt \\
&= \sum_{k=2}^N \sin^2 \frac{(k-1)\pi}{N} \int_{(k-1)\tau+\sigma}^{k\tau+\sigma} dt = \frac{2T}{N} \sum_{k=2}^N \sin^2 \frac{(k-1)\pi}{N} \quad (B-9)
\end{aligned}$$

$$\therefore A = \frac{N}{\pi} \frac{\sum_{k=2}^N \sin\left(\frac{(k-1)\pi}{N}\right) \left\{ \cos\left(\frac{(k-1)\pi}{N} + \frac{\sigma\pi}{2T}\right) - \cos\left(\frac{k\pi}{N} + \frac{\sigma\pi}{2T}\right) \right\}}{\sum_{k=2}^N \sin^2 \frac{(k-1)\pi}{N}} \quad (B-10)$$

Now solving for σ :

$$\frac{\partial}{\partial \sigma} \text{MSE}(A, \sigma) = \frac{\partial}{\partial \sigma} \left\{ \frac{1}{2T} \int_0^{2T} -2A x(t) x^s(t-\sigma) dt + \frac{\partial}{\partial T} \left\{ \frac{1}{2T} \int_0^{2T} A^2 [x^s(t-\sigma)]^2 dt \right\} \right\} \quad (B-11)$$

Using the result in Equation (B-8), the first partial derivative becomes

$$\frac{A}{T} \sum_{k=2}^N \sin\left(\frac{(k-1)\pi}{N}\right) \left\{ \sin\left(\frac{(k-1)\pi}{N} + \frac{\sigma\pi}{2T}\right) - \sin\left(\frac{k\pi}{N} + \frac{\sigma\pi}{2T}\right) \right\} \quad (B-12)$$

Using the result in Equation (B-9), the second partial derivative becomes

$$\frac{\partial}{\partial \sigma} \frac{1}{2T} \int_0^{2T} A^2 [x^s(t-\sigma)]^2 dt = \frac{A^2}{N} \frac{\partial}{\partial \sigma} \sum_{k=2}^N \sin^2 \frac{(k-1)\pi}{N} = 0 \quad (B-13)$$

\therefore Solve

$$\sum_{k=2}^N \sin\left(\frac{(k-1)\pi}{N}\right) \left\{ \sin\left[\frac{(k-1)\pi}{N} + \frac{\sigma\pi}{2T}\right] - \sin\left[\frac{k\pi}{N} + \frac{\sigma\pi}{2T}\right] \right\} = 0 \quad (B-14)$$

for σ . This will be the delay which gives the MMSE.

Solving the equation for $N=2$ gives $\sigma = -\frac{T}{2}$ and for $N=3$ gives $\sigma = -\frac{T}{3}$. It is, therefore, surmised that the optimum σ is $\sigma = -\frac{T}{N}$, i.e., $\sigma = -\frac{1}{2}\tau$. This solution will be verified.

Letting $\sigma = -\frac{T}{N}$ in Equation (B-14) gives

$$\begin{aligned}
 & \sum_{k=2}^N \sin \frac{(k-1)\pi}{N} [\sin(\frac{\pi}{N} (k - \frac{3}{2})) - \sin(\frac{\pi}{N} (k - \frac{1}{2}))] \\
 &= - \sum_{k=2}^N \sin(\frac{\pi}{2N}) \sin(\frac{2\pi}{N} (k-1)) \\
 &= - \sin(\frac{\pi}{2N}) \sum_{k=2}^N \sin(\frac{2\pi}{N} k - \frac{2\pi}{N}) \tag{B-15}
 \end{aligned}$$

Using

$$\sum_{k=0}^N \sin(ak + b) = \frac{\sin(\frac{N+1}{2} a) \sin(\frac{N}{2} a + b)}{\sin \frac{a}{2}}$$

gives

$$\begin{aligned}
 \sum_{k=2}^N \sin(\frac{2\pi}{N} k - \frac{2\pi}{N}) &= \frac{\sin(\pi + \frac{\pi}{N}) \sin(\pi - \frac{2\pi}{N})}{\sin \frac{\pi}{N}} + \sin(\frac{2\pi}{N}) \\
 &= \frac{-\sin \frac{\pi}{N} \sin(\frac{2\pi}{N})}{\sin \frac{\pi}{N}} + \sin(\frac{2\pi}{N}) \\
 &= 0
 \end{aligned}$$

Therefore, Equation (B-15) = 0, and Equation (B-14) is satisfied for $\sigma = -\frac{1}{2}\tau$.

Summarizing, the MMSE between $x(t)$ and $A x(t-\sigma)$ is obtained by setting A equal to the value given by Equation (B-10) and $\sigma = -\frac{1}{2}\tau$.

APPENDIX C
QUANTIZATION AND DITHERING FOR DIGITAL
CORRELATION RECEIVERS

ABSTRACT

Various analysis results exist which give the performance of digital receivers that use quantization (in an analog-to-digital convertor) and dithering. This memo describes the analyses, summarizes the results and shows the relationship between the different techniques. The main purpose here is to determine design requirements for the SAM receiver; however, the results apply to all receivers of the same general form. The following sections are included:

- I. Introduction
- II. Quantization and Gaussian Noise
- III. Quantization Noise and the NPR
- IV. Quantization and Non-Gaussian Interference
- V. Effects of Dither
- VI. Conclusions

LIST OF FIGURES

- C-1. Non-Coherent M-ary Digital Processing Demodulator
- C-2. Hardlimiting Quantizer Characteristic Even Number $2b$ of Intervals
- C-3. Deadzone Quantizer Characteristics Odd Number $2b-1$ of Intervals
- C-4. General Four Lever Quantizer Characteristic
- C-5. Quantization Loss vs. Normalized Threshold (in Gaussian Noise)
- C-6. Optimum Normalized Threshold vs. Number of Quantization Intervals (in Gaussian Noise)
- C-7. Minimum Quantization Loss vs. Number of Intervals (in Gaussian Noise)
- C-8. Minimum Quantization Loss vs. Number of Bits (in Gaussian Noise)
- C-9. Loss (L) in Output SNR for Four-Level Quantized DMF in (Strong) Additive Gaussian Noise as a Function of Upper-Lower Quantizer Output Level Breakpoint for Various Values of the Lower Quantizer Level k
- C-10. NPR Variation Versus Loading and Bits/Sample (N)
- C-11. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 0.001$)
- C-12. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 0.01$)
- C-13. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 1$)
- C-14. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 100$)
- C-15. $(S/N)_0$ of a Polarity Coincidence Detector with Uniformly Distributed Dither Divided by $(S/N)_0$ of a Classical Correlator as a Function of g , for Small Signal Power
- C-16. SNR Loss for Triangle Dither with Hardlimiting A-D

I. INTRODUCTION

The optimum receiver for M possible transmitted signals with additive Gaussian noise interference passes the received signal through M matched filters, each matched to one of the transmitted waveforms, and chooses as the detected waveform the one corresponding to the largest matched filter output. This gives maximum SNR and, therefore, minimum probability of error. Equivalently, the receiver may correlate the received signal with replicas of the transmitted waveforms. An analog processing receiver performs this using analog multipliers and integrators. A digital processing receiver performs the same function using digital correlators composed of shift registers and binary adders. This demodulator requires an analog-to-digital converter to sample and amplitude quantize the signals. The demodulator to be considered is shown in Figure C-1. A non-coherent carrier reference is assumed. The performance of this receiver in noise will be degraded over that of the linear matched filter receiver (or analog correlator) due to aliasing and quantization.* It will be assumed that the sampling rate is chosen large enough so that aliasing is negligible. Three quantizers will be considered in this report. They are the hardlimiting quantizer which has an even number of output levels, the deadzone quantizer with an odd number of levels, and a generalized four level quantizer. These are shown in Figures C-2 through C-4. It is of interest to know the output SNR degradation as a function of the number of quantization levels. Section II describes these results and Section III compares the results with standard curves which give ADC noise power ratios (NPR).

*The ADC will add additional distortion due to sampling time jitter and quantization level tolerances but these effects depend on system implementation and can usually be made negligible.

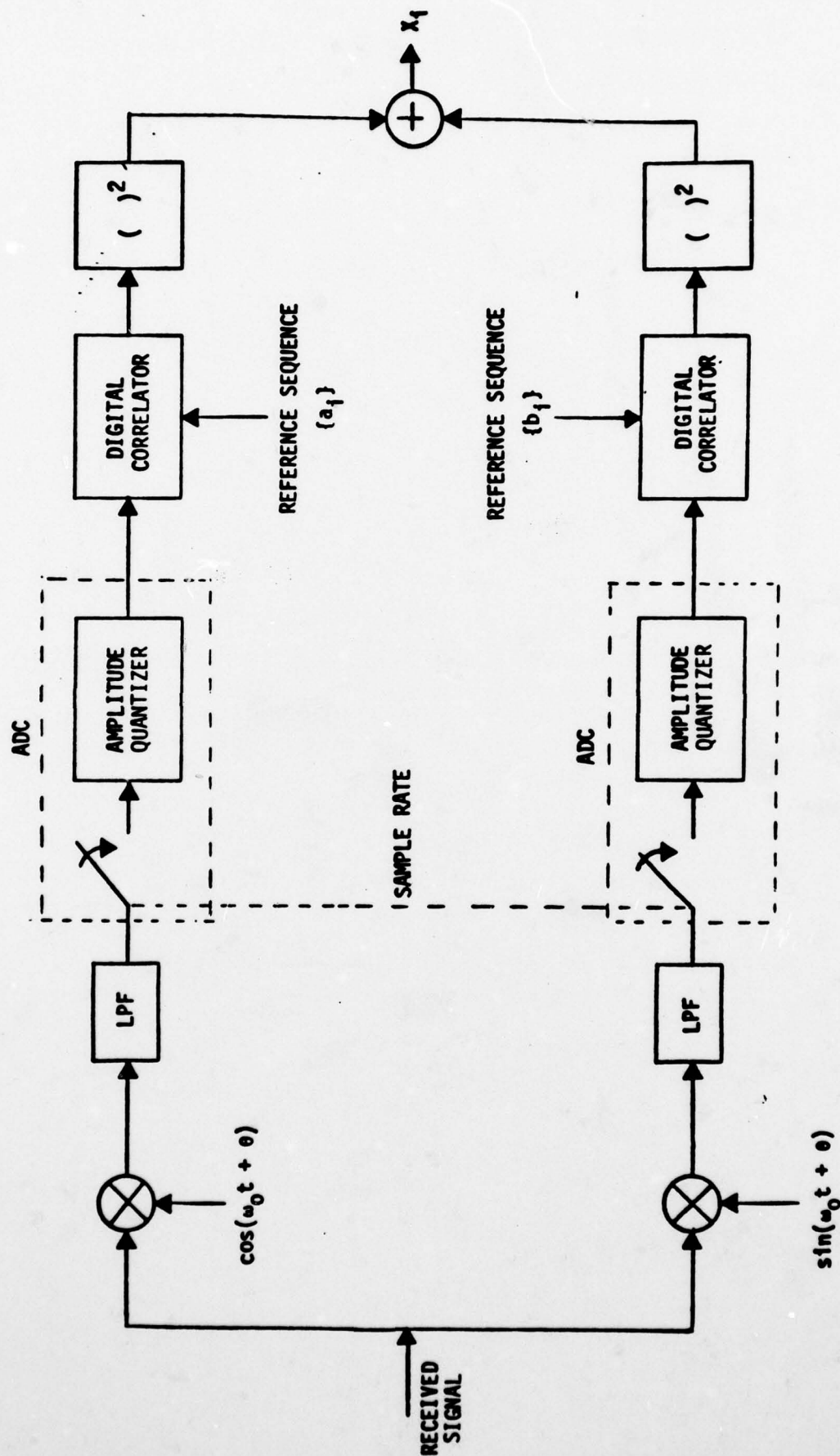


Figure C-1. Non-Coherent M-ary Digital Processing Demodulator

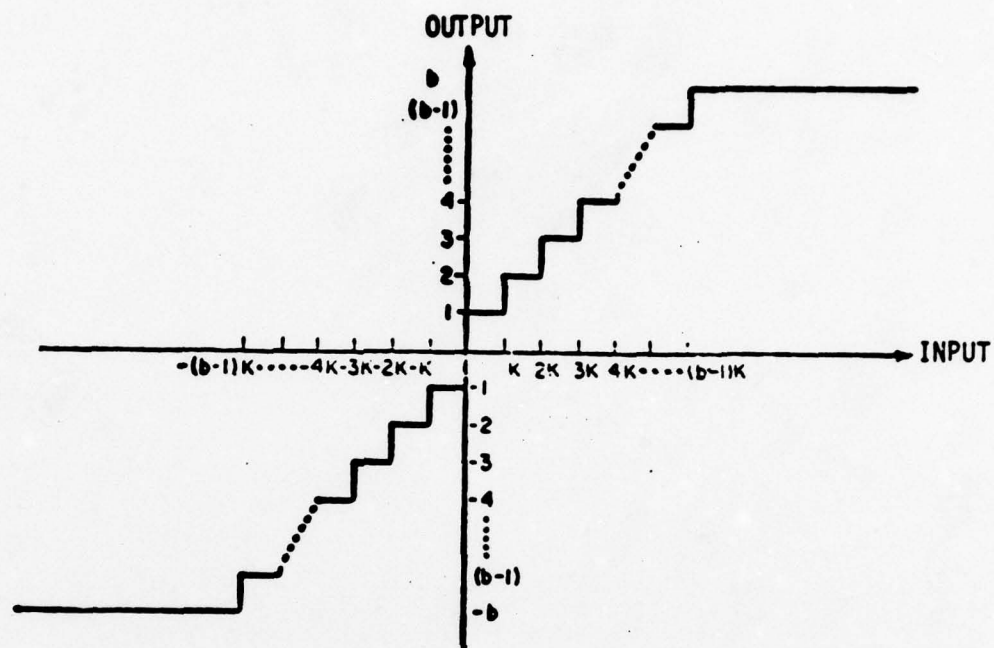


Figure C-2. Hardlimiting Quantizer Characteristic
Even Number $2b$ of Intervals

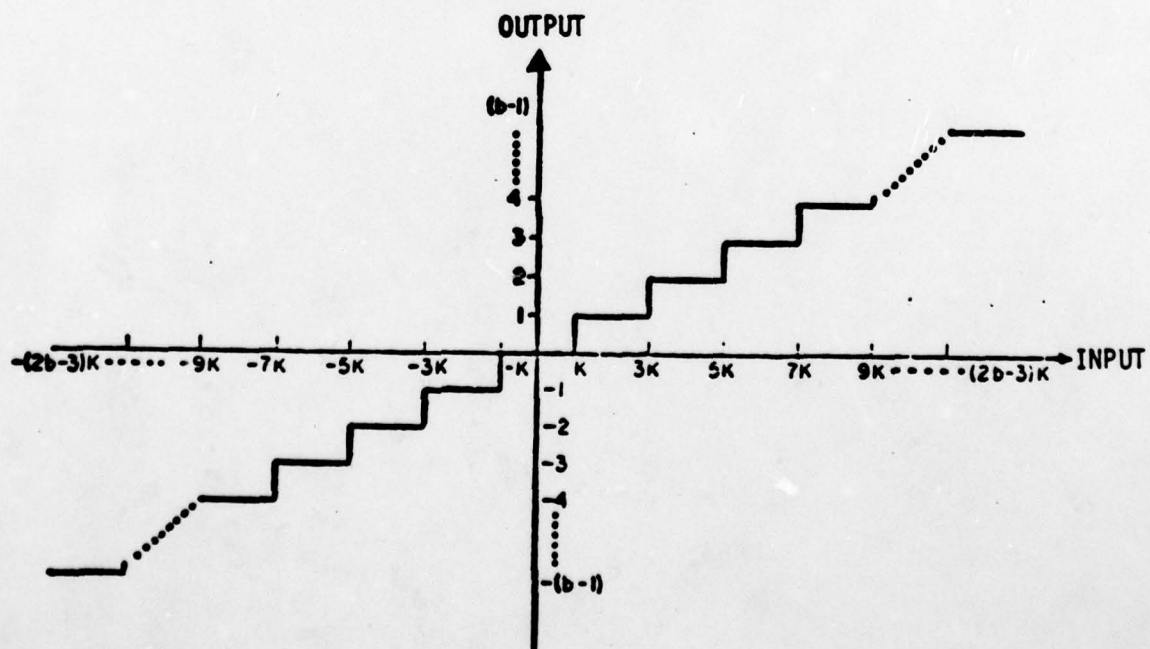


Figure C-3. Deadzone Quantizer Characteristics
Odd Number $2b-1$ of Intervals

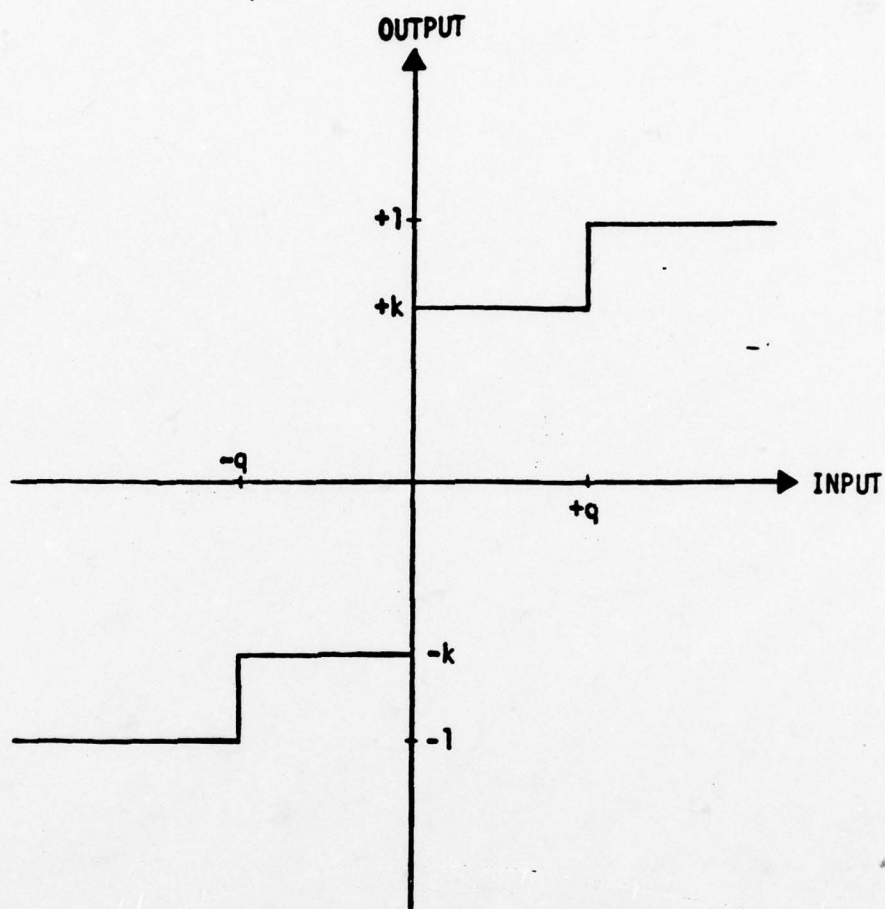


Figure C-4. General Four Level Quantizer Characteristic

It is also desired to know the performance of the digital receiver in a jamming environment. These results are given for the general four level quantizer in Section IV. A dither waveform may be used to improve performance and a description of the results is included in Section V.

II. QUANTIZATION AND GAUSSIAN NOISE

The signal-to-noise ratio at the output of the receiver is

$$\text{SNR} = \frac{[E(x_i)]^2}{\text{var}(x_i)} \quad (\text{C-1})$$

and for an ideal receiver matched to n symbols (chips) $\text{SNR}_0 = n(\text{SNR}_i)$ where SNR_i is the input SNR. The variable x_i in Equation (C-2) is the receiver's output decision variable. The loss due to quantization of the received signal is defined as

$$L = \frac{\text{SNR}_Q}{\text{SNR}_0} \quad (\text{C-2})$$

where SNR_Q is the output SNR for the digital receiver. Reference 1 determines the loss by analyzing the statistics of the receiver output. It is shown that the same loss function may be used for both coherent and noncoherent receiver processing. The results are

$$L_{2b}(\frac{K}{\sqrt{2}}) = \frac{2 \left[\sum_{t=0}^{b-1} \phi(\frac{K}{\sqrt{2}} t) \right]^2}{\sum_{t=0}^{b-1} (2t+1) [1 - \phi(\frac{K}{\sqrt{2}})]} \quad (\text{C-3})$$

$$L_{2b-1}(\frac{K}{\sqrt{2}}) = \frac{2 \left[\sum_{t=1}^{b-1} \phi[\frac{K}{\sqrt{2}} (2t-1)] \right]^2}{\sum_{t=1}^{b-1} (2t-1) [1 - \phi(\frac{K}{\sqrt{2}} (2t-1))]} \quad (\text{C-4})$$

where $\phi(t)$ and $\Phi(t)$ are the standardized normal probability density and distribution functions*, respectively, and K and b are defined in Figures C-2 and C-3. Equation (C-3) is for the hardlimiting quantizer and Eq. (C-4) is for the

$$* \phi(x) = \frac{1}{\sqrt{2\pi}} e^{-x^2/2}, \quad \Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^x e^{-u^2/2} du$$

deadzone quantizer. These equations were derived assuming a large number, $2B$, of time quantized samples and small SNR_i . The first assumption allows the sum of multinomial random variables to be approximated by a Gaussian density. This is a fairly good assumption for the signal structures under consideration. The small SNR_i condition allows the equations to be simplified to the forms given. The loss in output SNR may be minimized by finding the value of the quantizer boundary constant, K , which maximizes $L_r(\frac{K}{\sqrt{N}})$ for a given number of levels, $r = 2b$ or $2b-1$ and noise power N .

Figure C-5 shows the quantization loss function in dB for several values of r . Even values of r are for the hardlimiting quantizer and odd values for the deadzone quantizer. In the two level case, Eq. (C-3) reduces to $2/\pi = 2.0$ dB and for small K/\sqrt{N} , the loss approaches $2/\pi$ for both even and odd r . It can also be verified that for fixed b and N , L_{2b-1} approaches zero, i.e., a total loss, as K increases whereas L_{2b} approaches $2/\pi$ as K increases. That is, even for large K the hardlimiting quantizer still retains polarity information. Figure C-6 gives the optimum value of K/\sqrt{N} versus the number of quantization intervals. Figure C-7 gives the quantization loss when the optimum K/\sqrt{N} is used. In a digital correlation receiver, the quantized samples are encoded into binary digits and in order for this to be done in the simplest manner, quantizers of only certain numbers of levels should be used. The number of bits, from 2 to 5, corresponding to these levels are given on the abscissa of the graph shown in Figure C-6. For a fixed number of bits, it can be determined from Figure C-7 whether an even or odd r should be used. However, above 16 levels the difference is negligible. Figure C-8 gives the loss versus number of bits and also shows the best quantizer to use. Using a 2-bit quantizer instead of a 1-bit (2 level) hardlimiter quantizer reduces the loss by 1.22 dB. The improvement drops off quickly as the number of bits is increased above 3.

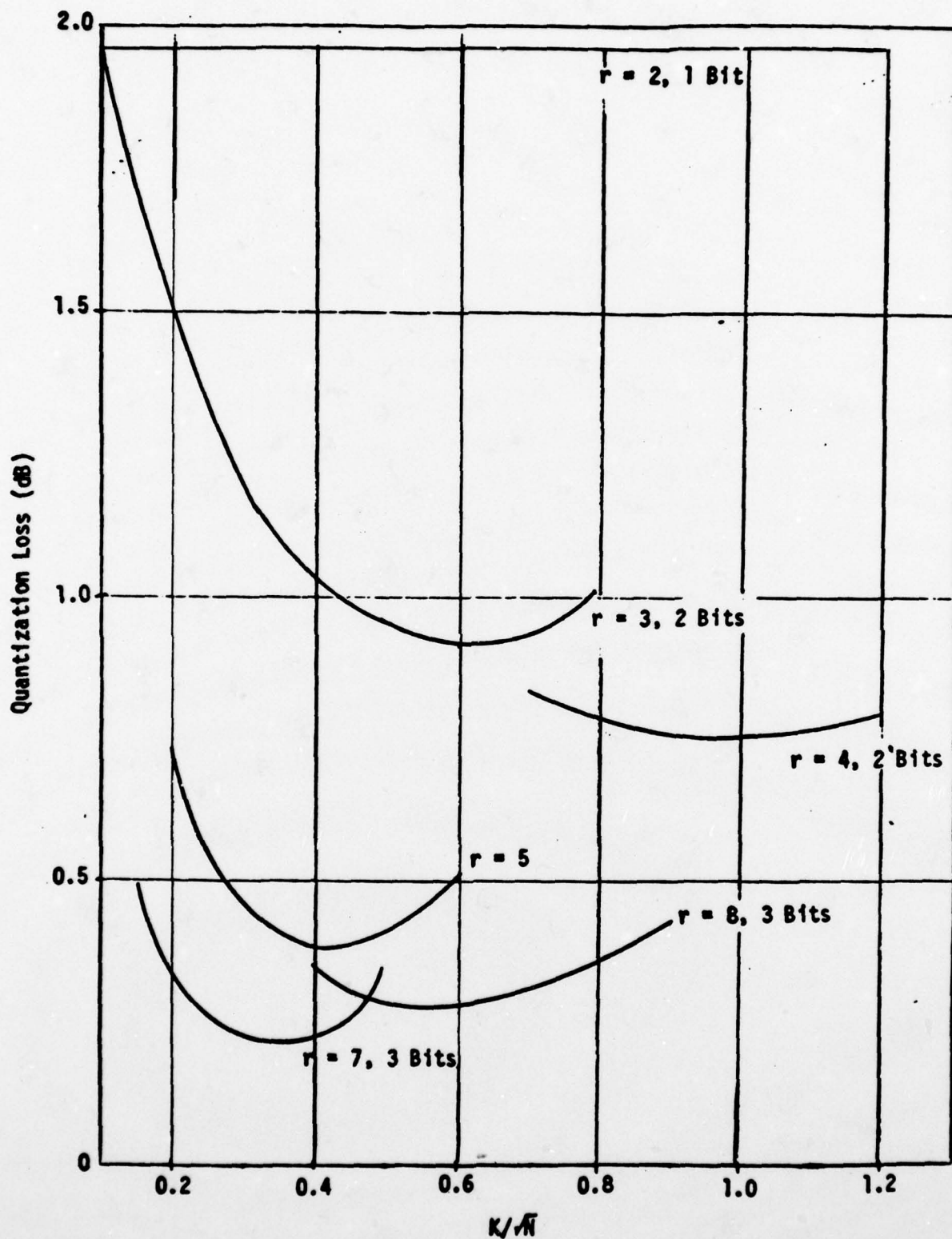


Figure C-5. Quantization Loss vs Normalized Threshold
(in Gaussian Noise)

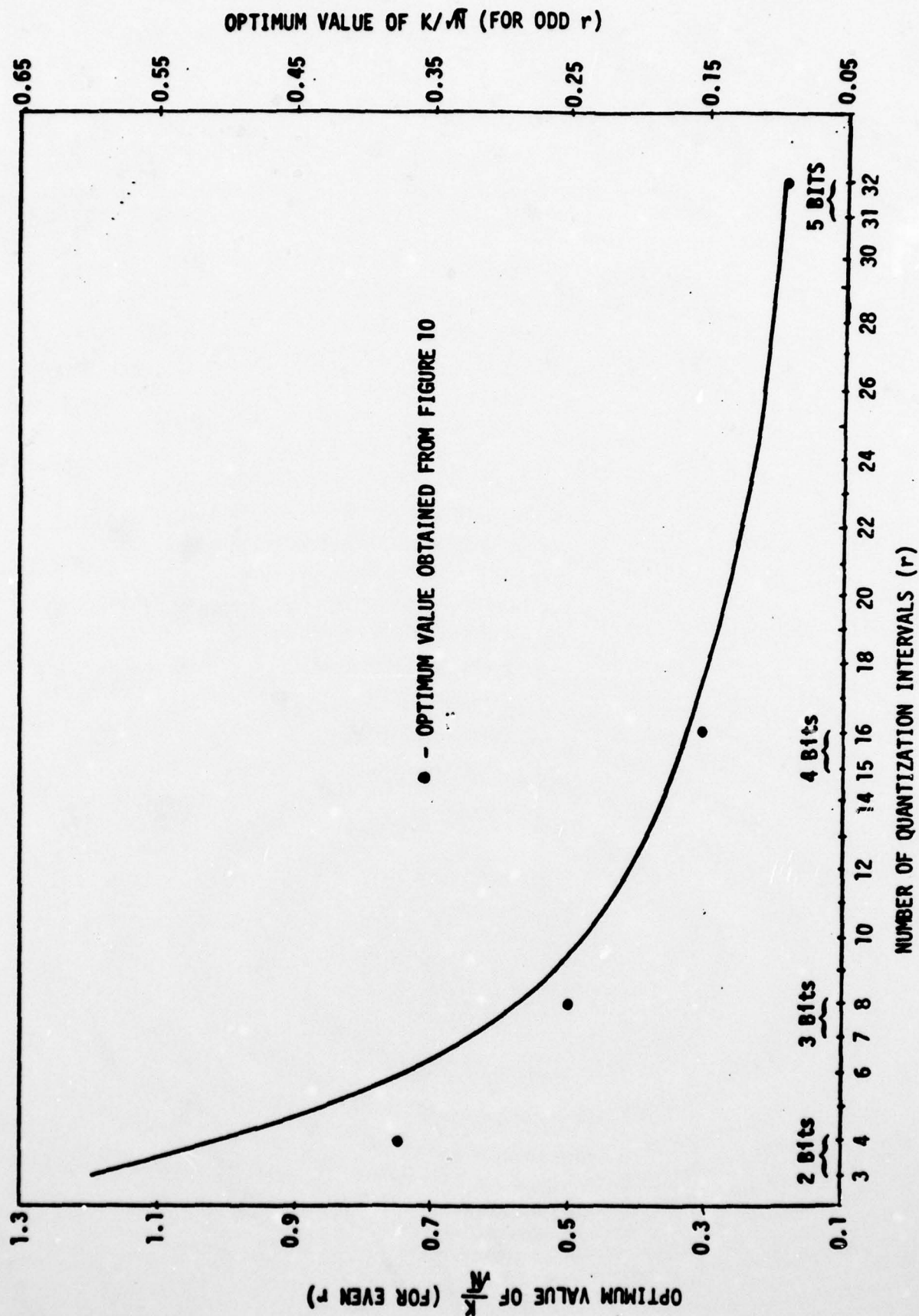


Figure C-6. Optimum Normalized Threshold vs Number of Quantization Intervals (in Gaussian Noise)

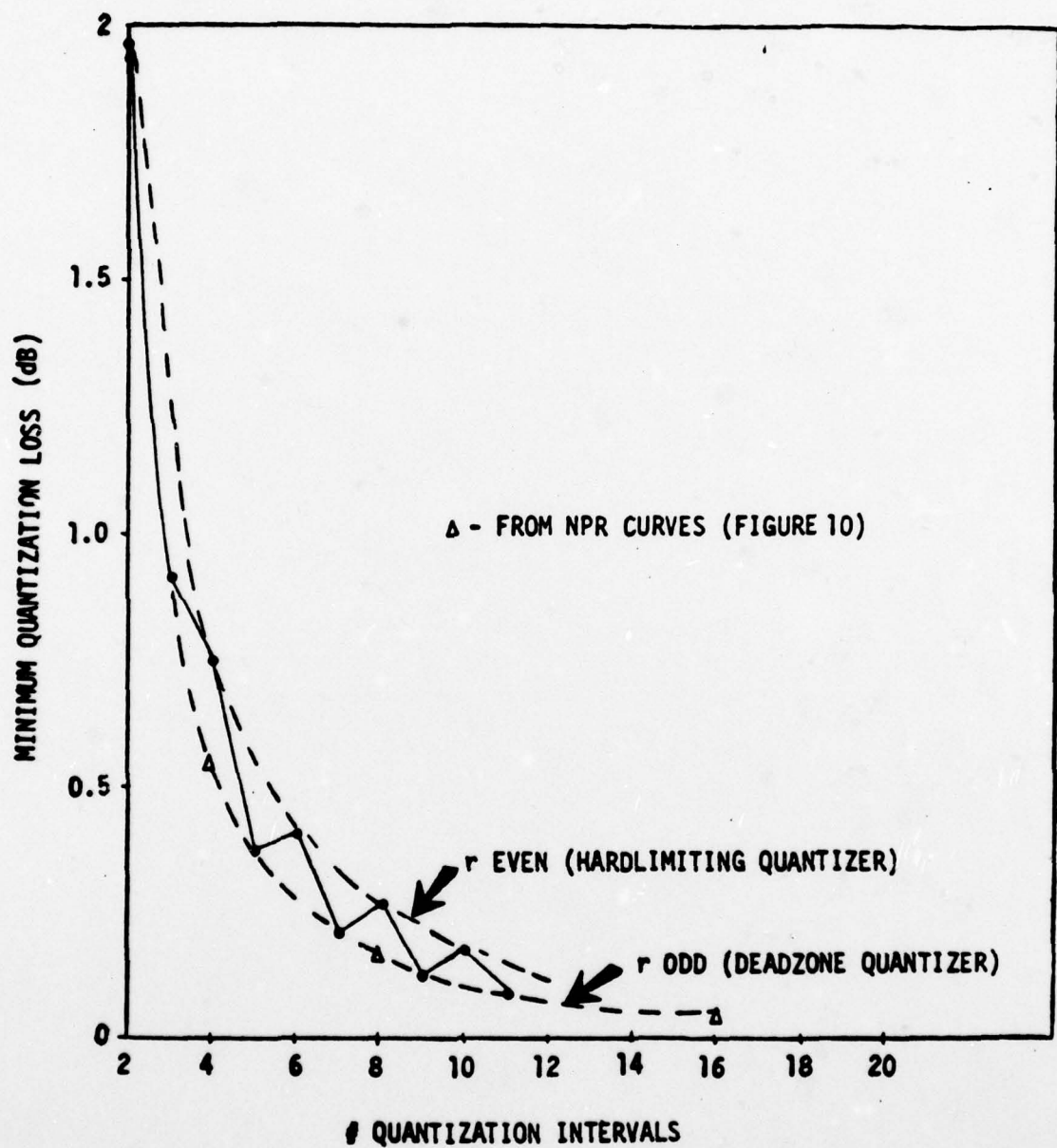


Figure C-7. Minimum Quantization Loss vs Number of Intervals (in Gaussian Noise)

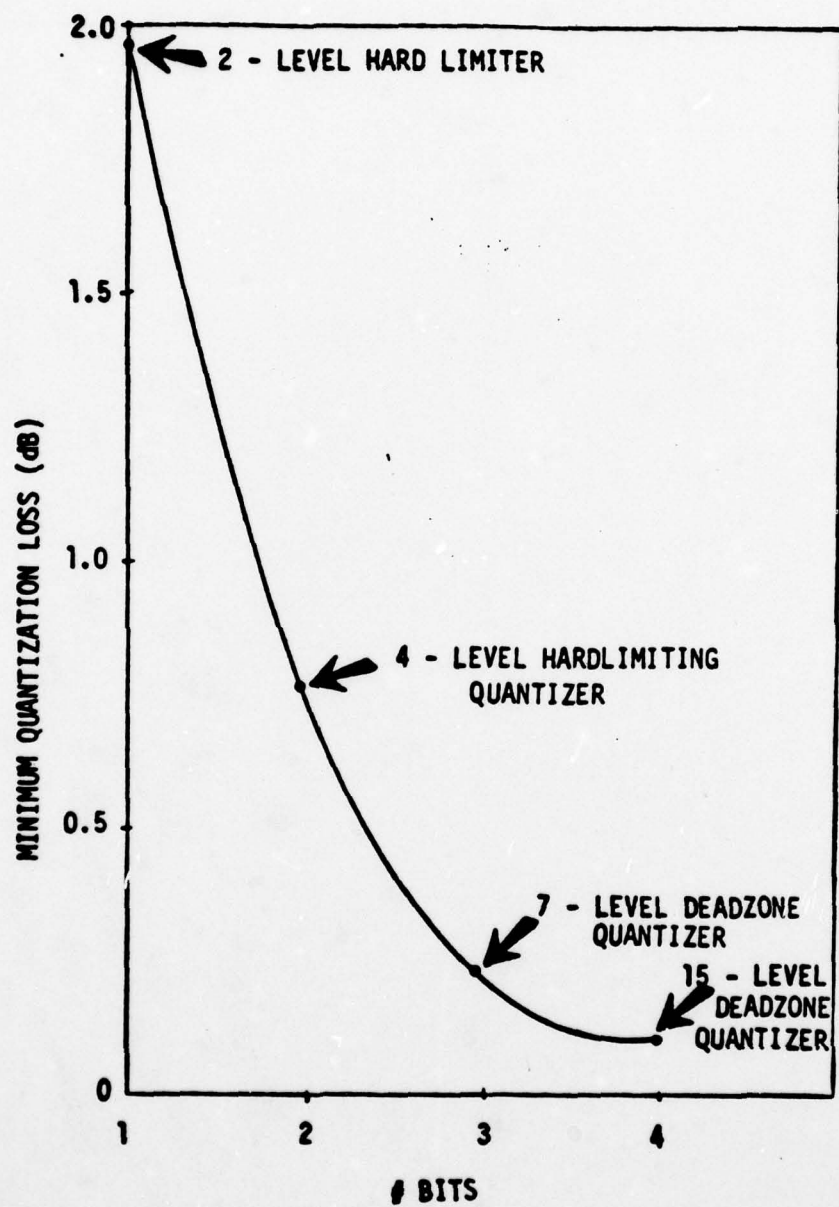


Figure C-8. Minimum Quantization Loss vs Number of Bits (in Gaussian Noise)

It can be shown that the quantization loss can be reduced by using a nonuniform quantizer. For the 4 level quantizer shown in Figure C-4, the output SNR is derived in Reference 2. It is given as

$$\text{SNR}_Q = \frac{2}{\pi} M \frac{S}{N} \left[\frac{k + (1-k) e^{-q^2/2N}}{1 - (1-k^2) \text{erf}(q/\sqrt{2N})} \right] \quad (\text{C-5})$$

The A/D input was taken as a general four-phase signal plus Gaussian noise. The derivation assumes small SNR. This result is then used in Eq. (C-2) with $\text{SNR}_0 = M \frac{S}{N}$ to give the quantization loss. The loss for five values of K is shown in Figure C-9. The $k = 0, 1$ and $1/2$ cases correspond to $r = 3, 2$, and 4 , respectively, in Figure C-5 and the results are the same. It is seen that $k = 1/3$ gives the minimum loss.

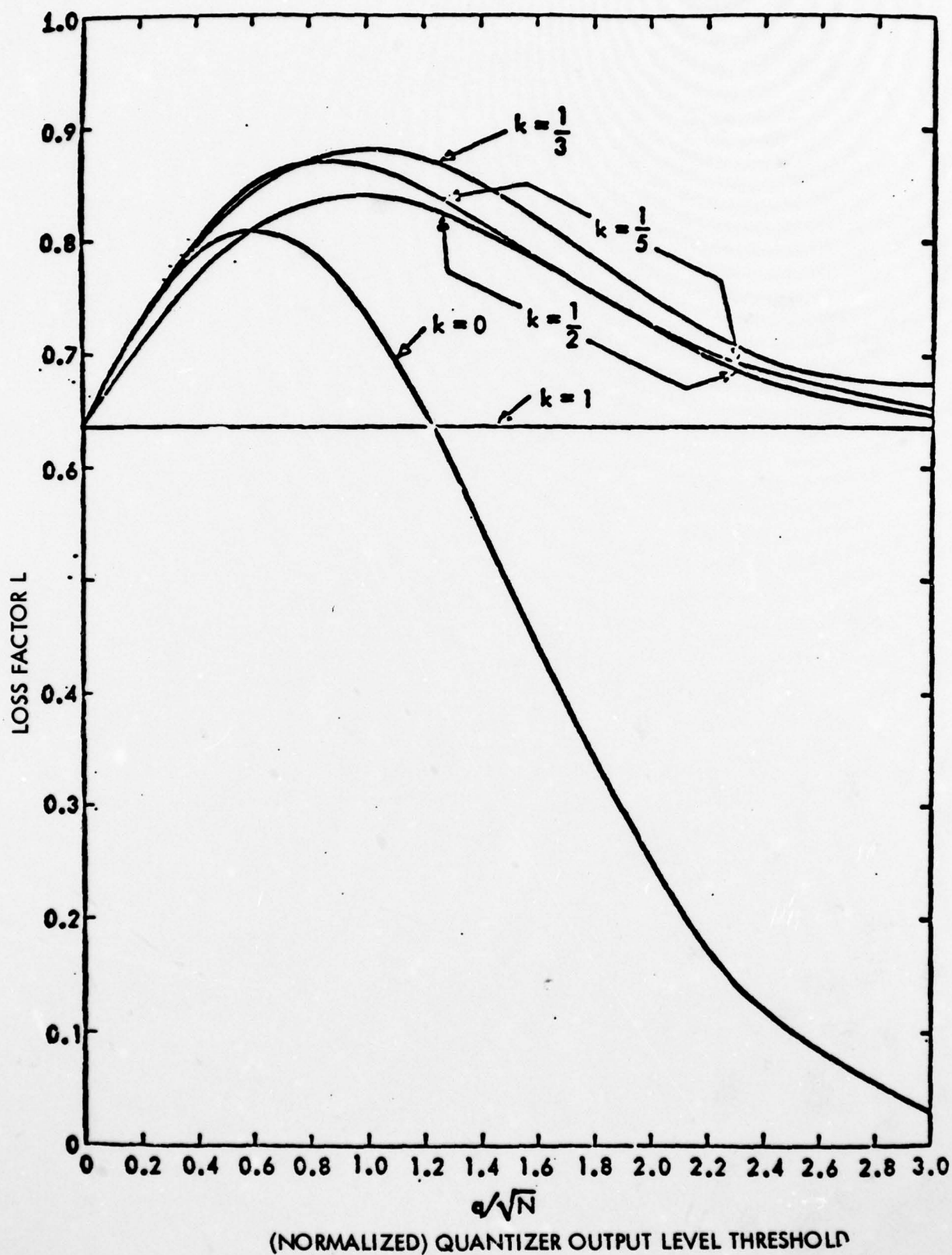


Figure C-9. Loss (L) in Output SNR for Four-Level Quantized DMF in (Strong) Additive Gaussian Noise as a Function of Upper-Lower Quantizer Output Level Breakpoint for Various Values of the Lower Quantizer Level k

III. QUANTIZATION NOISE AND THE NPR

The SNR loss due to quantization in a digital receiver may also be determined by assuming that the loss is due to an additional noise term, N_Q , which increases the level of the output noise. This quantization noise term is assumed to be white, therefore,

$$L = \frac{SNR_Q}{SNR_0} = \frac{\frac{S}{N+N_Q}}{\frac{S}{N}} = \frac{N}{N+N_Q} = \frac{N/N_Q}{N/N_Q+1} \quad (C-6)$$

The ratio N/N_Q is called the noise-power-ratio due to quantization, NPR_Q . Assuming the input is uniform across any quantization interval

$$N_Q = \sigma_Q^2 = \frac{K^2}{12} \quad (C-7)$$

where K is the quantizer step size. This is a good approximation for a large number of intervals. Therefore,

$$NPR_Q = \frac{(\text{RMS INPUT})^2}{K^2/12} = \frac{12\sigma_n^2}{K^2} \quad (C-8)$$

The load factor of an A/D converter is often defined as

$$LF = \frac{\text{RMS INPUT}}{\text{QUANTIZER PEAK}} = \frac{\sigma_n}{1/2 N_L K} \quad (C-9)$$

where N_L is an even number of levels. Using Equation (C-9) in (C-8) gives

$$NPR_Q = 3N_L^2(LF)^2 \quad (C-10)$$

and since $N_L = 2^{N_b}$ where N_b = number of bits, Equation (C-9) may be written in dB as

$$NPR_Q \text{ (dB)} = 4.8 + 6 \cdot N_b + 20 \log LF \quad (C-11)$$

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This equation is shown in Figure C-10 as the linear portion of the curves.* The decrease in NPR for large load factors is due to clipping. The derivation for this portion of the curves is rather lengthy and is given in Reference 3. Figure C-20 is often used in determining A/D distortion. An additional term of $10 \log (f_s/2B)$ may be added to Equation (C-10) to account for aliasing noise. The curves shown are for $f_s = 2 \cdot B$.

It is interesting to compare these results with those given in the last section. Using the optimum LF to get an NPR for each N_b and using Equation (C-6), the quantization loss is plotted on Figure C-7. The greatest deviation is at 2 bits where the difference is 0.2 dB. For a comparison, the optimum value of normalized threshold obtained from the NPR curves is shown on Figure C-6.

*Since Equation (C-10) is only valid at relatively large number of bits, the curves in Figure C-20 are adjusted for $N_b < 4$ by considering the Gaussian nature of the noise in determining the variance of the quantization noise.

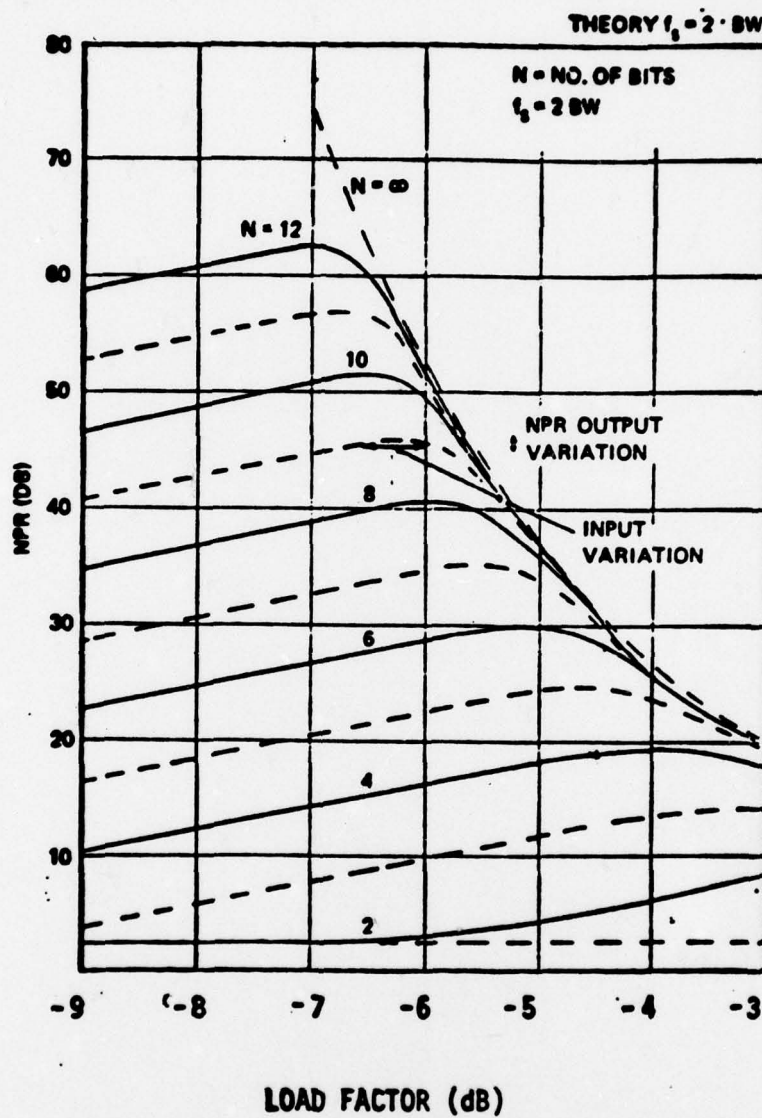


Figure C-10. NPR Variation Versus Loading and Bits/Sample (N)

IV. QUANTIZATION AND NON-GAUSSIAN INTERFERENCE

This case assumes narrow band interference; for example, an unmodulated carrier or an angle modulated signal with bandwidth narrow compared to that of the receiver's bandpass filter. This interference may have a small peak-to-rms ratio (≈ 1), i.e. it is a constant envelope type signal. If the amplitude of the interference is larger than that of the desired signal, then the interfering signal may partially or completely capture the quantizer. That is, the output of the quantizer will not change in response to the modulation of the desired signal. The amount of capture will depend on the relative phase between the interfering and desired signals. In addition, if the interference is at a different frequency than that of the carrier reference, then the relative phase will rotate and, therefore, cause a fluctuating signal suppression. The relative phase variation is assumed to be uniform across the M chips and the results will be averaged over all interfering phases from 0 to 2π .

The results to be presented are taken from Reference 2. The quantization loss is as defined in Eq. (C-2), where now the noise power N is defined as the power, J , in the narrowband interference. The four-level quantizer shown in Figure C-4 is used. Figs. (C-11) - (C-14) show the results for four signal power-to-jammer power ratio (S/J). Two signal phases were chosen as being representative. Signal phases of 0° , 90° , 180° , and 270° give identical performance as do phases of 45° , 135° , 225° , and 315° . If $k = 1$ and $S/J \ll 1$, the expression for the loss gives $2/\pi^2$, the degradation of a two-level quantizer in constant amplitude interference. Also for $q > \sqrt{2J} + \sqrt{2S}$, the loss reduces to $2/\pi^2$ since two level quantization is taking place.

For small S/J , the typical case, it can be seen that the range over which an SNR improvement (over a linear receiver) can be made is small. That is, the improvement depends on how accurately the AGC can measure the received signal

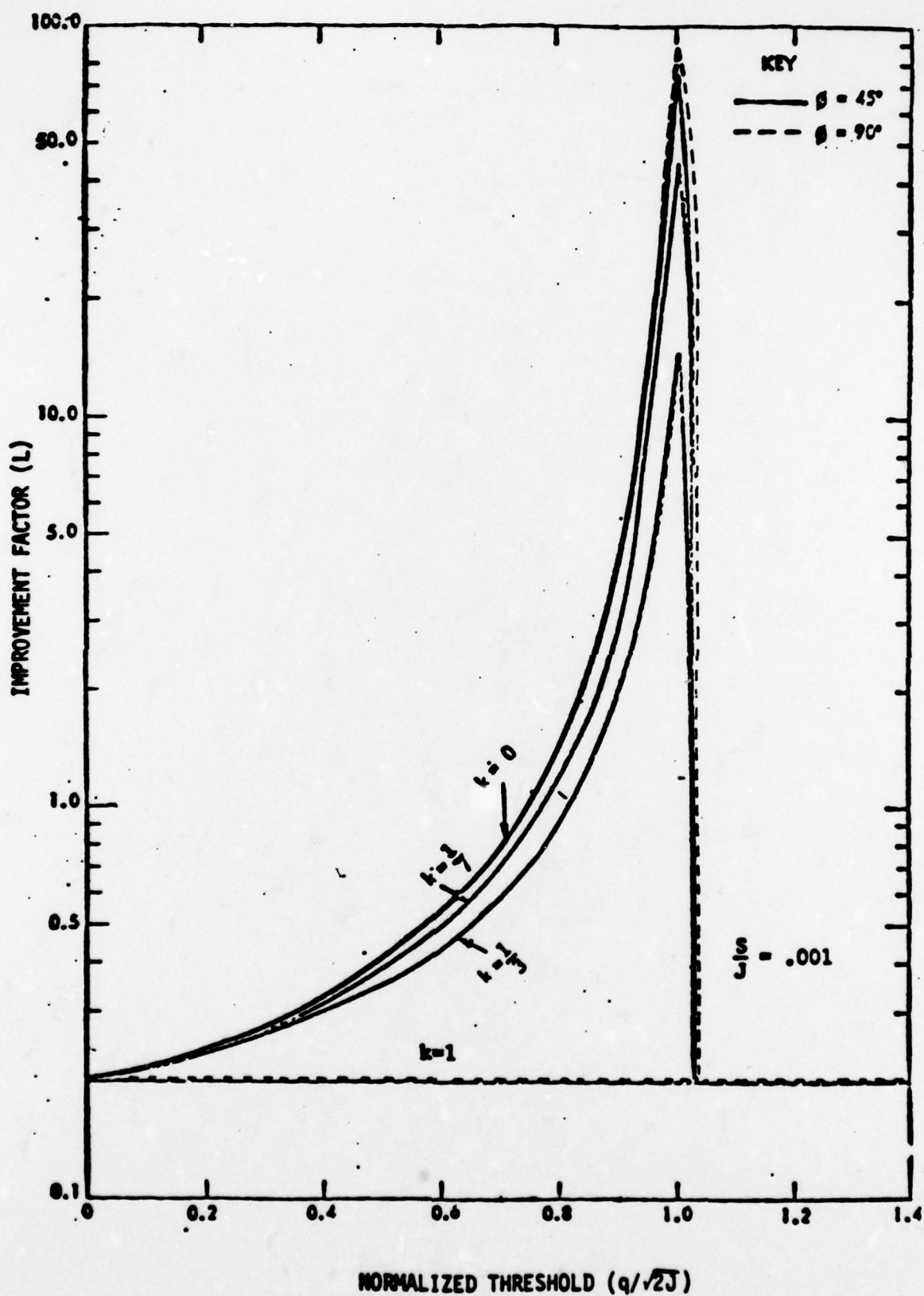


Figure C-11. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 0.001$)

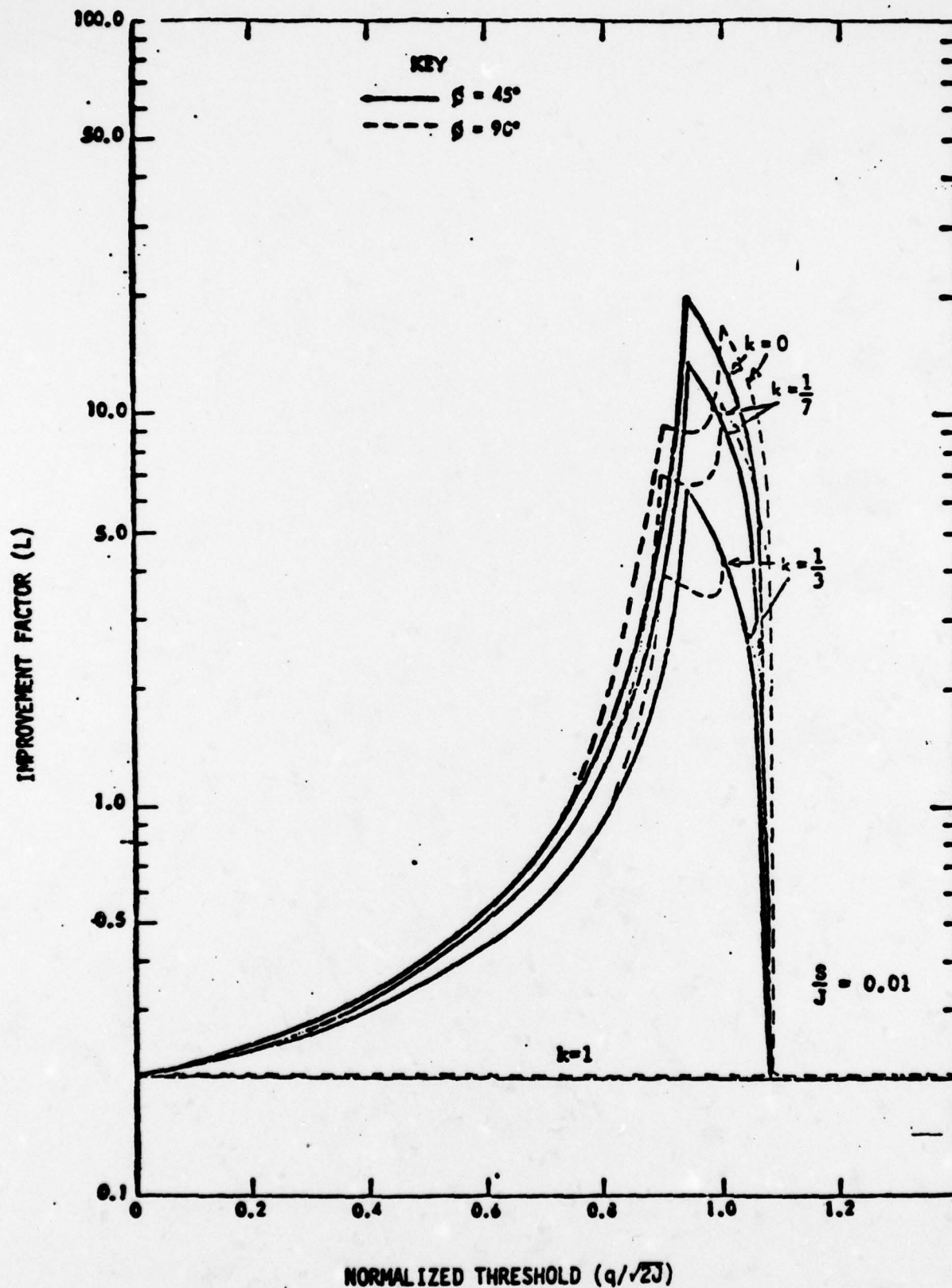


Figure C-12. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 0.01$)

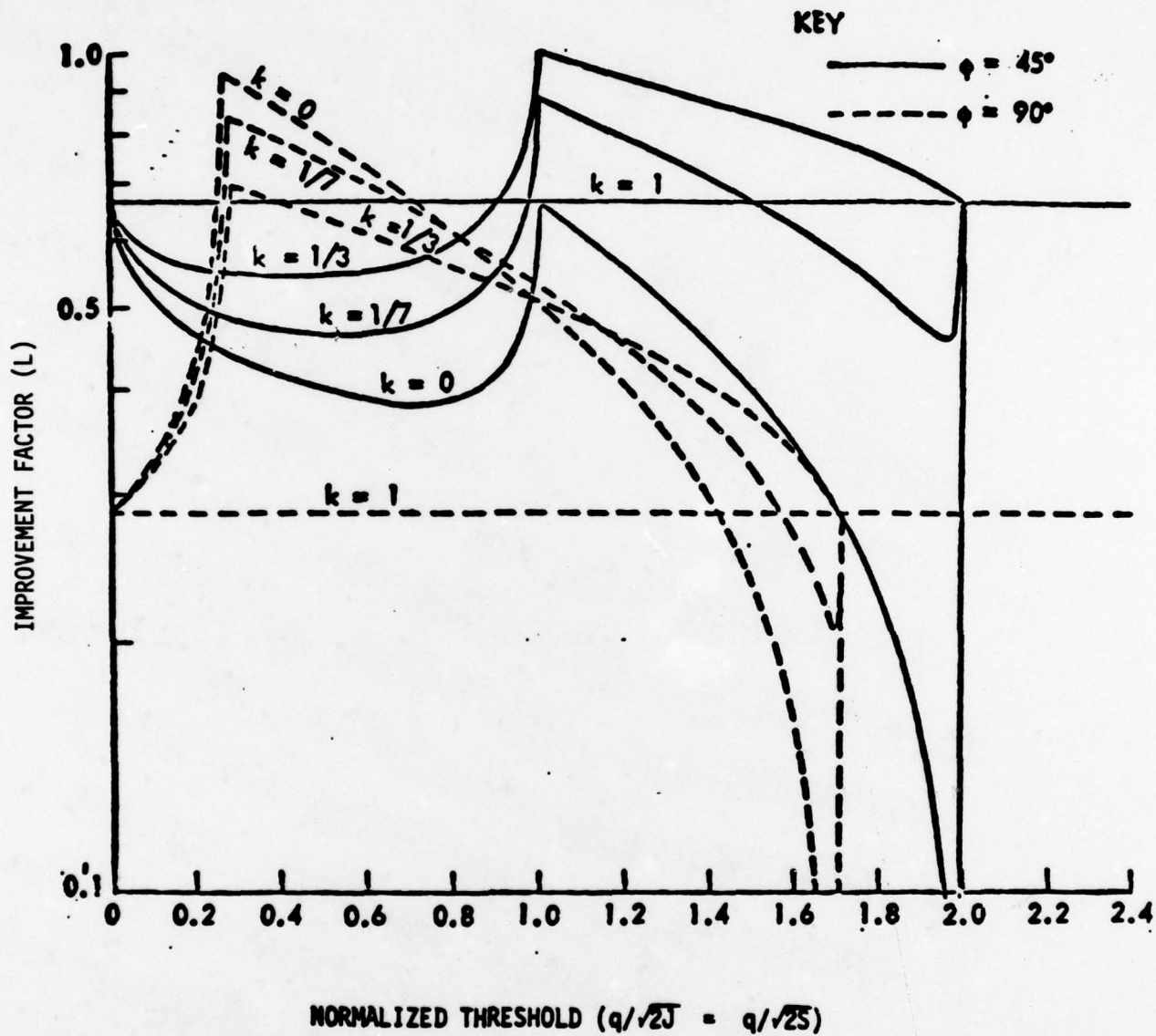


Figure C-13. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 1$)

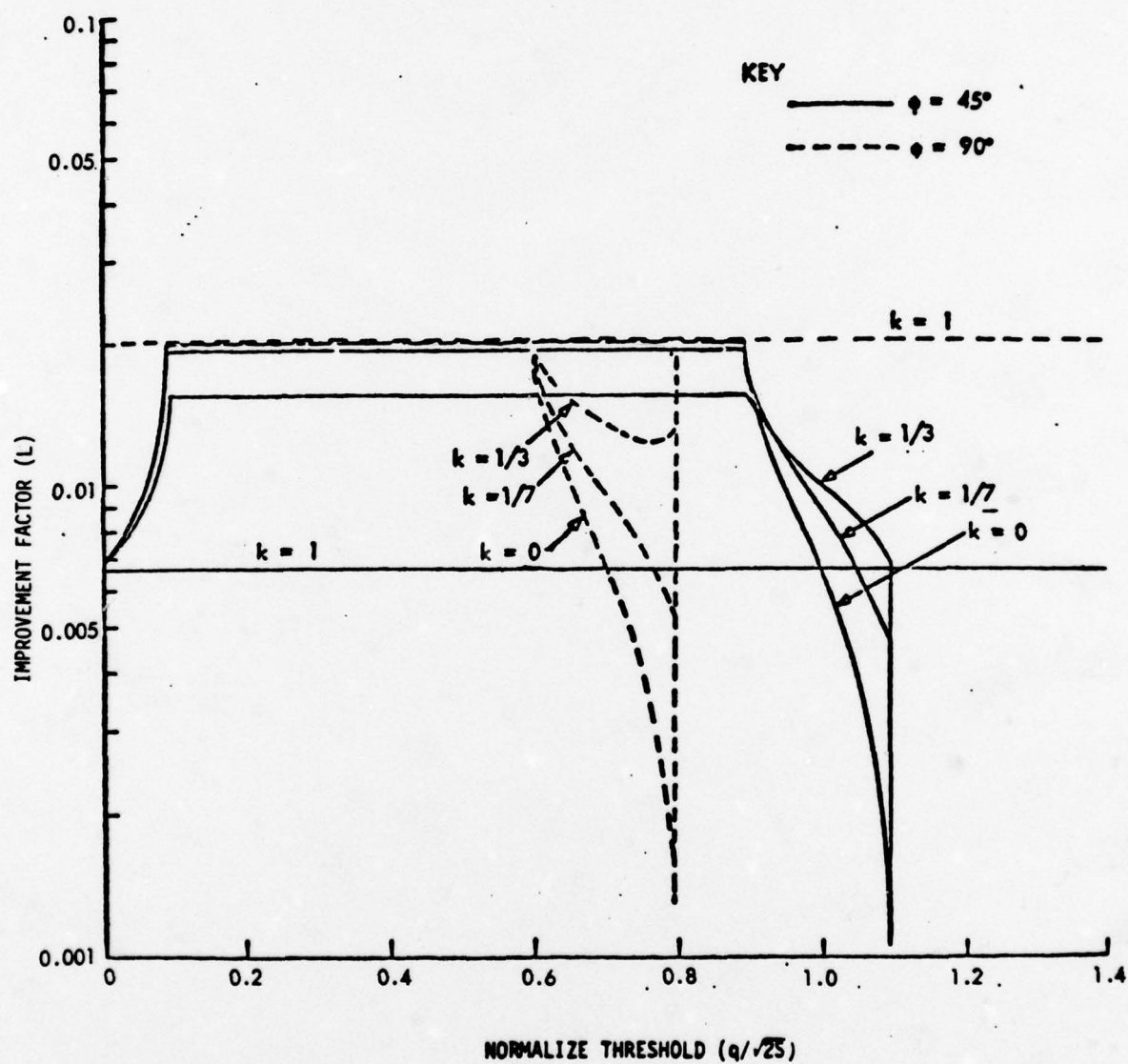


Figure C-14. Improvement Factor as a Function of Quantizer Parameters for 4-Phase Digital Matched Filter ($S/J = 100$)

plus interference envelope.* From Figure C-11, it is seen that at $q/\sqrt{2J} \approx 1.0$ the output SNR is almost 20 dB greater than that of a linear matched filtering receiver, however, a small error in measuring $\sqrt{2J}$ could cause the output SNR to drop by 27 dB. To prevent this, the system would need to operate at a loss factor of about one (0 dB). For small S/J, the optimum value of the lower quantization level is $k = 0$, i.e. a three-level quantizer. However, $k = 0$ gives rather poor performance in Gaussian noise, see Figure C-9, therefore, a compromise in the choice of k and q may be necessary in order to insure satisfactory performance in both Gaussian noise and constant amplitude interference. At high S/J, the improvement is less, however, the output SNR is higher due to the smaller jammer power.

These results are not surprising. It is obvious that at small S/J if the receiver quantizer threshold is adjusted to be approximately equal to the received signal envelope then the effect of the interfering signal will be reduced, whereas at large S/J, the quantizer threshold is following the desired signal envelope and thus reducing the receiver's performance with respect to a linear receiver. This same effect can be obtained by using a biased two-level quantizer (Reference 4), giving the same $k = 0$ curves with a 3 dB loss in improvement factor. However, these results assumed a uniform jammer signal phase across the M chips of the waveform. This is, in effect, averaging the capture effect of the jammer. An "intelligent" jammer may very likely be able to do better than uniform phase. In order to reduce the susceptibility to this type of interference a dither signal may be used.

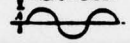


*In Figures C-11 - C-14, the quantizer threshold is normalized by dividing by the larger of the signal or jammer envelopes, $\sqrt{2S}$ or $\sqrt{2J}$

V. EFFECTS OF DITHER

Dithering is here defined as the addition of a fluctuating waveform to the quantizer signal input. Dithering can improve performance of both the four-level adaptive threshold quantizer discussed in the last section and the uniform level quantizers shown in Figures C-2 and C-3. Not unexpectedly, the analysis of the case of a non-coherent M-ary quadrature digital correlating (N-level quantizers) receiver using dither is very complex and the results don't seem to be available. However, conclusions can be drawn from the results of less complex systems. Obviously, if the jammer has the correct phase and a large amplitude it can completely capture a quantizer. The addition of a fluctuating waveform "averages out" the large jamming signal. The amount of improvement is a function of the jammer-to-dither power ratio.

Freeman, [5], considers the case of a coherent digital correlating receiver with hardlimiting. He calls this a Polarity Coincidence Correlator. The output of the device is proportional to the number of chip agreements of sign of the hardlimited received signal and the reference signal. He considers three types of interference: Gaussian noise, rectangular wave, and CW ; and three dither signals: uniform, CW, and Gaussian waveforms. Table C-1 is taken from Freeman's work and it summarizes his SNR results. He makes the usual small input SNR assumption. The output SNR's without dithering for Gaussian and CW interference agree with the results given in this memo for the two-level hardlimiter. The improvement in output SNR with dithering depends on the ratio of dither amplitude to interference power. The receiver must continuously monitor the interference power and adjust the dither amplitude so as to eliminate capture but not so large as to degrade the output SNR. It is found that uniform dither is slightly better than sinusoidal dither and both are superior to Gaussian noise dither. Freeman's results for uniform dither are shown in Figure C-15. Although not shown on the figure, from Table C-1 it can be seen that the rectangular

Table C-1. Effects of Dither on Hardlimiting Correlator

Interference Type	$(S/N)_0$ for a Signal Having N Pulses With Amplitude $\pm a$				
	Classical Correlation Detector	Polarity Coherent Detector			
		Without Dither	With Uniform Dither $-d_0 \leq d(t) \leq d_0$	With CW Dither 	With Gaussian Dither
Gaussian Noise	$\sqrt{S^2/a^2}$	$\frac{2}{\pi} N S^2/a^2$	$N \left[\frac{S}{d_0} \operatorname{erf} \left(\frac{d_0}{\sqrt{2} a} \right) \right]^2$	$\frac{2 N S^2}{\pi a^2} e^{-1/2} I_0 \left(\frac{A^2}{2 d_0^2} \right)$	$\frac{2 N S^2}{\pi a^2 (1 + d_0^2/a^2)}$
Rectangular Wave 	$\sqrt{S^2/a^2}$	$0, C > S$ $\infty, C < S$	$N S^2/d_0^2, C < d_0$ $0, C > d_0$	$\frac{4}{\pi^2} N S^2 (A^2 - C^2), C < A - S$ $0, C > A + S$	$\frac{2 N S^2}{\pi a^2} e^{-C^2/a^2}$
CW  J am	$\sqrt{S^2/a^2}$	$4 N S^2/a^2$	$N S^2/d_0^2, J < d_0$ $N \left[\frac{J}{d_0} \operatorname{erf} \left(\frac{d_0}{\sqrt{2} J} \right) \right]^2, J > d_0$	$\frac{16 N S^2}{\pi^2 A^2} K^2 \left(\frac{J}{A} \right), J - S < A$ $\frac{16 N S^2}{\pi^2 J^2} K^2 \left(\frac{A}{J} \right), A - S < J$	$\frac{2 N S^2}{\pi a^2} e^{-J^2/a^2} I_0 \left(\frac{A^2 - S^2}{a^2} \right)$

$(S/N)_0 = S^2/a^2$ for different detectors under different interference conditions, for signal power negligible compared to interference power.

1. $K(x)$ is the complete elliptic integral of the first kind
2. $I_0(x)$ is the modified Bessel function

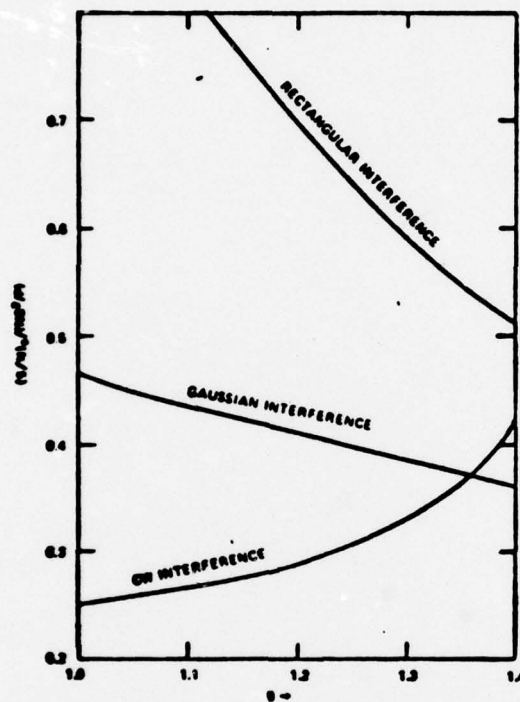


Figure C-15. $(S/N)_0$ of a Polarity Coincidence Detector with Uniformly Distributed Dither Divided by $(S/N)_0$ of a Classical Correlator as a Function of g , for Small Signal Power

* g is the dither to interference amplitude ratio
 i.e. $d_0 = \sigma_d = 2\sqrt{P}$ and $P = \sigma_n^2 = c^2 = J^2/2$

and CW interference give the same $(\text{SNR})_0$ for $d_0 > c$ and $d_0 > J$, i.e. $g > \sqrt{2}$. The worst case is maximized by letting $g = 1.36$ giving $(\text{SNR})_0 = 0.37 NS^2/P$, 4.3 dB below theoretical. He shows that for sinusoidal dither, the worst case is maximized at $g = 1.16$ giving performance 4.7 dB below optimum and for Gaussian dither, it is $g = 1$ giving performance 6.4 dB below optimum.

Lewis, [6], considers coherent PSK digital demodulation of N symbol binary sequences with tone interference at the carrier frequency. Infinite level quantization is assumed. A triangular or sinusoidal dither is added to the correlator input. The dither peak-to-peak is made equal to the quantizer interval size. Lewis calculates the quantization loss as previously defined. He shows that the uniform (triangle) dither gives better overall performance. His curves are shown in Figure C-16 for typical J/S ratios. The dither waveform should be essentially constant over a chip time, i.e. a dither frequency much less than the PN code rate. For uniform dither, the maximum quantization loss is 0.46 dB where the usable range of the A-D extends from $A_J/\Delta = 1/2$ (Δ is the interval size) to the clipping threshold of the quantizer. For small S/J , the clipping level of the hardlimiting quantizer is at

$$A_J = (2^{N_b-1} - 1/2)\Delta$$

and for the deadzone quantizer is at

$$A_J = (2^{N_b} - 1)\Delta$$

The clipping level for the hardlimiting quantizer is shown on Figure C-16.

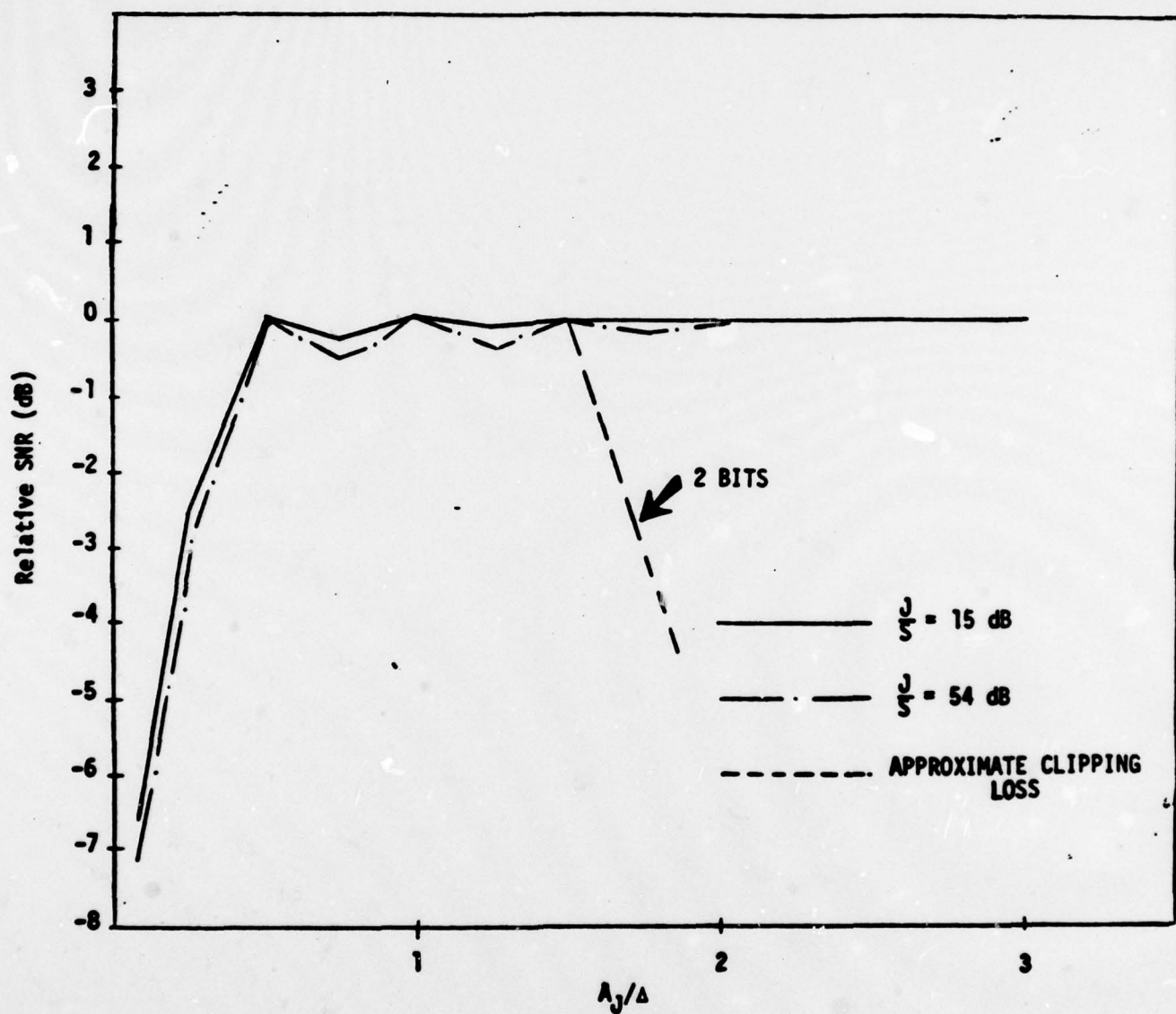


Figure C-16. SNR Loss for Triangle Dither with Hardlimiting A-D

VI. CONCLUSIONS

In this section, the results will be summarized. In Gaussian noise, the 1-bit quantizer, 2-level hardlimiter, gives 1.96 dB quantization loss and the 2-bit quantizer gives 0.74 dB loss an improvement of 1.22 dB. Going to a 3 bit quantizer only gains about 0.5 dB. Since the processing complexity in terms of increased hardware increases with the number of bits per sample, the 2-bit quantizer is the desirable choice. Considering non-Gaussian interference, although it was not verified analytically, the results indicate that the same conclusions can be made. For small S/J , the uniform level 1-bit quantizer gives a loss of $2/\pi^2 = -7.0$ dB and with an adaptive threshold, the 2-bit quantizer can give an improvement (over the linear receiver) of 20 dB or more (depending on S/J). However, a biased 2-level quantizer is only 3 dB poorer than a three-level (2-bit) quantizer [4]. The three level quantizer (deadzone with $N_b = 2$) gives the best performance in narrowband interference at small S/J as much as 8 dB over the 4-level at $S/J = 0.001$ ($k=1/3$, Figure C-11) and in Gaussian noise is only 0.4 dB poorer than the 4-level quantizer (Figure C-9). This implies that the best overall performance can be obtained with a 2-bit deadzone quantizer.

However, these results assume that the optimum normalized quantizer threshold is used, i.e. accurate measurement of the received signal envelope is required. Limitations on the associated hardware would necessitate the output SNR being backed off from the maximum gain. Table C-2 lists the improvement in SNR_Q by using a 3-level versus a 4-level quantizer in narrowband interference when the threshold is backed off from optimum enough to account for the percent error in measuring $q/\sqrt{2J}$ (This is for small S/J , Figure C-11). It also shows the L factor for the backed off condition with no actual error in measuring $q/\sqrt{2J}$. Above 30% backoff the advantage of the 3-level quantizer in narrowband interference is outweighed by the advantage of the 4-level ($k = \frac{1}{3}$) quantizer in Gaussian noise (where no backoff is required). Also, if the receiver cannot determine what type of interference is predominate, in order to set the optimum threshold, then a compromise

Table C-2. Effects of Envelope Measurement Error in Narrowband Interference

<u>Max Error in $q/\sqrt{2J}$</u>	<u>$L(k=0)/L(k=1/3)$ dB</u>	<u>$L(k=0)$ dB</u>
0%	7.6	19
10%	3.3	6.4
20%	2.2	3.1
30%	1.7	0.4
40%	1.3	-0.7
50%	1.1	-1.6

in threshold setting must be made and the 4 level quantizer will then give better overall performance.*

The addition of a uniform dither signal almost linearizes the quantizer characteristics (this result assumes tone interference at the carrier frequency [6]). At first glance, this may seem bad since at small S/J the 4-level quantizer gives large SNR gains over the linear matched filter receiver. However, as noted above, the gains are reduced when a practical signal envelope measurement error is considered. In addition, dithering reduces the probability that the quantizer will be captured by a large jammer waveform with a peak/rms ≈ 1.0 . If captured, the output SNR drops to 0 ($-\infty$ dB), i.e. no desired signal output. Cahn [7] determines upper bounds on the quantized SNR degradation using a minimax design philosophy. He determines the dither waveform probability density that minimizes a quantizer error for the worst case (unknown) interference. For a two level quantizer with dithering the worst performance degradation is 4.8 dB and for four level it is 2.3 dB. The dither amplitude should be greater than the interference amplitude. For small S/J, the dither-to-jammer amplitude ratio should be about 1.36 for both the 2- and 4-level quantizers.

*This conclusion is also supported if the realistic assumption is made that the receiver is continuously operating in a Gaussian noise environment and only needs to combat large narrowband interference a fraction of the operating time.

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APPENDIX D

FREQUENCY DISCRIMINATORS

In many signal processing systems, it is necessary to track the frequency of the signal in order to demodulate the signal efficiently. In these situations, a frequency-locked loop (FLL) or phase-locked loop (PLL) can be used to perform this function. The FLL is addressed in this memo. In particular, two types of frequency discriminators are described and compared. One is based on computing a discrete time approximation of the derivative of the phase of the received signal. The second type is based on computing the Fourier transform of the received signal. The two discriminators are shown to be equivalent for a certain choice of parameters.

Frequency Locked Loop Configuration

The system configuration of interest is shown in Figure D-1. The received signal $S(t)$ is mixed down to baseband quadrature components $i(t)$ and $q(t)$ using the VCO estimate of the center frequency of the received signal. The baseband components are integrated and the results, $I(t)$ and $Q(t)$, are input to the frequency discriminator. The discriminator output Z is filtered in the loop filter and is used to control the frequency of the VCO.

The input signal is given by

$$s(t) = A \cos[(\omega_c + \omega_d)t + \theta_0] + n(t)$$

where

ω_c = carrier frequency

ω_d = doppler offset

θ_0 = phase offset

$n(t)$ = white Gaussian noise of two-sided spectral density $N_0/2$

Then, the mixer outputs are given by

$$i(t) = s(t) \cos(\omega_c + \hat{\omega}_d)t = \frac{A}{2} \cos[(\omega_d - \hat{\omega}_d)t + \theta_0] + n(t) \cos(\omega_c + \hat{\omega}_d)t$$

$$q(t) = -s(t) \sin(\omega_c + \hat{\omega}_d)t = \frac{A}{2} \sin[(\omega_d - \hat{\omega}_d)t + \theta_0] + n(t) \sin(\omega_c + \hat{\omega}_d)t$$

where $\hat{\omega}_d$ = doppler frequency estimate.

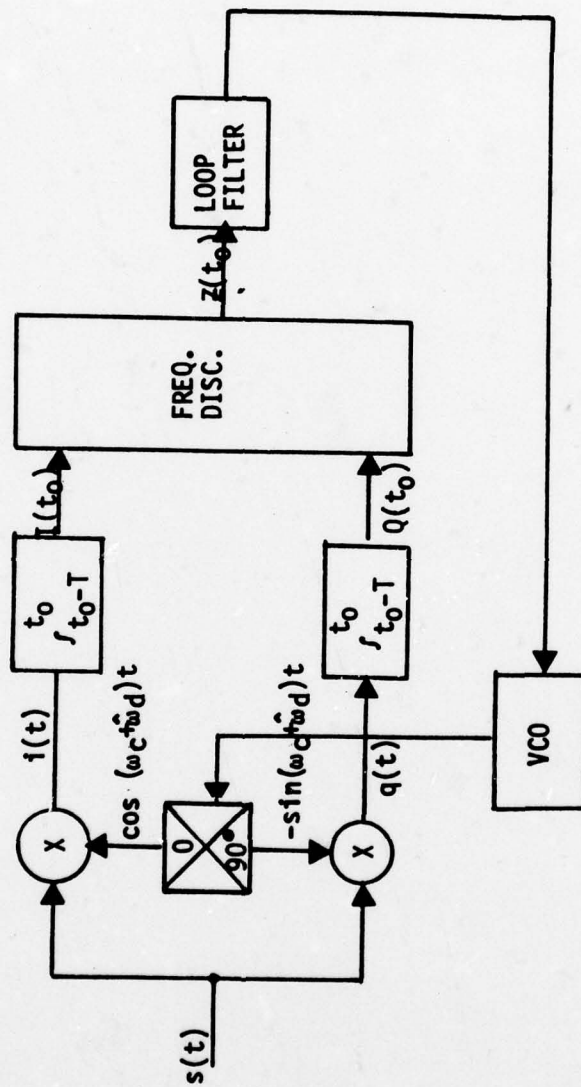


Figure D-1. Frequency Locked Loop Configuration

The double frequency terms have been neglected since they will be filtered out in the integrator. The integrator outputs are given by

$$I(t_0) = \int_{t_0-T}^{t_0} i(t) dt = \frac{AT}{2} \left(\frac{\sin(\omega_d - \hat{\omega}_d)T/2}{(\omega_d - \hat{\omega}_d)T/2} \right) \cos((\omega_d - \hat{\omega}_d)(t_0 - T/2) + \theta_0) + \int_{t_0-T}^{t_0} n(t) \cos(\omega_c + \hat{\omega}_d) t dt$$

$$Q(t_0) = \int_{t_0-T}^{t_0} q(t) dt = \frac{AT}{2} \left(\frac{\sin(\omega_d - \hat{\omega}_d)T/2}{(\omega_d - \hat{\omega}_d)T/2} \right) \sin((\omega_d - \hat{\omega}_d)(t_0 - T/2) + \theta_0) + \int_{t_0-T}^{t_0} n(t) \sin(\omega_c + \hat{\omega}_d) t dt$$

$$\text{Let } n_c(t_0) = \int_{t_0-T}^{t_0} n(t) \cos(\omega_c + \hat{\omega}_d) t dt$$

Then,

$$R_{n_c}(\tau) = E[n_c(t_0)n_c(t_0+\tau)] = E \left[\int_{t_0-T}^{t_0} \int_{t_0-T+\tau}^{t_0+\tau} n(\rho)n(\sigma) \cos(\omega_c + \hat{\omega}_d)\rho \cos(\omega_c + \hat{\omega}_d)\sigma d\rho d\sigma \right]$$

$$= \int_{t_0-T}^{t_0} \int_{t_0-T+\tau}^{t_0+\tau} N_0/2 \delta(\rho - \sigma) \cos(\omega_c + \hat{\omega}_d)\rho \cos(\omega_c + \hat{\omega}_d)\sigma d\rho d\sigma$$

$$= \frac{N_0}{4} (T - |\tau|) \quad \text{for } |\tau| \leq T$$

Similarly,

$$n_s(t_0) = \int_{t_0-T}^{t_0} n(t) \sin(\omega_c + \hat{\omega}_d) t dt$$

$$R_{n_s}(\tau) = E[n_s(t_0)n_s(t_0+\tau)] = R_{n_c}(\tau) \triangleq R_n(\tau)$$

Phase Differential Frequency Discriminator

The first discriminator is based on an approximation to the time derivative of the input phase. The signal phase, $\theta(t)$, is given by

$$\theta(t) = \tan^{-1} \frac{Q(t)}{I(t)}$$

The frequency is given by

$$\begin{aligned}\omega(t) = \dot{\theta}(t) &= \frac{d}{dt} \tan^{-1} \frac{Q(t)}{I(t)} \\ &= \frac{1}{1 + \left(\frac{Q(t)}{I(t)}\right)^2} \cdot \frac{I(t)\dot{Q}(t) - Q(t)\dot{I}(t)}{I^2(t)} \\ &= \frac{I(t)\dot{Q}(t) - Q(t)\dot{I}(t)}{I^2(t) + Q^2(t)}\end{aligned}$$

For a constant envelope signal $I^2(t) + Q^2(t) = \text{constant}$. Therefore,

$$\omega(t) \approx I(t)\dot{Q}(t) - Q(t)\dot{I}(t)$$

We approximate the time derivatives as follows:

$$\dot{Q}(t) \approx Q(t) - Q(t-T)$$

$$\dot{I}(t) \approx I(t) - I(t-T)$$

Therefore,

$$\begin{aligned}\omega(t) &\approx I(t)[Q(t) - Q(t-T)] - Q(t)[I(t) - I(t-T)] \\ &= Q(t)I(t-T) - I(t)Q(t-T)\end{aligned}$$

The term $\omega(t)$ represents the signal frequency after conversion to baseband and therefore is equal to the difference in frequency between the received signal and the local estimate of the received frequency (that is, the frequency error). The FLL is then designed to null out $\omega(t)$. Figure D-2 shows the structure of the frequency discriminator.

DFT Frequency Discriminator

The DFT frequency discriminator is based on the principle of forming two filters, one higher in frequency than the center frequency of the signal and one lower in frequency. The frequency error signal is then obtained by subtracting the magnitudes of the upper and lower filter outputs. For a positive frequency error, the higher frequency filter will have a larger output than the lower frequency filter, resulting in an error signal which is used to correct the

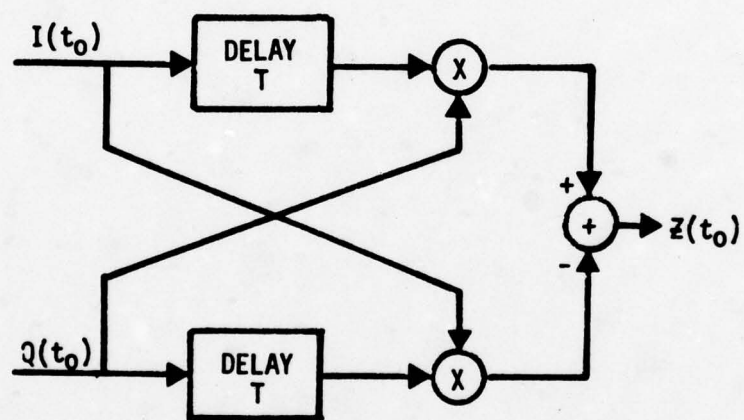


Figure D-2. Phase Differential Frequency Discriminator

local oscillator. A negative frequency error results in an error signal of the opposite polarity. Figure D-3 shows the structure of the DFT discriminator.

Using complex notation, the upper filter output, $X(u,t)$, is given by

$$\begin{aligned} X(u,t) &= I(t-T) + jQ(t-T) + (I(t) + jQ(t))e^{j\pi/2} \\ &= I(t-T) - Q(t) + j(Q(t-T) + I(t)) \end{aligned}$$

$$\begin{aligned} \text{The lower filter output, } X(l,t) &= I(t-T) + jQ(t-T) + (I(t) + jQ(t))e^{-j\pi/2} \\ &= I(t-T) + Q(t) + j(Q(t-T) - I(t)) \end{aligned}$$

Then,

$$\begin{aligned} Z(t) &= |X(u,t)|^2 - |X(l,t)|^2 \\ &= 4[Q(t-T)I(t) - I(t-T)Q(t)] \end{aligned}$$

Therefore we see that for a two-point DFT, this discriminator is equivalent (within a constant factor) to the phase-differential frequency discriminator described earlier.

It is of interest to compute the mean and variance of $Z(t)$ where we take

$$Z(t) = Q(t-T)I(t) - I(t-T)Q(t)$$

From previous expressions, we get

$$I(t) = K \cos \theta(t) + n_c(t)$$

$$Q(t) = K \sin \theta(t) + n_s(t)$$

$$\text{where } K = \frac{AT}{2} \left(\frac{\sin(\omega_d - \hat{\omega}_d)T/2}{(\omega_d - \hat{\omega}_d)T/2} \right)$$

$$\theta(t) = (\omega_d - \hat{\omega}_d)(t - T/2) + \theta_0$$

$$n_c(t) = \int_{t-T}^t n(\rho) \cos(\omega_c + \hat{\omega}_d)\rho d\rho$$

$$n_s(t) = \int_{t-T}^t n(\rho) \sin(\omega_c + \hat{\omega}_d)\rho d\rho$$

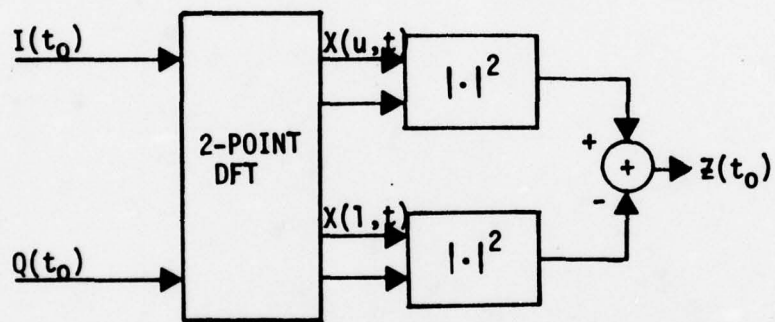


Figure D-3. DFT Frequency Discriminator

Then,

$$\begin{aligned} Z(t) &= K^2 \sin(\theta(t-T) - \theta(t)) + K[n_c(t) \sin \theta(t-T) + n_s(t-T) \cos \theta(t) - n_s(t) \cos \theta(t-T) \\ &\quad - n_c(t-T) \sin \theta(t)] + n_c(t) n_s(t-T) - n_s(t) n_c(t-T) \\ &= K^2 \sin(\hat{\omega}_d - \omega_d)T + N(t) \end{aligned}$$

where $N(t) = K[n_c(t) \sin \theta(t-T) + n_s(t-T) \cos \theta(t) - n_s(t) \cos \theta(t-T) - n_c(t-T) \sin \theta(t)]$
 $+ n_c(t) n_s(t-T) - n_s(t) n_c(t-T)$

Since $n_c(t)$ and $n_s(t)$ are zero mean and uncorrelated,

$$E[N(t)] = 0$$

Also, using the fact that

$$R_n(\tau-T)R_n(\tau+T) = 0$$

where $R_n(\tau) = R_{n_c}(\tau) = R_{n_s}(\tau)$

it can be shown that

$$\begin{aligned} E[N(t)N(t+\tau)] &= R_N(\tau) = 2K^2 R_n(\tau) \cos(\omega_d - \hat{\omega}_d)\tau - K^2 R_n(\tau-T) \cos(\omega_d - \hat{\omega}_d)(\tau+T) \\ &\quad - K^2 R_n(\tau+T) \cos(\omega_d - \hat{\omega}_d)(\tau-T) + 2R_n^2(\tau) \end{aligned}$$

The noise variance is given by,

$$R_N(0) = 2K^2 R_n(0) + 2R_n^2(0)$$

since $R_n(T) = R_n(-T) = 0$

The discriminator output signal to noise ratio can then be written as:

$$\begin{aligned} \text{SNR}_0 &= \frac{E^2[Z(t)]}{R_N(0)} \\ \text{SNR}_0 &= \frac{[K^2 \sin(\omega_d - \hat{\omega}_d)T]^2}{R_N(0)} \end{aligned}$$

When $\omega_d = \hat{\omega}_d$, $\text{SNR}_0 = 0$ since the error signal out of the discriminator is zero.

The function $E[Z(t)] = K^2 \sin(\omega_d - \hat{\omega}_d)T$ is the discriminator error signal. Figure D-4 shows the form of the error signal.

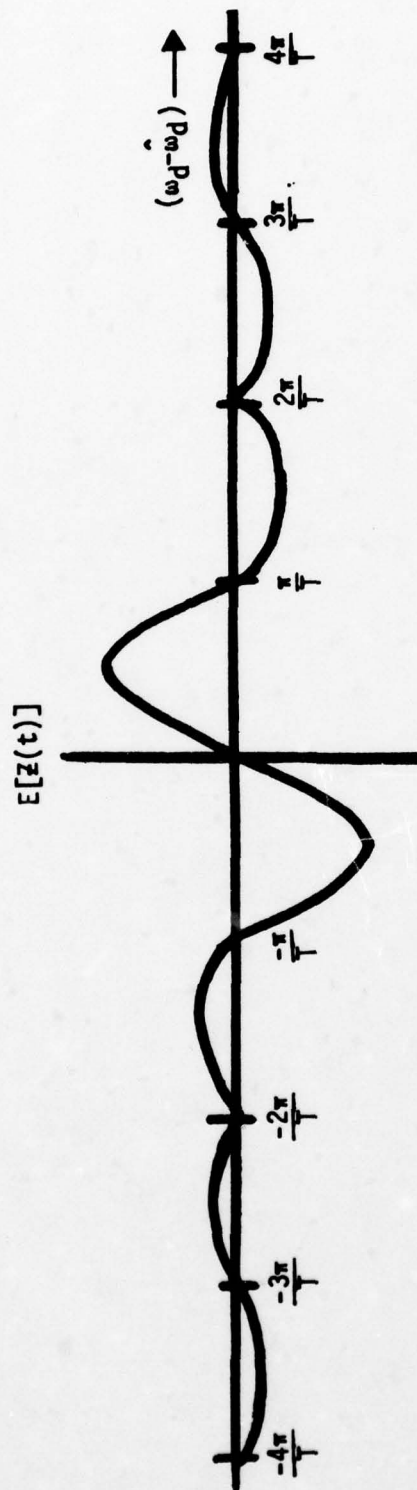


Figure D-4. Frequency Discriminator Error Signal

APPENDIX E
FREQUENCY-LOCKED LOOP AND PHASE-LOCKED
LOOP COMPARISON

The second order phase-locked loop has long been used as the standard carrier acquisition and tracking device. However, in order to maintain satisfactory output phase jitter conditions the acquisition times may be prohibitively large. The following solutions exist:

1. Frequency estimation filtering
2. PLL with dual loop bandwidths
3. PLL with VCO frequency sweeping
4. Frequency - locked-loop acquisition

The first technique involves the use of noncoherent matched filters spaced over the frequency uncertainty band. The largest output is then used to reduce the frequency uncertainty to the bandwidth of the filter. This information may be used to adjust the VCO frequency of a phase-locked loop which then may quickly pull-in and maintain frequency and phase coherence. This procedure is well documented (Viterbi [1]), and will not be pursued in this memo. For large frequency uncertainty the complexity may be excessive and in addition it would be difficult to produce this device as a standard module since a large number of components would have to be switched. The second procedure was a PLL with the capability of switching between two loop bandwidths. A wide bandwidth is used for acquisition and a reduced bandwidth for tracking. A similar technique involves adjusting the loop gain of the PLL. At low SNR these techniques may still not perform satisfactorily in the acquisition mode. The results presented here may be used to examine the practicality of the dual loop bandwidth procedure.

Acquisition techniques three and four will be examined in detail. Frequency acquisition using the PLL with and without VCO frequency sweeping is compared with acquisition performance using the frequency-locked loop (FLL).

[1] Viterbi, A.J., Principle of Coherent Communication, McGraw Hill, 1966.

The two devices are compared by optimizing the loop bandwidths of each device in terms of the tradeoff between dynamic frequency (or phase) error during acquisition and RMS frequency (or phase) error due to input noise during tracking. The RMS frequency error at this loop bandwidth is plotted versus input SNR and acquisition times are plotted versus loop bandwidth. In this way, at any available SNR, the optimum device may be selected and the loop bandwidth determined.

The tracking device selected should be able to track the doppler effects produced by relative motion between the transmitter/receive pair. The range may be expressed, in a Taylor series, as

$$r(t) = r_o + \dot{r}t + \ddot{r} \frac{t^2}{2} + \ddot{\ddot{r}} \frac{t^3}{6} + \text{higher order terms} \quad (\text{E-1})$$

where

- r_o = Initial range, m
- \dot{r} = Range rate, m/s
- \ddot{r} = Range acceleration, m/s²
- $\ddot{\ddot{r}}$ = Range jerk, m/s³

Dividing this by the carrier wavelength, $\lambda = c/f_o$, gives the number of wavelengths of received phase offset and multiplying by 2π gives the phase function in radians.

$$p(t) = 2\pi \frac{f_o}{c} [r_o + \dot{r}t + \ddot{r} \frac{t^2}{2} + \ddot{\ddot{r}} \frac{t^3}{6}] \text{ radians} \quad (\text{E-2})$$

The corresponding doppler frequency is

$$f(t) = \frac{f_o}{c} [\ddot{r} + \ddot{\ddot{r}}t + \ddot{\ddot{\ddot{r}}} \frac{t^2}{2}] \text{ by} \quad (\text{E-3})$$

where

- $f_d = \frac{f_o}{c} \dot{r}$ = Initial Doppler Frequency
- $\dot{f}_d = \frac{f_o}{c} \ddot{r}$ = Doppler Rate
- $\ddot{f}_d = \frac{f_o}{c} \ddot{\ddot{r}}$ = Doppler Acceleration

A second-order PLL, with perfect integrator, can track the doppler rate with a steady-state error. A third-order PLL is required in order to track the doppler acceleration, i.e., range jerk. However, a second-order FLL can track a jerk. Therefore, RMS frequency errors for the 3rd-order PLL and 2nd-order FLL will be compared using the jerk optimized loop bandwidths. Table E-1 compares tracking capabilities of the PLL and the FLL. The 3rd-order PLL may not be used during acquisition due to its stability problems at low input signal level. A 2nd-order loop would be used during acquisition and the 3rd-order PLL switched in for tracking.

In this memo, suppressed carrier signals are considered therefore I-Q loops will be used. The I-Q PLL, commonly called the Costas PLL will be denoted as CPLL and the I-Q FLL as IQFLL. A detailed analysis of these loops has been performed by Huang [2]. He derived expressions for mean-square frequency error and his results will be incorporated in this memo. His results lacked information concerning selection of loop bandwidths without which a meaningful comparison of the CPLL and the IQFLL is difficult. A criterion for selection of the loop bandwidths is presented here. Block diagrams of these loops are given in Figures E-1 and E-2.

For a phase coherent communication system the IQFLL, since it has an indeterminate phase error, would have to be used in conjunction with a PLL. The advantage of this procedure is that the IQFLL does not suffer from cycle-slipping as does the CPLL and therefore may acquire much faster depending on input SNR and loop bandwidth. The frequency output of the IQFLL could be used to adjust the CPLL VCO frequency. For a noncoherent receiver an IQFLL alone would be sufficient since the carrier must only be acquired and tracked to keep it within the IF bandwidth. This option, of course, assumes that the operating conditions are such that the IQFLL frequency jitter, determined herein, is not excessive.

[2] Huang, T.C., "Analysis of an I-Q Frequency Locked Loop," TRW IOC 7333.3-372, February 12, 1975.

Table E-1. Effects of Signal Dynamics FLL vs PLL

HIGHEST ORDER EFFECT	LOOP FILTER		LOOP ORDER	STEADY STATE ERROR	
	FLL	PLL		FLL	PLL
DOPPLER OFFSET	$\frac{S+A}{S}$	1	1	0	CONSTANT
DOPPLER OFFSET	$\frac{S+A}{S^2}$	$\frac{S+A}{S}$	2	0	0
DOPPLER RATE	$\frac{S+A}{S}$	1	1	CONSTANT	INCREASING
DOPPLER RATE	$\frac{S+A}{S^2}$	$\frac{S+A}{S}$	2	0	CONSTANT
DOPPLER ACCELERATION	$\frac{S+A}{S^2}$	$\frac{S+A}{S}$	2	CONSTANT	INCREASING
DOPPLER ACCELERATION	$\frac{S+A}{S^3}$	$\frac{S+A}{S^2}$	3	0	CONSTANT

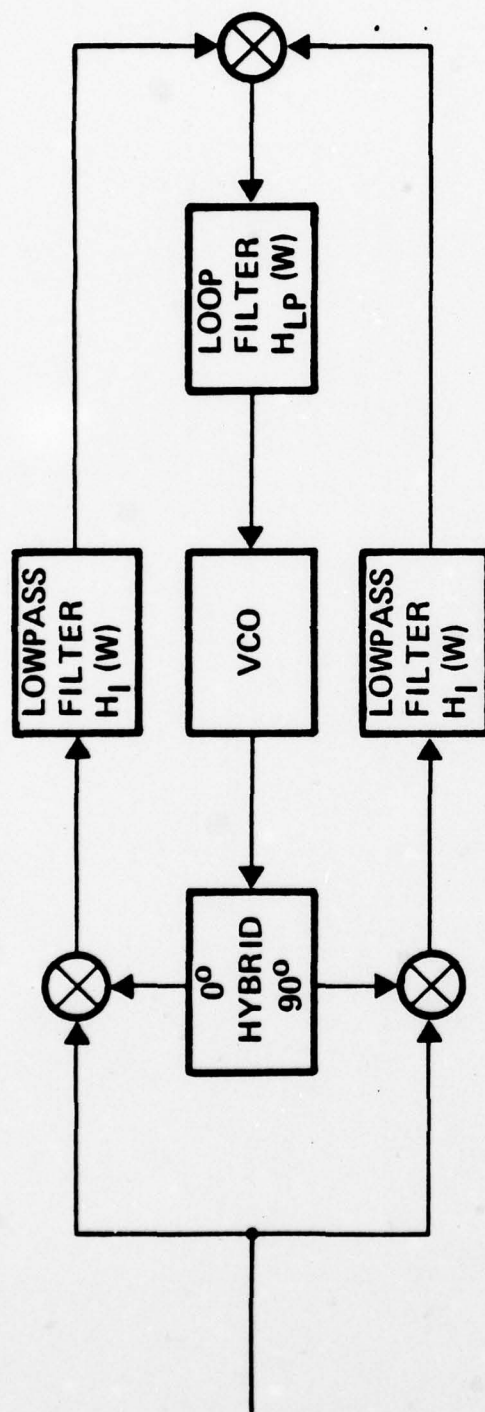


Figure 1. Costas Phase-Locked Loop

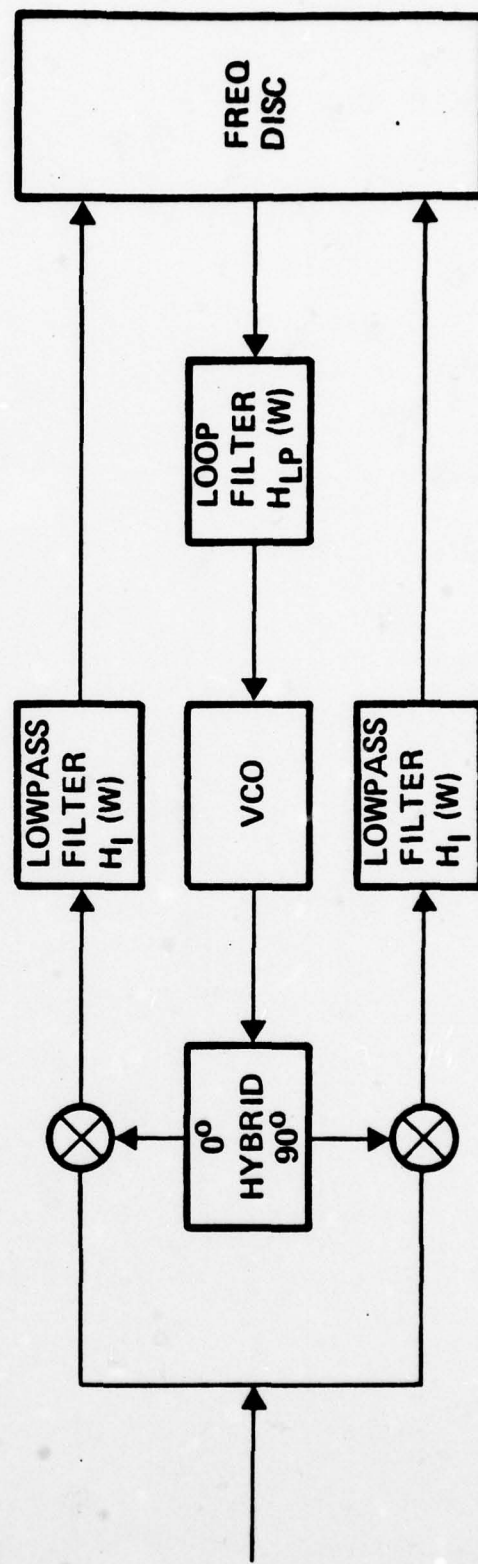
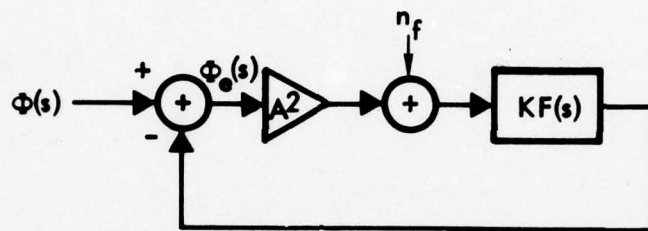
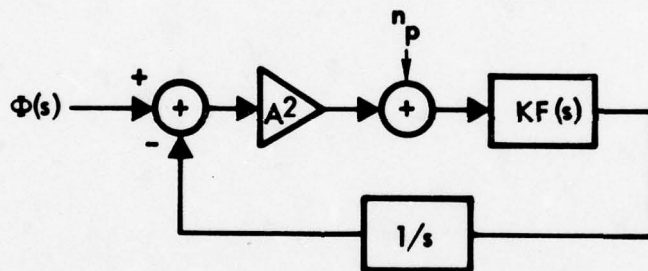


Figure E-1. I-Q Frequency-Locked Loop



IQFLL ANALYTICAL MODEL



CPLL ANALYTICAL MODEL

Figure E-2. Tracking Loop Models

II. RMS Frequency Error for Second Order Loops

Denoting the loop input as

$$x(t) = A \cos[\phi(t)] + n(t) \quad (E-4)$$

where $\phi(t) = \omega_0 t + p(t) + \theta$

$p(t)$ = doppler phase function

θ = initial phase offset not included in $p(t)$

the stochastic differential equations describing the loops may be written as

$$\text{IQFLL: } s\phi_e(s) = s\phi(s) - KF(s) [A^2 s\phi_e(s) + \text{Frequency Noise}] \quad (E-5)$$

$$\text{CPLL: } s\phi_e(s) = s\phi(s) - KF(s) \left[\frac{A^2}{2} L[\sin 2\phi_e(t)] + \text{Phase Noise} \right] \quad (E-6)$$

where $\phi_e(t) = L^{-1}[s\phi_e(s)]$ = Frequency Error

$\phi(t) = L^{-1}[s\phi(s)]$ = Input Frequency

L^{-1} = Inverse Laplace Transform

Linearizing the CPLL equation by assuming a small phase error it may also be written in terms of phase error as:

$$\text{CPLL: } \phi_e(s) = \phi(s) - K \frac{F(s)}{s} [A^2 \phi_e(s) + \text{Phase Noise}] \quad (E-7)$$

Equations (E-5) and (E-7) may be depicted by the models given in Figure E-2. The describing equation for the IQFLL and the CPLL may be solved for the frequency error and phase error, respectively.

$$\text{IQFLL: } s\phi_e(s) = [1 - H_F(s)] s\phi(s) - H_F(s) \frac{\text{Frequency Noise}}{A^2} \quad (E-8)$$

where $H_F(s) = \frac{KA^2 F(s)}{1 + KA^2 F(s)}$ IQFLL Loop Transfer Function

$$\text{CPLL: } \phi_e(s) = [1 - H_C(s)] \phi(s) - H_C(s) \frac{\text{Phase Noise}}{A^2} \quad (E-9)$$

where $H_C(s) = \frac{KA^2 F(s)}{s + KA^2 F(s)}$ = CPLL Loop Transfer Function

The frequency error variance for the IQFLL may be written as

$$\sigma_{\dot{\phi}_F}^2 = \sigma_{\dot{\phi}_{Fd}}^2 + \sigma_{\dot{\phi}_{Fn}}^2 \quad (E-10)$$

where $\sigma_{\dot{\phi}_{Fd}}^2$ = dynamic frequency error variance for IQFLL

$\sigma_{\dot{\phi}_{Fn}}^2$ = noise frequency error variance for IQFLL

Similarly for the CPLL the frequency error variance is denoted as

$$\sigma_{\dot{\phi}_C}^2 = \sigma_{\dot{\phi}_{Cd}}^2 + \sigma_{\dot{\phi}_{Cn}}^2 \quad (E-11)$$

where $\sigma_{\dot{\phi}_{Cd}}^2$ = dynamic frequency error variance for CPLL

$\sigma_{\dot{\phi}_{Cn}}^2$ = noise frequency error variance for CPLL

Huang [2] gives expressions for the noise frequency error variances for both loops. They are derived by finding the spectral densities of the equivalent frequency and phase noises and then integrating over the loop bandwidth to obtain the variances. Only the results will be given here. The equivalent noise spectra will depend on the bandwidth and shape of the input loop filters. Huang gives results for three filter types: Ideal rectangular, Gaussian shape, and first-order RC. The first-order RC filter gives minimum error variance and therefore results for this filter shaping will be used. The bandwidths are two-sided noise bandwidth. For the input filter $B_1 = \pi f_c$ where B_1 is the two-sided noise bandwidth in hertz and f_c is the 3 dB (single-sided) cutoff frequency, the frequency error variances are

$$\sigma_{\dot{\phi}_{Fn}}^2 = \frac{B_1 B_L}{2R\pi^2} \frac{\left[1 - \frac{2B_1}{\pi B_L} \tan^{-1} \left(\frac{\pi B_L}{2B_1}\right) + \frac{1}{R} - \frac{B_1}{RB_L} \tan^{-1} \left(\frac{\pi B_L}{4B_1}\right)\right]}{\left[1 - \frac{1}{R} \tan^{-1} \left(\frac{\pi B_L}{2B_1}\right)\right]} \quad (E-12)$$

for the IQFLL and

$$\sigma_{\dot{\phi}_{Cn}}^2 = \frac{B_1 B_L}{2R\pi^2} \left[1 - \frac{2B_1}{\pi B_L} \tan^{-1} \left(\frac{\pi B_L}{2B_1}\right)\right] + \frac{B_1 B_L}{\pi^2 R^2} \left[1 - \frac{4B_1}{\pi B_L} \tan^{-1} \left(\frac{\pi B_L}{4B_1}\right)\right] \quad (E-13)$$

for the CPLL where

$$B_L = \text{two-sided loop noise bandwidth, Hz} \quad (\text{E-14})$$

$$R = P_s/P_n = A^2/2B_1N_0 = \text{input carrier-to-noise power ratio} \quad (\text{E-15})$$

The variances may also be expressed in terms of a carrier-to-noise density ratio by defining $CNO = R \cdot B_1$.

The input bandwidth, B_1 , for both loops will be chosen to correspond to the input frequency uncertainty. The loop bandwidth, B_L , must be chosen so as to optimize the tradeoff between its effect on the error variance due to input noise and the error variance due to input signal dynamics. This may be done by choosing the bandwidth which minimizes the expressions given by Eq. 10 and 11. One approach is to choose the bandwidth which makes the frequency (or phase) noise variance equal to some function of the dynamic frequency (or phase) error. The square of the peak or steady-state error will be used as the dynamic error function. If the steady-state error is zero (this will depend on the assumed input dynamics and the loop filter transfer function) the peak squared will be used. Note that if the dynamic error function used were the (time) average of the squared dynamic error this procedure would correspond to minimizing Equations (E-10) and E-11).

Since second-order loops are considered in this section a frequency ramp (i.e., doppler rate) input will be considered as the highest order effect. For the IQFLL the loop filter will be $F(s) = sta/s^2$ and for the CPLL $F(s) = sta/s$. For the IQFLL from Eq. (E-8) the dynamic frequency error becomes

$$\dot{\phi}_{Fde}(t) = L^{-1} \left[\frac{s^2}{s^2 + KA^2(sta)} s\phi(s) \right] \quad (\text{E-16})$$

and from Eq. (E-3) $\phi(s) = L[\dot{f}dt] = \dot{f}d/s^2$. Using the final value theorem

$$\lim_{t \rightarrow \infty} \dot{\phi}_{Fde}(t) = \lim_{s \rightarrow 0} s \left(\frac{s^2}{s^2 + KA^2(sta)} \right) \frac{\dot{f}d}{s} = 0. \text{ The peak value of}$$

the frequency error will now be found.

$$\dot{\phi}_{Fde}(t) = L^{-1} \left[\frac{s}{s^2 + KA^2s + KA^2a} \right] = \dot{f}d \frac{1}{\sqrt{KA^2a - 0.25K^2}} e^{-\frac{1}{2}Kt} \sin \sqrt{KA^2a - 0.25K^2}t$$

Finding the maximum of this function gives the dynamic error peak frequency

$$\dot{\phi}_{F,dep} = \frac{f_d}{\sqrt{KA^2a - 0.25K^2A^4}} e^{-\pi/4} \sin \frac{\pi}{4} = 0.322 f_d / \sqrt{KA^2a - 0.25K^2A^4} \quad (E-17)$$

This equation may be written in terms of loop noise bandwidth by evaluating the integral given in Eq. (E-14). It may also be found by equating the denominator of the loop transfer function to $s^2 + 2\rho\omega_n s + \omega_n^2$ and determining the natural frequency ω_n , and the damping factor, ρ , in terms of the loop parameters: A, K and a. Doing this gives $\sqrt{KA^2a - 0.25K^2A^4} = \sqrt{\omega_n^2 - \rho^2\omega_n^2} = \omega_n/\sqrt{2}$. The second equality results from setting $\rho = 1/\sqrt{2}$ as is often done in practice. This choice of ρ gives reasonable performance in terms of dynamic overshoot characteristics and is the optimum value when a second-order loop is used to minimize mean-square-error for a frequency-step input. It may then be shown that

$$\begin{aligned} B_L &= \frac{\omega_n [4\rho^2 + 1]}{4\rho} \\ &= \frac{3}{4} \sqrt{2} \omega_n = 1.06\omega_n \text{ for } \rho = \frac{1}{\sqrt{2}} \end{aligned} \quad (E-18)$$

Using these results in Equation (E-17) gives

$$\dot{\phi}_{F,dep} = \frac{f_d}{2.07B_L} \quad (E-19)$$

The following equation is then solved for B_L as a function of CNo, f_d , and B_1

$$[\dot{\phi}_{F,dep}(f_d, B_L)]^2 = \sigma_{\dot{\phi}_{Fn}}^2 (B_1, B_L, CNo). \quad (E-20)$$

This equation may be solved graphically. Figure E-3 gives the optimized loop bandwidth versus CN_0 . Using these bandwidths the RMS frequency error is plotted versus CN_0 in Figure E-4.

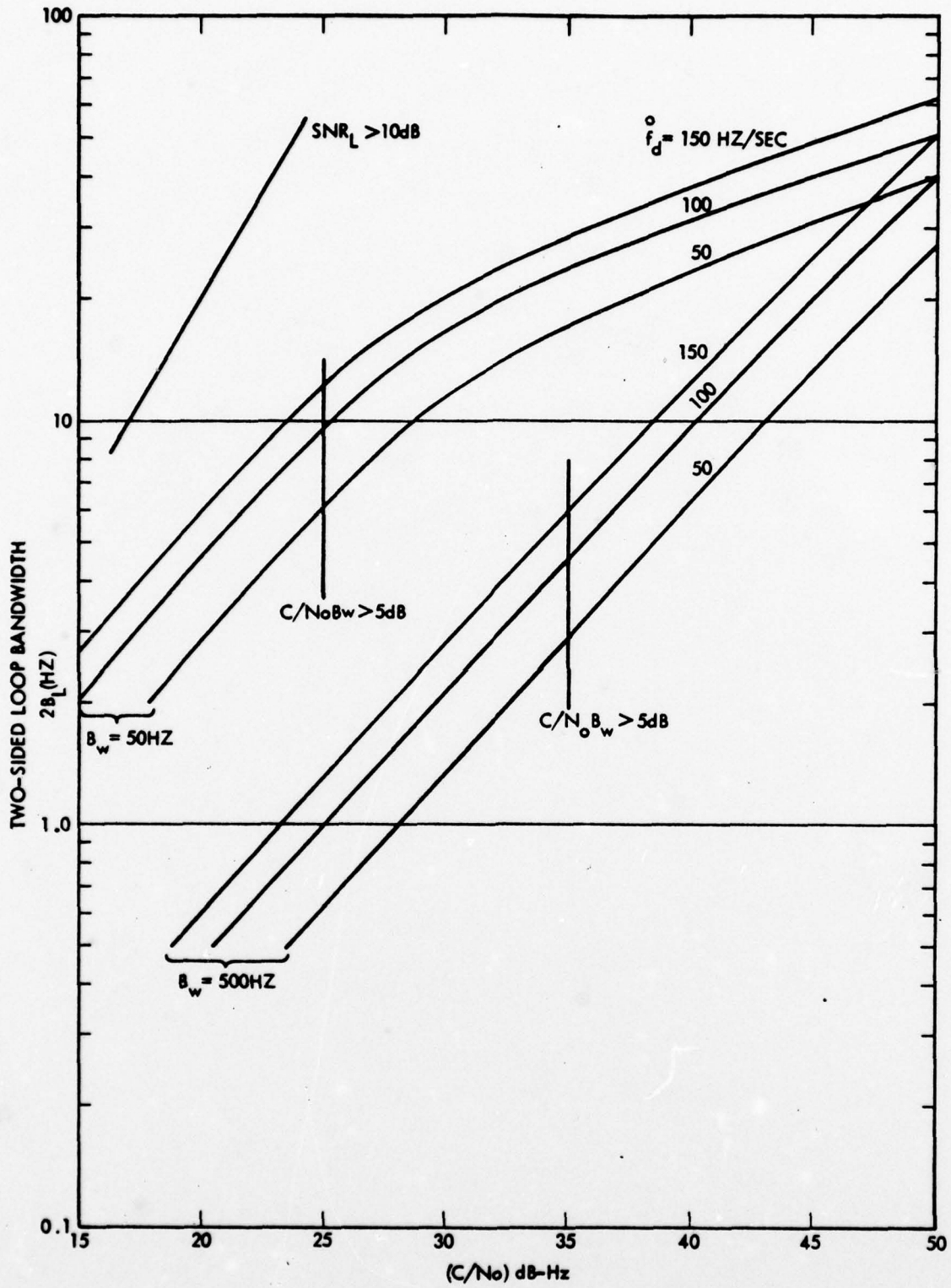


Figure E-3. FLL Optimized Loop Bandwidth vs C/N_0

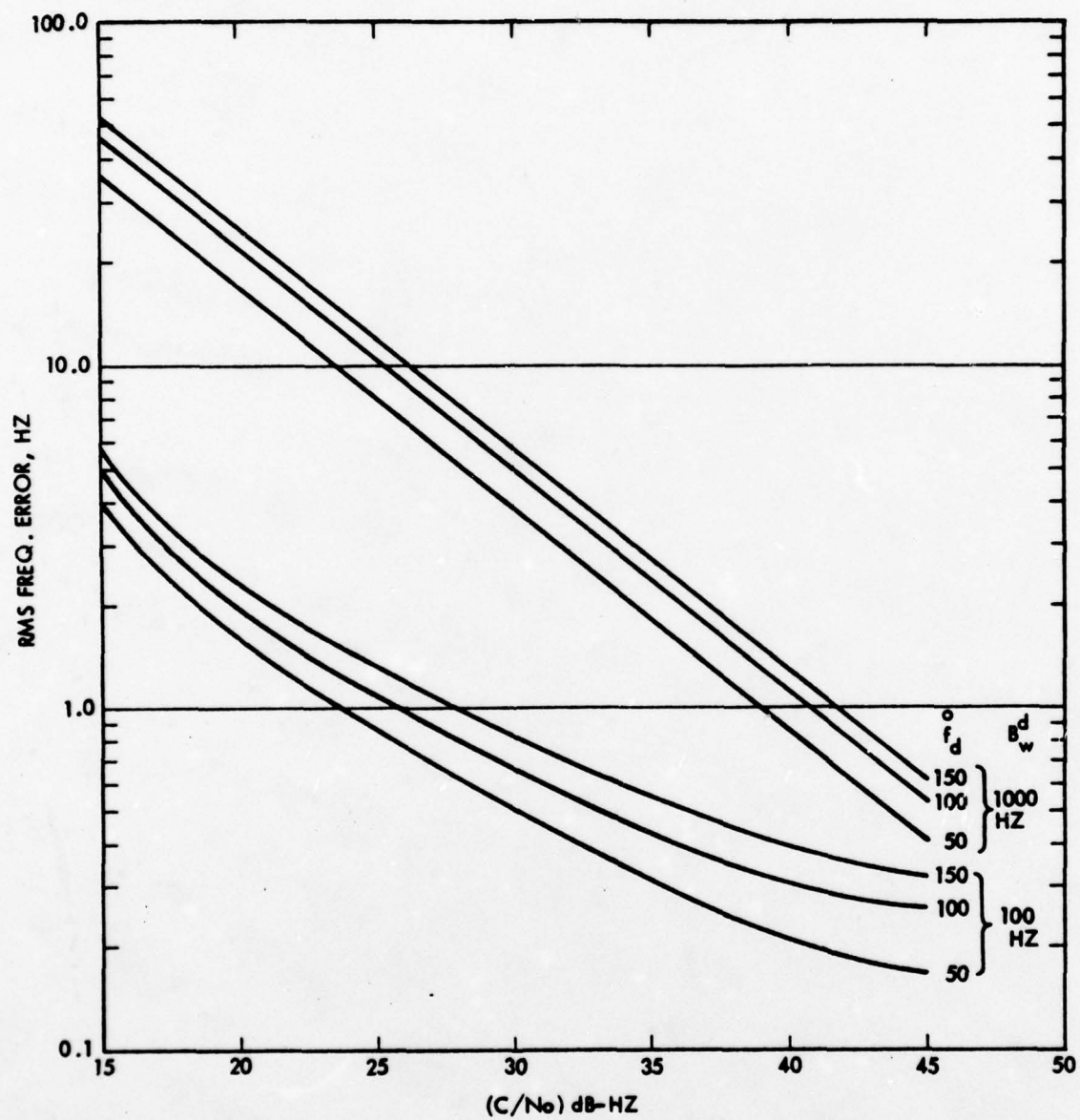


Figure E-4. Second-Order Frequency Lock Loop RMS Frequency Error vs C/N_0 (Using Optimized B_{LP})

A similar procedure is used to find the optimized loop bandwidth and corresponding RMS frequency error for the second-order CPLL. The steady-state dynamic phase noise error and the optimized B_L determined. The dynamic phase error is

$$\phi_{c,de}(t) = L^{-1}[(1 - H_c(s))\phi(s)] \quad (E-21)$$

and with $F(s) = \frac{s+a}{s}$ and $\phi(s) = \frac{\dot{f}d(2\pi)}{s^3}$

$$\phi_{c,de}(t) = L^{-1}\left[\frac{2\pi\dot{f}d/s}{s^2 + KA^2s + KA^2a}\right] \quad (E-22)$$

The steady-state phase error is

$$\text{s.s. } \phi_{c,de} = \lim_{t \rightarrow \infty} \phi_{c,de}(t) = \frac{2\pi\dot{f}d}{KA^2a}, \text{ radians.} \quad (E-23)$$

Again using $\rho = 1/\sqrt{2}$ gives

$$\text{s.s. } \phi_{c,de} = 7.07 \frac{\dot{f}d}{(B_L)^2} \quad (E-24)$$

The variance of the phase noise, since it is not given by Huang, will be derived here. He gives the equivalent phase noise spectrum for RC filtering as

$$\frac{S_{N_c}(\omega)}{A^4} = \frac{N_o}{A^2} \frac{2B_1^2}{\omega^2 + 4B_1^2} + \frac{N_o^2}{A^4} B_1^3 \frac{16}{\omega^2 + 16B_1^2} \quad (E-25)$$

which may be written as

$$\frac{S_{N_c}(\omega)}{A^4} = \frac{1}{CN_o} \frac{2B_1^2}{\omega^2 + 4B_1^2} + \left(\frac{1}{CN_o}\right)^2 \frac{4B_1^3}{\omega^2 + 16B_1^2} \quad (E-26)$$

Therefore,

$$\sigma_{\phi_{cn}}^2 = \frac{1}{2\pi} \int_{-\pi B_L}^{\pi B_L} \frac{S_{N_c}(\omega)}{A^4} d\omega$$

$$= \frac{1}{\text{CN}_0} \frac{B_1}{\pi} \tan^{-1} \left(\frac{\pi B_L}{2B_1} \right) + \left(\frac{1}{\text{CN}_0} \right)^2 \frac{B_1^2}{\pi} \tan^{-1} \left(\frac{\pi B_L}{4B_1} \right), \text{ rad}^2 \quad (\text{E-27})$$

Equating $\phi_{\text{C,de}}^2$ and $\sigma_{\phi\text{CN}}^2$ gives the optimized loop bandwidth. The results are shown in Figure E-5 for three values of doppler rate. The resulting RMS frequency error, from Equation (E-13), is given in Figure E-6.

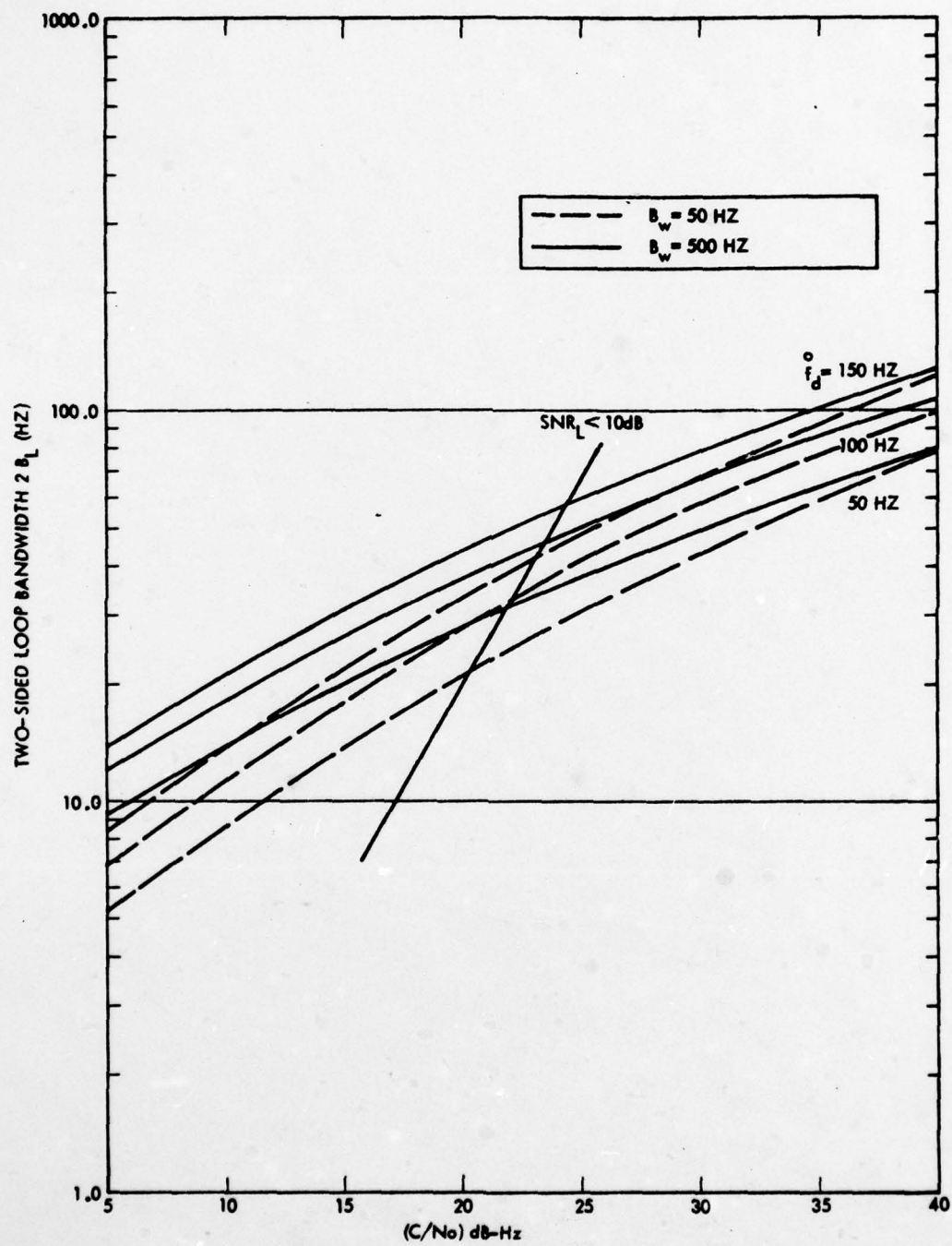


Figure E-5. Optimized Second-Order Costas Loop Bandwidth vs C/N_0

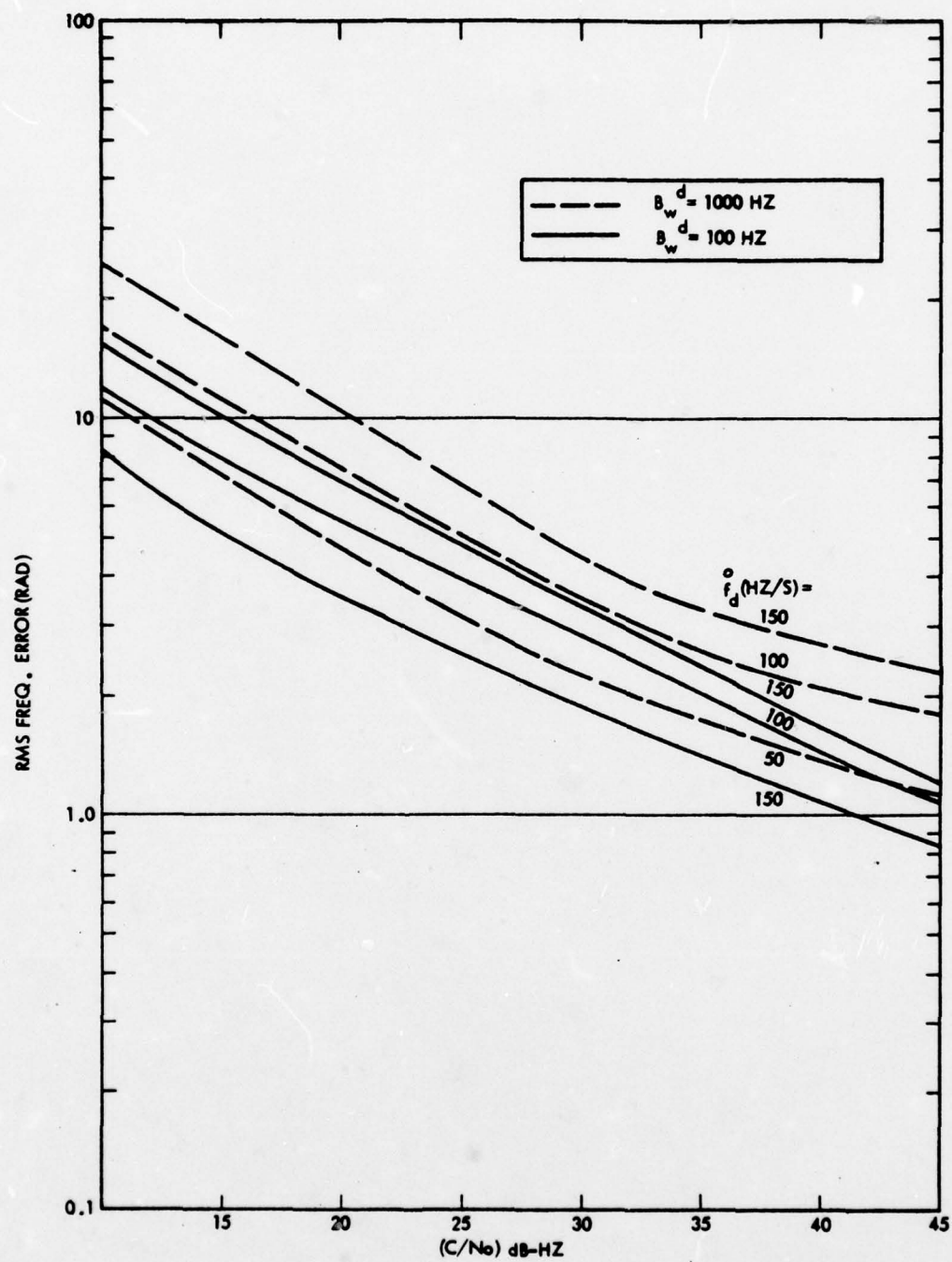


Figure E-6. Second-Order Costas Loop RMS Frequency Input C/N_0 (Using Optimized B_{LP})

APPENDIX F

MICROPROCESSOR ARCHITECTURE

F.1 MICROPROCESSOR ARCHITECTURE

A key item in the modem is the micro-signal processor. A study was conducted for microprocessor architecture determination and other processor organization considerations.

MICROPROCESSOR ARCHITECTURE DETERMINATION

The fundamental decisions and factors involved in determining the processor architecture from system requirements to the hardware implementation are depicted in Figure F-1. The system requirements characterize the processing algorithms as to processing time allowed and operations per second. The algorithms in turn determine whether a general-purpose or special-purpose processor can be used. The general-purpose processor has a more programmable computer orientation, while the special-purpose processor is optimized to a single application. Very high-speed processing usually requires a special-purpose processor.

The general-purpose processor selection then requires an investigation into processor architecture - both internal structure and whether more than one processor is necessary. This, of course, is an iterative process. Multiple processor arrays have advantages in high data processing capability and if redundancy for reliability enhancement is required, but additional complexity is the penalty. Central processor architectures are the focal point of almost all processor architectures. Classification is by serial, pipeline, parallel, and array processor. The base is the data flow (singular or multiple) between building blocks and the central processor control, again whether singular or multiple.

The serial configuration has a single data path between the data storage and the central processor or the computing function. The control signals (or instructions) emanate from a single control memory and are executed sequentially. This is the more frequently used organization, due to the straightforward concepts.

The pipeline organization uses a single data path but requires multiple instructions for processing. The computing function is divided into identical serially con-

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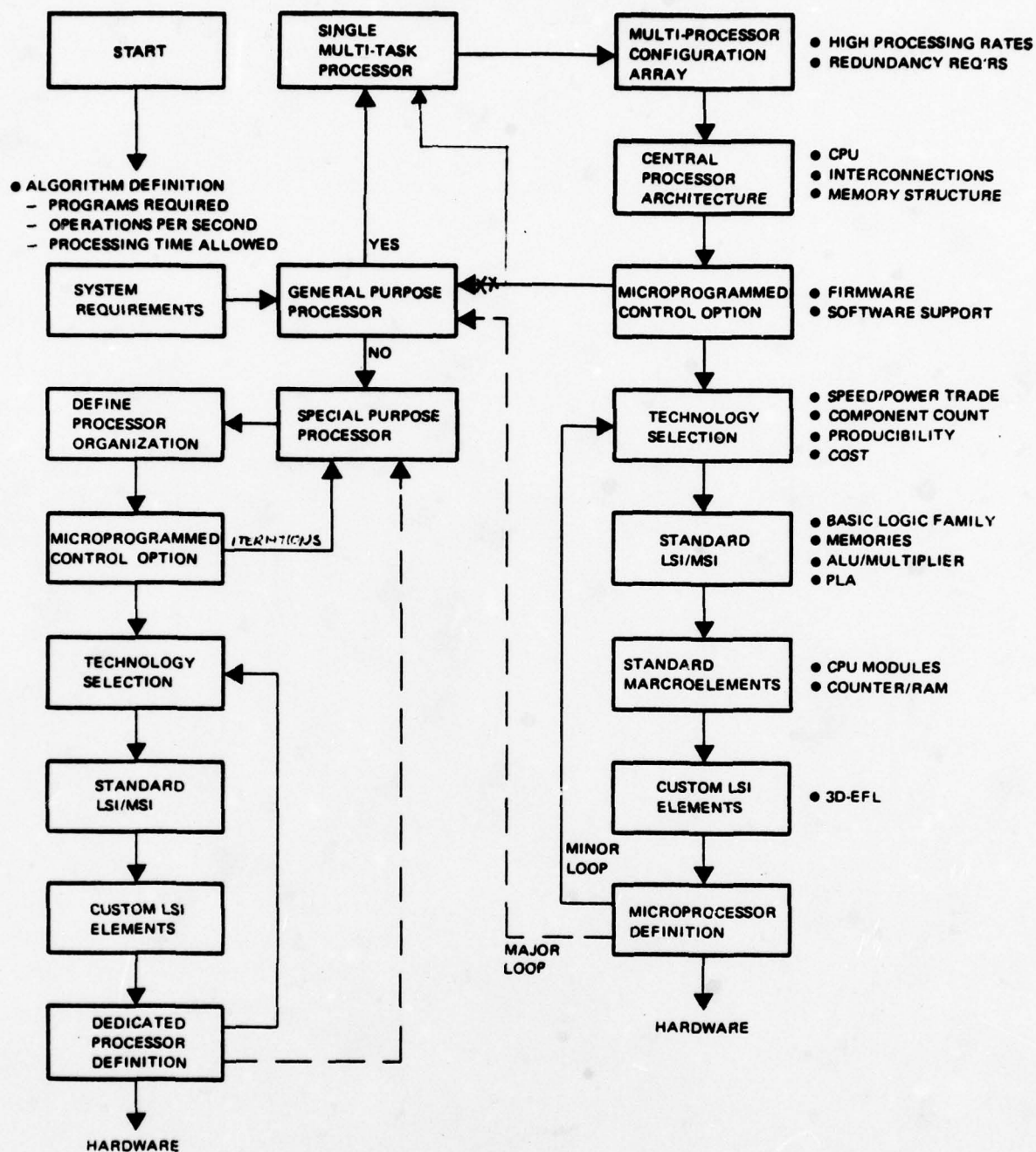


Figure F-1. Processor System Definition

nected modules, each time division multiplexed and doing a part of the same on-going task. Algorithms that require continuous, fast, multi-step processing with few feed-back iterations can be readily applied to this configuration.

The parallel processor processes data in separate independent functions. There are multiple data paths and instructions. The multiple instructions allow different operations in each function to occur concurrently. Operational processing rates can be enhanced by a factor of N if there are N parallel functions. Maximum flexibility in function allocation by task is obtained due to this independence. The array is a simplification of the parallel processor. Multiple data paths interconnect the functions, but a single instruction provides control. The computing function is divided into modules of equal capability but arranged in parallel. The same instruction is executed by all functions simultaneously. This reduces the control complexity while retaining the parallel improvement factor.

The microprocessor control section generally uses microprogramming as a substitute for hardwired control logic. The microprograms consist of instructions (or microinstructions) that provide all the control and selection signals to the control processor, data storage and input/output. Additionally, address information for branching and indirect addressing is generated. The microinstructions containing control/addresses are stored in program memories which can be either RAM/s or ROM/s, depending on the permanence and maturity of the application program.

Microprogramming techniques are used because of the efficiencies and economics of handling firmware as opposed to conventional random logic. The control section of a non-microprogrammed processor tends to be complex, due to the logic networks required. Using microprograms, the control is simplified. Randomness remains, but only stored as random data in the program memory — not as an unstructured logic network. The flexibility of microprogramming is considered to be its major advantage. The user can modify his microprogram to tailor it to the particular application — thereby spanning a multitude of applications and minimizing design and total costs.

After the architecture has been selected, the basic technology of the processor elements is determined primarily based on element, speed of operation, associated power dissipation, total parts count, cost, and availability. These elements are derived from the candidate architecture and are consistent with the system/algorithm requirements.

A hardware hierarchy is evident with processor configurations and can be classified as follows:

Logic components	MSI as part of logic families
Elements	Higher integration such as LSI
Modules	Conglomeration of LSI or VLSI (very large-scale integration)

The elements and logic combine to form modules which are the major determinants of the architecture.

The speed-power requirements bound the basic logic family that can be used. Medium to high-speed technologies include emitter coupled logic (ECL), Schottky TTL, and low-power Schottky TTL. Schottky TTL is about a 100 MHz family and used for high-speed applications. Low-power Schottky TTL is intended for low cost, medium-speed processor being a 30 MHz family and one-fifth the Schottky power dissipation. It is interchangeable with Schottky TTL directly. ECL is almost 50% faster than Schottky and dissipates about the same power but is not interchangeable with any TTL family.

The standard off-the-shelf LSI selection is based on function performed, availability, as well as the logic family criteria. Memories and arithmetic logic units (ALU's) fall in this category. It is cost-effective and simple in design to incorporate these elements into processors. A level above this, called "macrologic," involves elements combined as a modular function. These include counter and RAM combinations, as well as the CPU or "computer on a chip" modules. High device density on a single integrated circuit is a requirement for these functions, thereby reducing component totals.

To further reduce the total component count, custom LSI is next considered. Custom LSI is used as a complementary function to standard LSI for elements not available. When large unit production quantities are required, say greater than 1000 units, custom LSI becomes attractive from a cost standpoint. Lower cost in parts reduction and assembly become evident.

Custom LSI considerations include functional partitioning, packaging and utilization. The functional partitioning is a detailed definition of internal interconnections, interface signals (control, data, clock, and addressing), other element interface compatibility, and logic/circuit boundary complexity. The LSI packaging concepts must be well integrated with the partitioning to generate viable elements. Size, power accommodation, interconnect limitations, both internal and external, and producibility will be major concerns.

As an example, triple diffused emitter follower logic (3D-EFL), developed at TRW, meets the need for a custom LSI technology with the higher speed of bipolar technology but the high device densities and high yield capability of MOS technology. The 3D-EFL density is comparable to MOS and its fabrication sequence is correspondingly simple. This technology can operate at data rates from near dc to 30 MHz.

The special purpose segment of the processor system definition involves similar tasks as for the general purpose approach. The technology selection through the hardware hierarchy is the same except for the standard macro-elements probably not being applicable due to their general purpose nature. The processor organization more closely follows the algorithm data flow with much less flexibility for changes and use with other applications. If a microprogrammed control is used, as in a controller mode, some adaptability is retained, although in very high speed applications a fixed control

is generally used. The net result is a processor organization somewhat optimized and dedicated to a single algorithm.

PROCESSOR CONFIGURATIONS

Processor System Definition

A major consideration underlying the applications analysis is whether a special purpose processor is more optimum than a "general purpose" microprocessor. A microprocessor has the advantage of programmability spanning many applications and is modular and expandable. When multiple algorithms and tasks can be processed with many inputs and outputs and multi-decision paths, then a microprocessor is used effectively. Implicit is the use of large data storage or memories.

A special purpose, non-programmable, hard wired configuration processor is used, where a repetitive singular function or task is required. A simple one-of-its-kind unit should consider a special purpose processor also. If very high speed operation is required, arbitrarily in excess of 50% of the maximum microprocessor capability, then a microprocessor is marginal. Capability here is measured in operations or instructions per second.

The allocation of applications programs will be based on the preliminary data processing requirements such as input/output data rate, instructions required per algorithm, data storage capacity including permanent storage (read-only memories), and operational duty cycle. The latter is a figure of merit involving the total micro-signal-processor utilization. This parameter is defined herein as the ratio of program processing time to the total micro-signal-processor time available for data processing, times 100 percent.

$$\text{Processor Utilization} = \frac{N \times T_{mp}}{T_o} \times 100$$

where N = number of instructions executed

T_{mp} = basic micro-signal-processor cycle time

T_o = time allowed for processing on a periodic basis --
can use a time slot basis or the inverse of the input
data rate.

Note that $N \times T_{mp}$ is the time required to process a given algorithm.

As an example:

$$\text{Processor Utilization} = \frac{10 \times 50 \times 10^{-9} \text{ sec}}{1 \times 10^{-6} \text{ sec}} \times 100 = 50\%$$

where $N = 10$ instructions

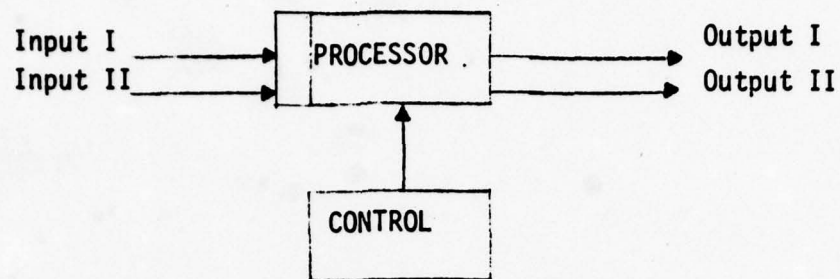
$T_{mp} = 50$ nanoseconds basic cycle

$T_o =$ the inverse of 1 MHz

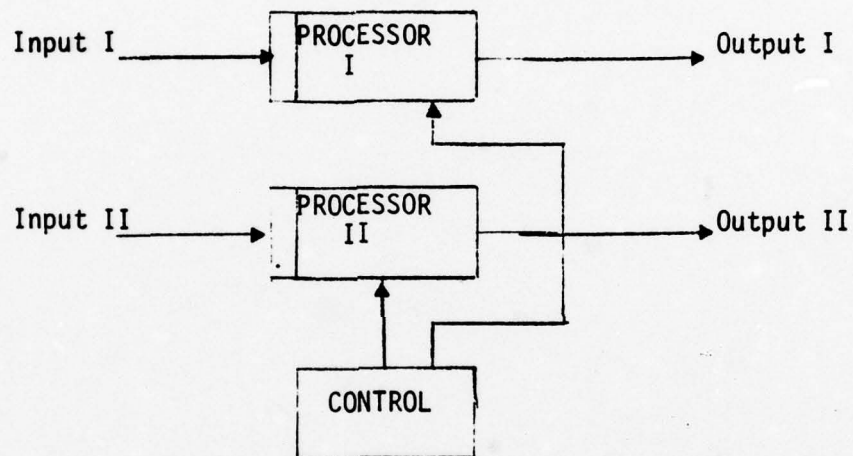
If the capability of a micro-signal-processor is exceeded or has a small margin (<10%), then a viable alternative is to use multiple processor organizations. Refer to Figure F-2. The centralized microprocessor operates on multiple real time tasks to effect maximum utilization or minimum idle time with margin. This uses a single microprocessor on a time-shared basis.

The multiple microprocessor configuration in Figure F-2b improves the processing limits by a factor of two. If each processor is capable of 20×10^6 instructions per second (or 20 MIPS) then the combination ranges up to 40 MIPS. Each processor can be considered to be a module that is readily expandable with the incremental speed improvements. The centralized control of the processors, both hardware and software, becomes more complex due to the input/output scheduling and prioritizing. The processors can be merged and replicated only on an element level, such as random access memories. The finer control and modularity is somewhat offset by the internal software overhead of usage status, memory management -- storage sector allocation, and access priorities.

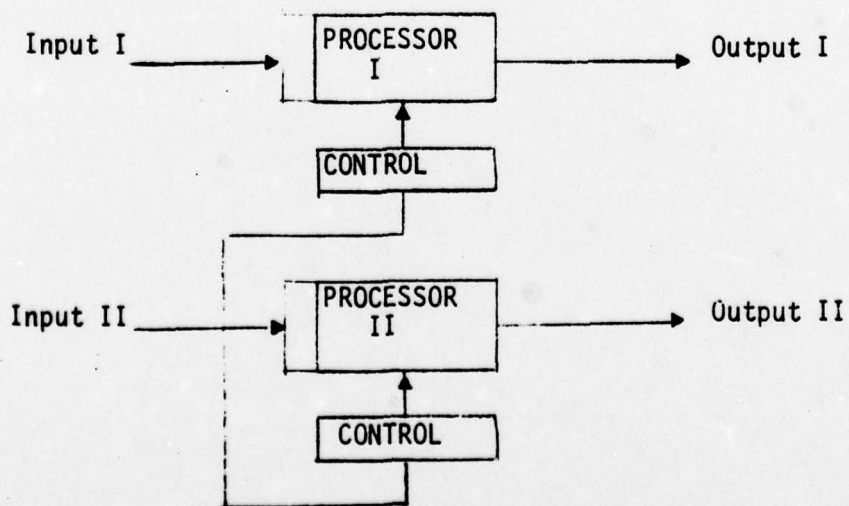
Another approach is the Federated microprocessors illustrated in Figure F-2c. Each microprocessor is completely self-contained as a module. Each can operate independently or be linked to the other by the input/output control signals. When an input is ready for a transfer, the request is honored by the first processor and all other inputs are inhibited. This is to avoid duplicate processing in optimizing program allocations. If the first processor is busy processing an on-going program, then the request is shifted to the second processor. No transfers occur if both are busy. This is the most flexible approach for a large system. But high data transfer rates and multiple real time input/output conflicts can cause processing scheduling difficulties. Another linking is to use the master-slave concept. A processor is designated the "master" unit while all others are "slaves". The master processor is the director and resolves allocation conflicts. All interface control must now be routed through the master processor with the attendant increase in complexity.



(a) CENTRALIZED MICRO PROCESSOR



(b) MULTIPLE MICROPROCESSORS



(c) FEDERATED MICRO PROCESSORS

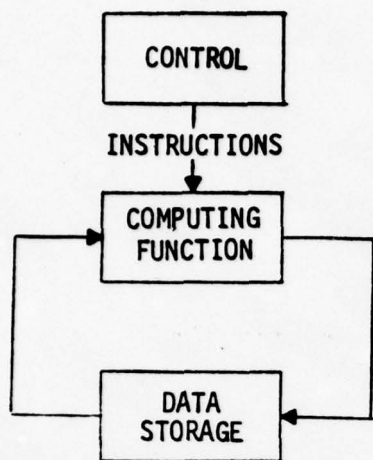
Processor Architecture

The architecture herein relates to the basic components or building blocks (computation, data storage, control and input/output) that are required in processors and the connections required. The configuration of the building blocks is the ultimate determinate factor of the program processing performance given the implementation technology. Processors will be optimized for the given classes of algorithms with emphasis on basic elements, commonality, and a general purpose micro-signal-processor.

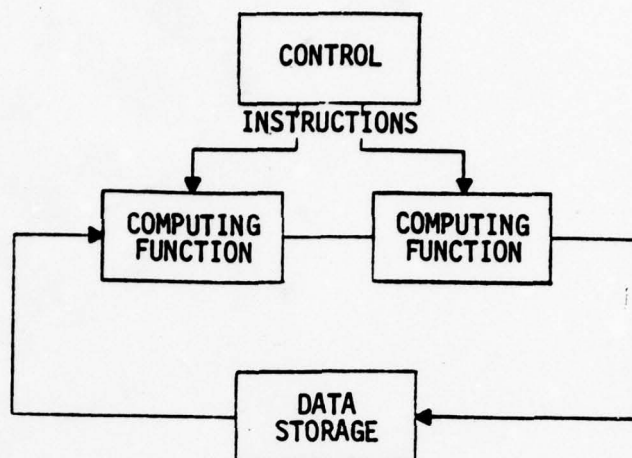
The computing function organization is the focal point of almost all processor architectures. The computing function can be classified as serial, pipeline, parallel and array. The basis is the data flow (singular or multiple) between building blocks and the computation control (again, whether singular or multiple). Refer to Figure F-3.

The serial organization is depicted in Figure F-3(a). All the essential processor functions are shown except the input/output interface. The computing function provides all the arithmetic operations and data manipulation capability. The data storage is the memory for program and data retention and retrieval. The control generates timing and control signals or instructions in the case of a programmable control. The data flow between the computations and storage is a single data path; and the singular control instructions are executed sequentially. The computation-storage interconnections can be fixed to accommodate a given class of algorithms or flexible as in the data bus concept for more generalized use. This is the most frequently used organization due to the straightforward concepts.

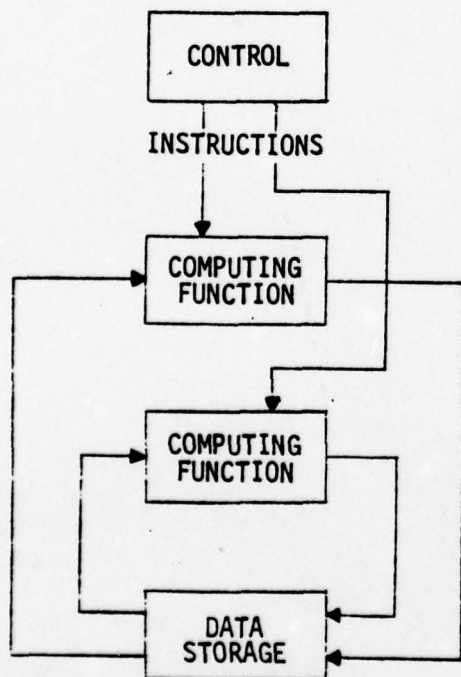
The pipeline organization [Figure F-3(b)] uses a single data path but requires multiple instructions for processing. The computing function is divided into identical serially connected modules, each time-division multiplexed and doing a part of the same on-going task. The output of



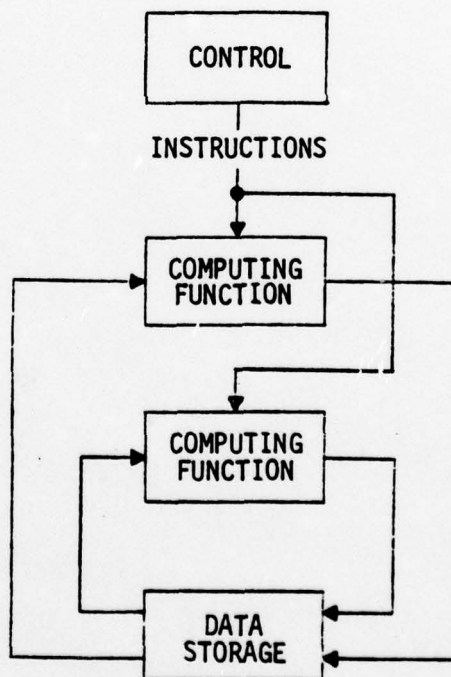
(a) SERIAL



(b) PIPELINE



(c) PARALLEL



(d) ARRAY

FIGURE F-3. COMPUTING FUNCTION ORGANIZATION

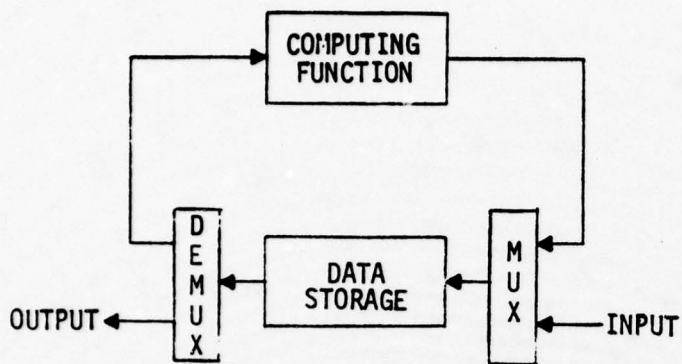
computation is passed to the next module in line with all modules operating concurrently. Algorithms that require continuous fast multi-step processing with few feedback iterations, can be readily applied to this configuration.

The parallel organization [Figure F-3(c)] processes data in separate independent functions. There are multiple data paths (computation-storage) and multiple instructions. The multiple instructions allow different operations in each function to occur concurrently such as an addition and multiply. The storage is shown as having two inputs and two outputs with interval partitioning. Two separate memories could also have been used. Operational processing rates can be enhanced by a factor of N if N functions are processing in parallel. Maximum flexibility in function allocation by task is obtained due to this independence.

The array organization is a simplification of the parallel configuration. Refer to Figure F-3(d). Multiple data paths interconnect the computation function and storage but a single instruction provides the timing and control. The computation is divided into modules of equal capability but arranged in parallel. The same instruction is executed by all functions simultaneously. This reduces the control complexity while retaining the parallel processing improvement factor.

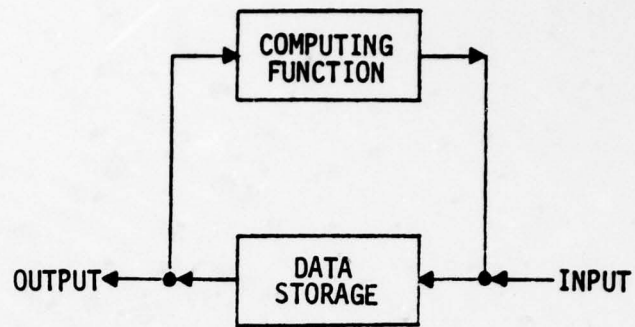
Data interconnections are used for processor classification and are a determinate of processor performance. For example, an internal serial data transfer between elements, given the same technology, would operate at a much lower data rate than an isolated parallel data transfer. Three representative data transfer networks are shown in Figure F-4.

The dedicated interconnections [Figure F-4(a)] are either directly connected or selected as one of N inputs (multiplexer/demultiplexer). The individual isolated data paths are fixed and uni-directional.

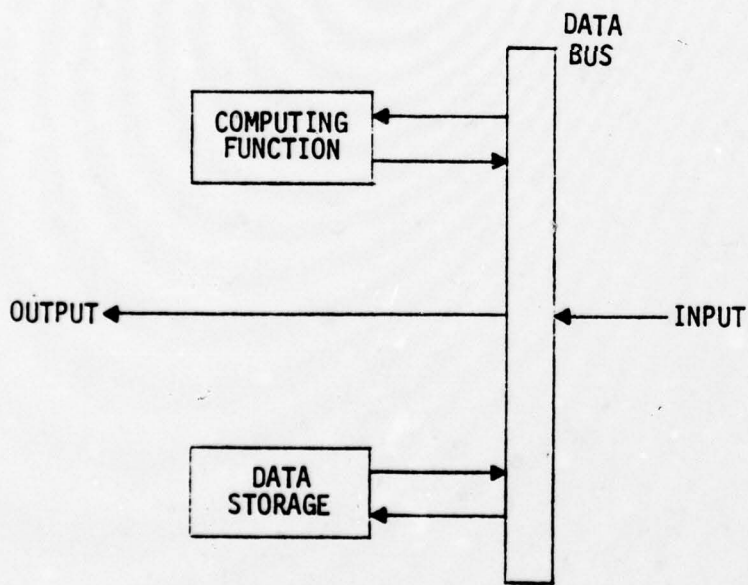


NOTE: MUX = MULTIPLEXER
DEMUX = DEMULTIPLEXER

(a) DEDICATED INTERCONNECTION



(b) PARTY LINE



(c) DATA BUS

FIGURE F-4. INTERNAL DATA TRANSFER NETWORKS

Addition of more computing functions, as in a parallel processor, requires more selectors but effectively isolates each function for simultaneous operations. Data can be transferred to function one while an addition and transfer to function two, and function two output to storage occurs concurrently. Function two to function one in the same sequence is also possible.

The party line illustrated in Figure F-4(b) basically connects all the inputs together and the outputs together using a dual party line. A party line as shown, has a single source or destination and all other destinations or sources respectively are "daisy-chained" together. The input party line requires isolators in the form of tri-state drivers which have a high-impedance output when not in use. Additional computing functions can be added by simply connecting to the party lines. The interconnections are reduced to just the party lines but data is transferred serially there by slowing the overall data processing.

The data bus is a simplification of the party line network, in that both the input and output are combined into a single bi-directional transmission media. Tri-state drivers are required as well as a bus controller and a priority-access system. The latter is necessary when simultaneous requests for bus access occur. The data bus allows a very modular approach with a minimum of interconnections but is the slowest of the three given configurations in total data processing.

All microprocessors use two types of memories - random access memories (RAM's) for data storage and read-only memories (ROM's) for permanent, non-volatile storage. RAM's are used for buffering internal/external data rates (refer to Figure F-5), main data storage, the main memory, for input/output and program results, high speed temporary storage for partial results and main memory access speed enhancement - the scratch pad or cache memory, and the stack memory - a last-in first-out memory.

The stack memory is used for storing addresses during subroutines, interrupts and index operations. Additionally, it is sometimes used with computing functions to reduce memory storage requirements. ROM's are considered for the program memory (microprograms) and permanent storage such as tables, coefficients and constants.

Memory parameters that are iterated with the architectures are: access times, bit capacity and words by bits per word organization, data flow and interconnection with other processor elements, and ancillary capability such as direct memory access (DMA) control.

The interface with other equipment outside the boundary of the microprocessor requires data storage, line drivers/receivers, and compatible control logic. Serial to parallel data conversion and the inverse may be required. Error detection and encoding (such as a parity) may also be used. The control signals consist of a source request with a response of a data transfer. Interrogate-response and "handshaking" asynchronous interfaces use this flexible technique. If the interface is dedicated to another subsystem, a demand access method can be used where the data source and destination originates at the subsystem. This provides a synchronous system with known data transfers. Transfer word formats can be data only or have a preceding control/address word then data. The latter requires decoding and steering logic. All of these data transfers activate the interrupt structure which in turn initiates subroutines for I/O operations and algorithm processing.

The microprocessor control section generally uses microprogramming as a substitute for hardwired control logic. The microprograms consist of instructions (or microinstructions) that provides all the control and selection signals to the computing function, data storage and input/output. Additionally, address information for branching and indirect addressing is generated. The microinstructions containing control/address are stored

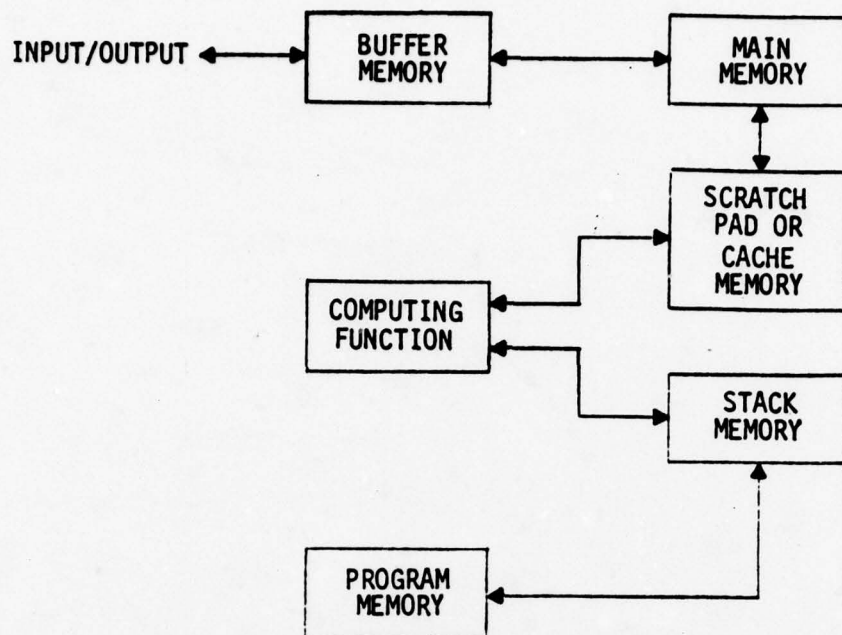


FIGURE F-5. MEMORY STRUCTURE

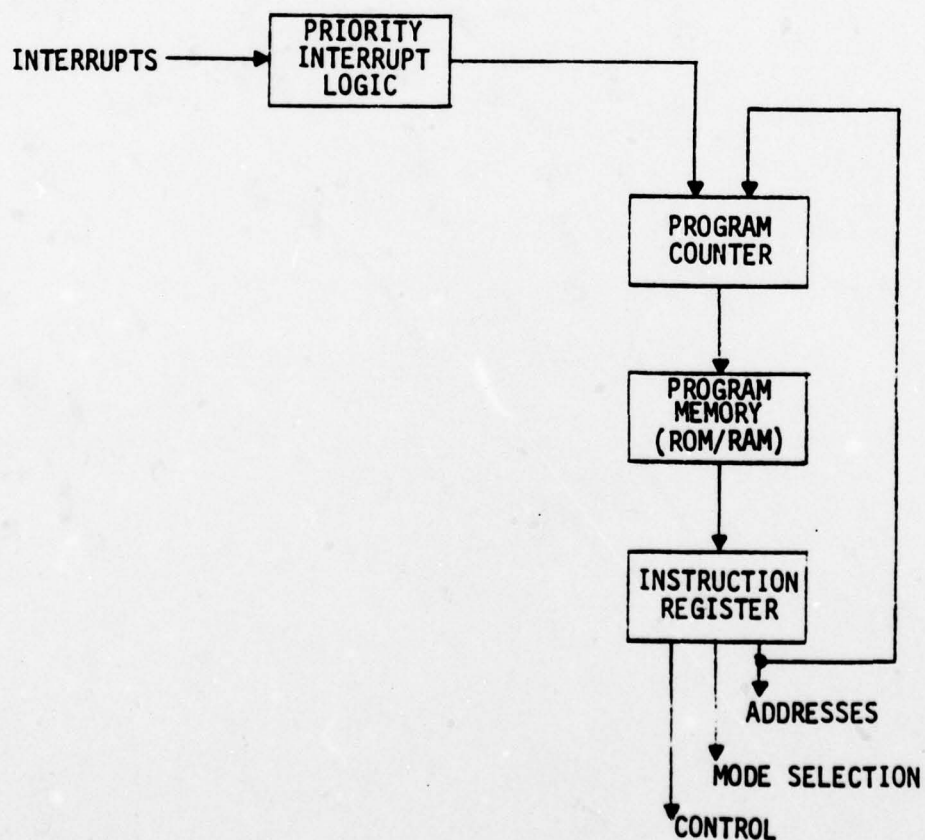


FIGURE F-6. MICROPROGRAMMED CONTROL

in program memories which can be either RAM's or ROM's depending on the permanence and maturity of the applications program. Refer to Figure F-6.

Each microinstruction has fields dedicated or sectorized for the operation of each element. Each field thereby contains the microcode (binary pattern) which can be decoded and distributed synchronous with the processor clock for data transfers and other operations. The program counter provides the program memory address with capability to accommodate conditional branching and interrupt addresses. Within a program, microinstructions are executed sequentially. While microprograms contain information to control hardware, they can be stored in a permanent memory coining the term "firmware".

Microprogramming techniques are used because of the efficiencies and economics of handling firmware as opposed to conventional random logic. The control section of a non-microprogrammed processor tends to be complex due to the logic networks required. Using microprograms, the control is simplified. Randomness remains, but only stored as random data in the program memory - not as an unstructured logic network. The flexibility of microprogramming is considered to be its major advantage. The user can modify his instruction set to tailor it to the particular application. Program changes can be made by memory substitutions in ROM's or program reloading in RAM's.

The program memory outputs are groups of synchronous, word parallel, data streams and directly dependent upon the architecture being investigated. When each of the outputs performs a single unique control function, this is labeled horizontal microprogramming or minimal encoding. This approach is used primarily for higher operating speeds by being more parallel in concept. The horizontal approach does require a wide control word (number of bits per word) and availability of each element directly.

Vertical microprogramming uses microinstructions that are all or partially encoded. Some control allocation flexibility is lost and instruction execution speed is slower due to the decoding process. Multiple instructions may be necessary, such as control and address separated into two instructions, thereby slowing execution

The microprogrammed control has two ways of initiating an external response - polling or interrupt. Polling uses a sampler that sequentially senses the state of each input line, and based on being enabled or not, either branches to a predetermined program or continues polling. The interrupt method generates a unique microprogram address for each line. The program is then executed immediately. Polling has the slower response time since each input must be scanned individually and each must wait its turn to be recognized. Interrupts offer the fastest microprocessor response time but requires additional logic for address generation and priority determination.

The instruction set definition begins with the review of the algorithms for the given applications. Requirements, such as addition, multiply, etc., will be developed after generating the preliminary assembly language programs from the algorithms. Commonality and frequency

of use in most (or all) applications will be in the selection criteria. The micro-signal-processor organization (the element configuration and interconnections) can now correlate the basic functions such as parallel processing with a fast I/O necessary to meet the operational processing requirements - operations per second - and the instruction set. The final iterative merger of the organization, instruction set and application algorithms generate the microinstructions in the microprogrammed control. The program memory word can now be defined as to format and word length.

APPENDIX G

G.1 MICRO-SIGNAL-PROCESSOR (MSP) IMPLEMENTATION

The MSP implementation is based on the existing JTIDS RSED microprocessor and the SAM MSP and has two major parts, the central processor and the microprogrammed control (Figure G-1). The basic microprocessor organization is referred to as a pipeline microprocessor (herein designated PM). The "pipeline" results from the interrelationship of the central processing unit and the hardware multiplier and the separation of the main memory into an input/output memory. These central processor elements can then be serially connected in a time division multiplex operation, each simultaneously processing a part of an algorithm.

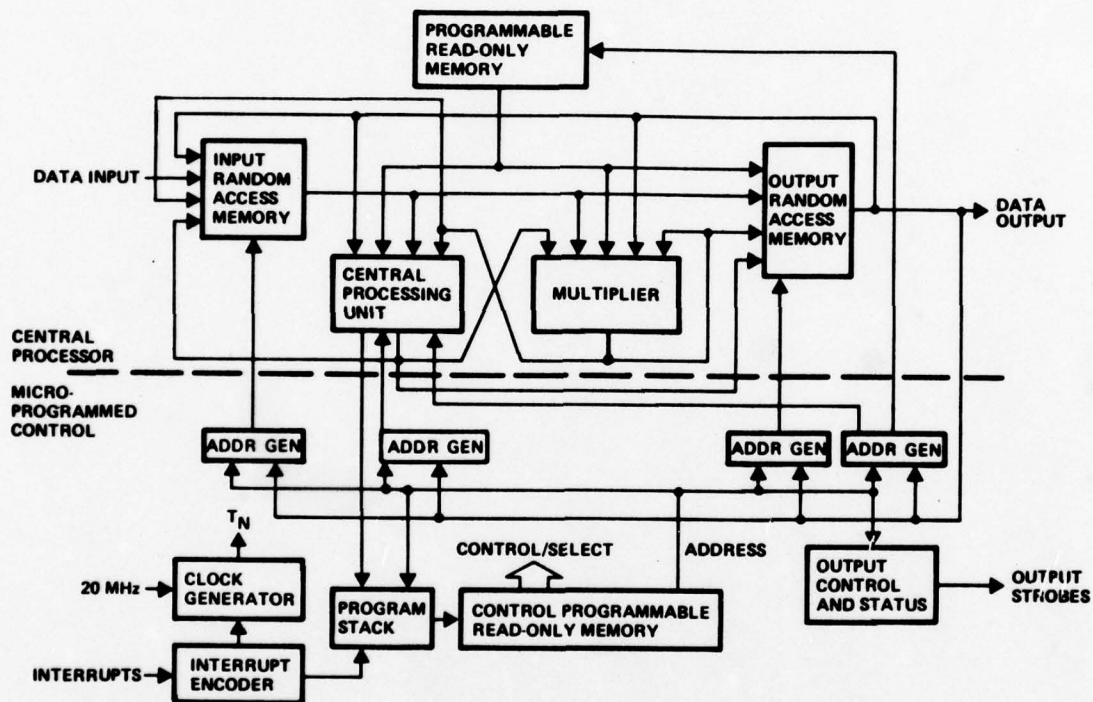


Figure G-1. MSP Functional Block Diagram

The central processor provides all the computational and data storage capability of the MSP. The central processing unit (CPU) consists of four AMD 2901A integrated circuits containing all of the arithmetic computations and logic operations. The hardware multiplier is capable of 200 nanosecond binary 16 x 16 multiplications and is inter-connected with the CPU through a dual cross-coupled data path. The latter allows data interchanges for

add-multiply operations in a pipeline mode. The other functions of the central processor include the input and output random-access memories (RAM's) for temporary data storage and general working registers, and the programmable read-only memory (PROM) or ROM for nonvolatile storage such as filter coefficients and sine/cosine tables. The external data input/output with the RAM's is through the use of a direct memory access (DMA) at 5×10^6 words per second.

The basic pipeline architecture uses separate data paths for non-conflicting simultaneous point-to-point data transfers, parallel control using minimal instruction decoding (horizontal microprogramming) for independent resource manipulations, and parallel memory addressing capability for multiple memory data accesses within each machine cycle.

The most flexible processor control technique is the microprogrammed control using "firmware." All data transfers and operations are under the control of the control ROM (or PROM) stored programs - the microprograms. The microprogram consists of a set of words or instructions each labeled as a microinstruction. A microinstruction provides the lowest tier of control information for each of the elements. The control ROM (C-ROM) and a decode/distribution network provide the facility to systematically execute the sequences of microinstructions.

While microprograms contain information to control hardware, they are stored in a permanent memory and executed as stored programs. This produces a hardware/software overlap, coining the term "firmware" for the control ROM microprogram. Generally the microprogramming provides a systematic alternative to hardwired control, flexibility (program changes by simple ROM substitutions), and a potential reduction in component count.

The memory addresses or pointers are derived from the C-ROM instruction format and distributed via an address bus to dedicated memory address generators. The program stack includes the program counter that controls the C-ROM and receives an interrupt address from the interrupt encoder for program initialization and flags for conditional branching. The program stack contains a small stack memory with first-in-last-out operation that stores addresses during interrupt conditions and provides the associated sub-routine save/restore.

The MSP architecture uses an efficient but constrained instruction set. There are two basic types of instructions needed for the signal processing algorithms: central processor, control and address. The machine cycle is 320 nsec in duration and eight subintervals of 40 nsec each. The technology used is the low-power Schottky TTL logic family and standard off-the-shelf bipolar LSI such as RAM's, ROM's, and CPU's. The parts count is 170 integrated circuits with a power dissipation of about 35 watts.

A summary of the MSP characteristics is shown in Table G-1.

TABLE G-1. MICRO-SIGNAL-PROCESSOR (MSP) SUMMARY

- Microprocessor Organization for Signal Processing Applications
 - Data Demodulation
 - Bit Synchronization
 - Acquisition and Tracking
 - Other Functions: Mode Control and Built-In Test
- Fast Parallel Microprocessor Organization - Parallel Data, Address and Microprogram Control
- Based on an Existing Qualified TRW High Performance Microprocessor Used for the JTIDS Reed-Solomon Encoder/Decoder and Standard Avionics Modules (SAM) for Existing Modems
- MSP Characteristics
 - 8 to 16-Bits/Data Word
 - 320 Nanosec Microcycle
 - Hardware Multiplier (16 x 16)
 - Vector Interrupt (2×10^{-6} Sec Response Time)
 - DMA 5.0×10^6 Words/Sec
 - TTL Compatible Interfaces
 - Parts Count - 170 IC's

TABLE G-1. MICRO-SIGNAL-PROCESSOR (MSP) SUMMARY (Continued)

- Power Dissipation - 37 Watts With 512 RAM/512 CROM Word Capacity
- Size - 5 x 7 x 4 Inches With Dip IC's and One-Half ATR Cards
- Instruction Execution Rate₆ for Realtime Throughput - Up to 20×10^6 Instructions Per Second
- Software Support: Modified Existing RSED Assembler/Emulator
- Capable of Multiprocessor Operation and can be Configured as a Two-CPU and a Single-CPU MSP
- Internal Organization Allows Simple Bite Implementation
- Modular by Functions: CPU, Multiplier Sequencer, Data Storage, Control Memory, Program
- Modular Elements are Technology Interchangeable - Optimize Speed-Power Product for a Given Application

G.1.1 Central Processor

Introduction

The central processor of the micro-signal-processor (MSP) includes all the arithmetic and logic functions, data storage, hardware multiplication, permanent coefficient storage, and input/output buffers and control (Figure G-2). This is the core of the pipeline processor organization. Multiple separate and parallel data paths permit non-overlapping simultaneous data transfers. The two separate memories (input and output) provide two functions: the working registers or work space for the central processing unit (CPU) and multiplier, and is the data buffer for the I/O direct memory accesses (DMA's). The cross data interconnection of the CPU/multiplier facilitates pipeline processing by this direct path. Computations and data transfers can now occur simultaneously with a single instruction by direct routing of processed data to the input of the next stage which is operating on previous data. The parallel data paths, combined with parallel control signals and parallel memory addressing, provide the MSP with the capability of instruction execution rates up to 25×10^6 instructions per second.

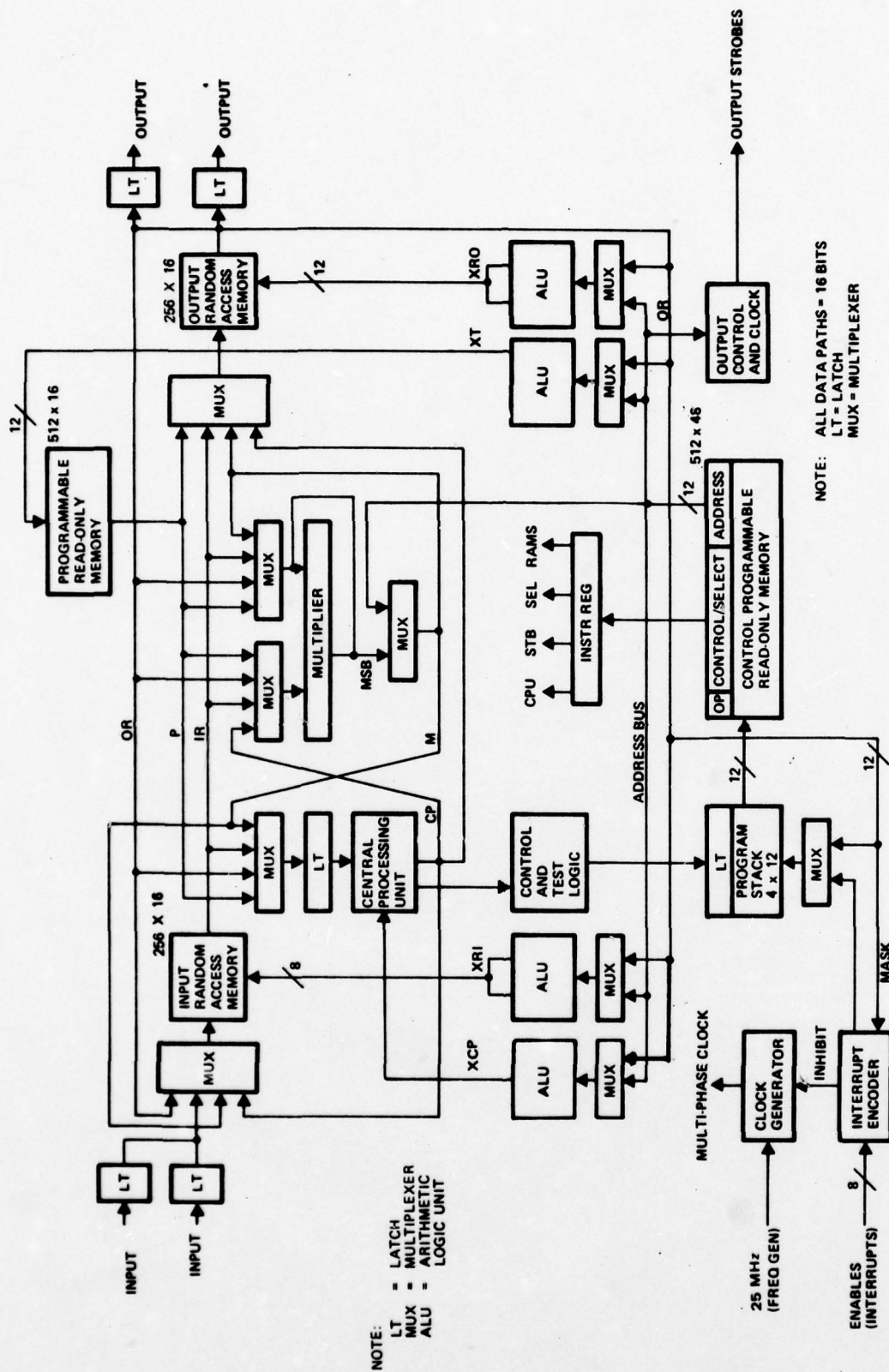


Figure G-2. Micro-Signal Processor Detailed Block Diagram

An example of the MSP processing capability is illustrated in Figure G-3. The example simple recursive algorithm is as follows:

$$S_t = ((S_{t-1}) * (a)) + R$$

This is depicted as a functional flow with the output S_t being sampled at the end of the sequence N. A pipeline is set up in firmware producing the given data flow. The a from the read-only memory (ROM) is multiplied with the previous output S_{t-1} at $t-2$ time. The $S_{t-1} * a$ is added to R at $t-1$ time and the results are stored in the CPU RAM at t time. All of this is accomplished in a single instruction. The pipeline setup and clearing, however, does require a few instructions each. Note that most of the processing time is in the iterative loop if $N > 16$.

Architecture Selection

In a general sense, the architecture of processors can be classified into such major types as serial, parallel, pipeline, or array. The basis of the categories is the data flow (singular or multiple) and program or instruction control (again, whether singular or multiple) (Figure G-4). It is recognized that there may be other types and certainly other methods of classifications, but the four above are appropriate for algorithm-oriented processors.

The serial processor is depicted in Figure G-4a. All the essential processor functions, except the I/O interface, are shown. The control, such as data sequencing and timing, can be generated by discrete logic or by a ROM. The ALU provides the computational and data manipulation capability, and the data memory is just storage which could be multiple memories or a hierarchy of memories. The data flow between the ALU and memory is a single data stream; and the control signals or instructions are executed sequentially. The ALU-memory interconnections can be hardwired to accommodate a class of algorithms, as in a special purpose processor. A flexible internal communication network can be implemented using the data bus concept which can be in a form of a party line or a full duplex bus with many users. The single chip CPU's generally operate in this serial configuration.

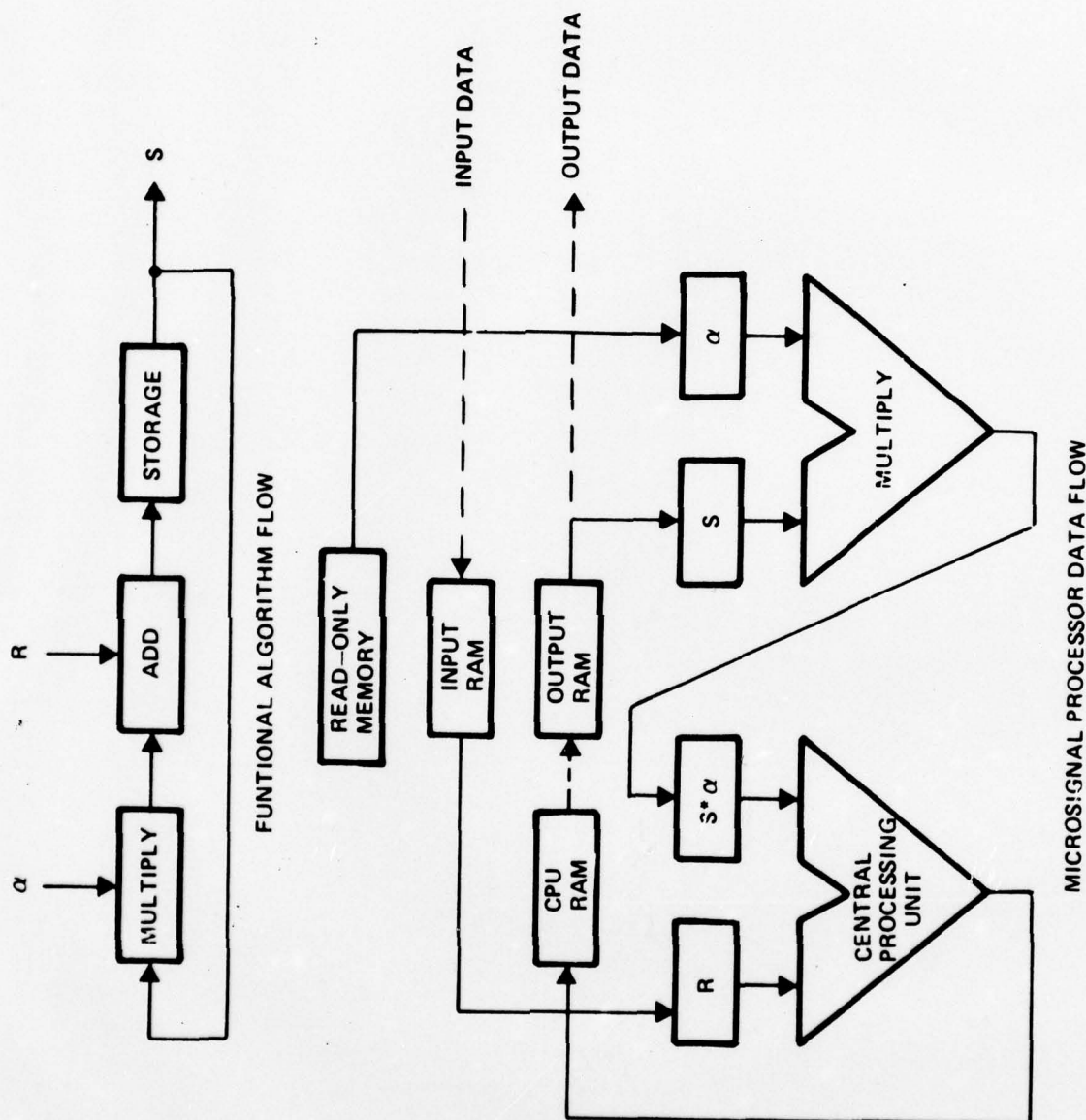


Figure G-3. Microsignal Processor Pipeline Data Flow Example

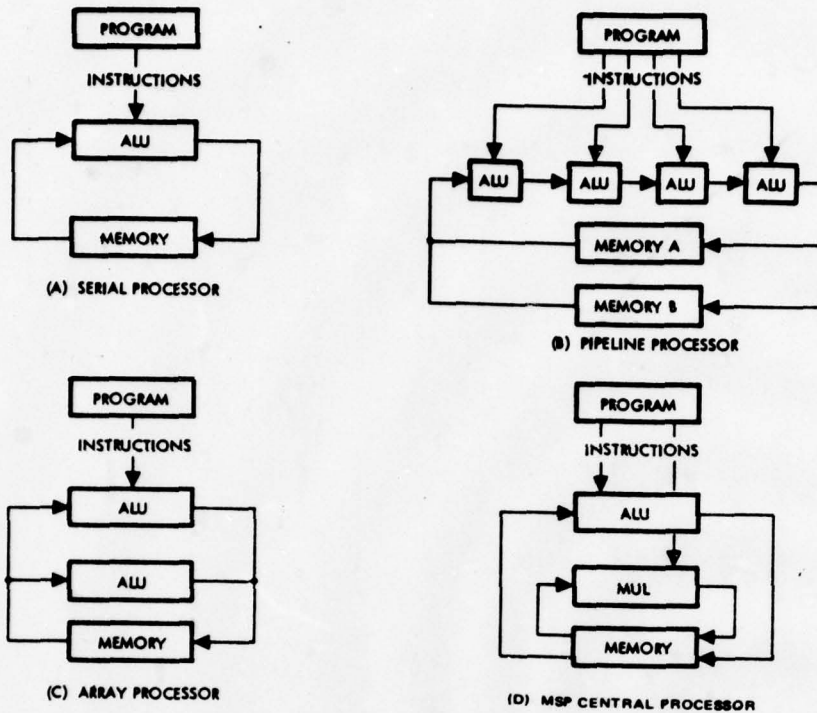


Figure G-4. Microprocessor Architecture

The pipeline processor (Figure G-4b) uses a single serial data stream but requires multiple signals for processing. The ALU is divided into identical serially-connected modules, each time-division multiplexed, doing a part or the same task. The output of a module is passed to the next module in line with all modules operating concurrently. Algorithms that require continuous, fast, multistep processing with few feedback iterations could be applied to this type of processor. The memory can be organized the same as the serial processor.

The array processor (Figure G-4c) processes data in parallel. This requires a single signal, but multiple data streams. The processor is now divided into modules of equal capability but arranged in parallel. This centralizes the data memory for the "array" of processors so that the same instruction can be executed by all processor modules simultaneously.

The MSP central processor (Figure G-4d) is an evolution of the array processor where there are multiple data paths but also there are multiple

instructions. The multiple instructions allow different operations to occur concurrently. In addition, the cross-connection allows a configuration that can be programmed to be similar to the pipeline processor. Thus there is inherent flexibility to accommodate both architecture types within this selected central processor organization.

Detailed Central Processor Operation

The central processor is organized around two computational modules and dual random-access memories (RAM's) interconnected by parallel data paths. RAM's and module assignments are under microprogram control and multiple tasks can be conducted without interference. For example, each computational module (CPU or multiplier [MPY]) can be dedicated to a memory which would then be the working space. External input/output data transfers and memory-to-memory swaps can also be accomplished. In array programs, this occurs simultaneously with the computations. This provides an effective increase in data processing rates. Note that arithmetic operations use memory direct transfers without intermediate storage such as registers, providing data processing rate enhancement.

The CPU provides all arithmetic and logic functions (such as exclusive-or) within the processor. The basic CPU is the AMD 2901A integrated circuit containing computational capability, data storage and instruction decoding. The CPU is expandable in 4-bit word increments, as required, from the given 16-bits per word. The CPU output can transfer data to the input and output RAM and the multiplier (MPY).

The input and output RAM's are identical and have a capacity of 256 words by 16 bits per word each. These RAM's use the Schottky technology that is compatible with the MSP instruction execution cycle. Expansion capability is by these block capacities (256 x 16) up to 4096 words by 16 bits/word per each memory. The memory address can be either direct from the address field in each microinstruction or indirect as a computed address (adding a constant to a fixed address) in either the Central Processor itself or the address generators, the latter of which will be described in the next section. Data to be stored is transferred as a 5 M word per second DMA. The output RAM transfer is also 5 M wps DMA. All control signals are from the Microprogrammed Control microinstruction fields. Each memory operates independently and has separate data paths for external input/output, CPU, MPY and the table lookup PROM.

The multiplier (MPY) is a 16-bit by 16-bit binary multiplier with a selection on the 32-bit product - all of the most significant bits or least significant bits. The MPY data can be transferred to the input/output memories, wrapped back on itself, or interchanged with the CPU. It receives a direct input from the PROM table lookup that is essential for signal processing, digital filtering and frequency translations.

The programmable ROM shown is a 512 word by 16 bits/word nonvolatile memory. All algorithm coefficients and constants are permanently stored in the PROM. The PROM can interface with the output RAM or directly with the CPU and MPY. This provides a fast direct access for program execution. When power dissipation is of concern and the memory access repetition is low, power strobing can be implemented to reduce power consumption as these are nonvolatile memories.

G.1.2 Microprogrammed Control

The microprogrammed control (MPC) provides all the direct address control, and clock signals to the central processor. This includes any multiplexer selects and I/O load strobes. The control and addresses are stored in the control PROM (C-PROM). Each microprogram consists of microinstructions which have fields dedicated or sectorized for each central processor function in addition to the direct address fields. Each field thereby contains the microcode which would be decoded and distributed for data transfers and other operations.

Microprogramming techniques are used because of the efficiencies and economics of handling microinstructions in firmware as opposed to the conventional random logic approach. The control section of a nonmicroprogrammed processor tends to be complex, containing numerous gates, multiplexers, storage elements, and decoding networks for each instruction that is executed. Using microinstructions stored in a semiconductor ROM, the control can be greatly simplified. Randomness remains, but only stored as random data in the memory - not as an unstructured design of logic networks. In essence, a more structured organization of hardware logic results.

The control memory outputs, which are groups of synchronous word-parallel data streams, whose patterns are a function of the memory contents, are used to set flip-flops, select multiplexer inputs, load/increment, or select ALU functions or any other control function associated

with hardware operation. When the control memory outputs perform a single unique control function, this is labeled horizontal microprogramming or minimal encoding. This approach is used in the microprocessor primarily for higher operational speed and multi-instruction executions. The horizontal approach requires a wide (bits per word) control word and control availability of all functions with each word.

Vertical programming uses microinstructions that are partially or fully encoded, such as in the use of memory addresses in RAM's. The penalty is that some flexibility is lost and speed of operation is reduced proportional to the number of C-PROM reads per instruction and decoding time. The latter results from multiple steps being required for a single operation. Encoding microinstructions does tend to reduce the control memory storage capability requirements. Typically, the encoding is done within a single 8-bit byte or 16-bit word.

The data flow for the microinstructions starts with either a direct address selected by the P-multiplexer presetting the P-CTR (program counter) or P-CTR being incremented by one. The P-CTR is within the program stack. The instruction fields, or the bit allocations within the instruction are transferred to the central processor or used as part of the microprogrammed control functions. Control signals and direct memory address are shifted word parallel to the instruction register (storage for the control signal decoding) and the memory address generators (ALU and MUX), respectively. The jump instruction (JMP), both conditional and unconditional, requires use of the address or pointer in the control PROM format. For program loops, the program iteration count, or the count for jump, is maintained in the program stack. Indicators from the CPU generate the conditions upon selection for the C-PROM pointers for branching on a given test condition. The program stack (a first-in last-out register file) is used to store C-PROM address data for interrupt conditions based on data enables and subroutine loops. In addition, addresses of the dual I/O memories, and the PROM can be saved and restored within the address generators. The address bus permits communications with all counters on a single data bus. Address data from the microinstruction field may be loaded into the counters during the machine cycle. A firmware counter in the XRI and XRO address generator is used with the I/O data transfer or DMA's for maintaining word count during the transfer time duration.

All of the above resources are under the control of the P-CTR or program counter. All control signals and required timing signals are referenced to the P-CTR and the clock generator. All timing and operations are fully synchronous with the clock generator. The clock generator oscillator operates at 25×10^6 Hz to provide eight time periods within the 320 nsec basic cycle.

The inputs to the C-PROM program stack are from the address bus for interrupt restore, indirect addresses from the central processor and priority interrupt logic consisting of the interrupt encoder logic. Typically, a logic system performs an operation either in response to a change in state of its inputs or as a function of time, such as an internal timer. For the microprogrammed control, there are two ways of initiating a response - polling or interrupt. Polling uses a sampler that sequentially senses the state of each input line and, based on input logic states, either jumps to the appropriate PROM program directly or continues polling. The interrupt method generates a unique PROM address for each input line. This address may be either the beginning of a microprogram or the address of a jump microinstruction which in turn contains the starting address. The latter is a form of indirect addressing. In either case, the interrupting program is executed immediately.

Polling provides the slower microprocessor response since each input must be scanned individually and each must wait its turn to be recognized. This is somewhat less complex than the interrupts and sequentially handles simultaneous inputs. Interrupts, especially priority interrupts, require additional logic for address generation and the priority strategy. The technique does offer the fastest microprocessor response time, which is almost negligible if the highest priority is requested. The interrupts, as used in the MPC, are the data enables which are transformed to the interrupt address.

There are four address generators, one for each of the memories: input RAM, output RAM, PROM table look-up and the register file in the CPU. These are designated XRI, XRO, XT and XCP. Each address generator consists of an ALU and an input multiplexer. The ALU is the Fairchild 9405 providing data storage and arithmetic capability. The multiplexer selects either the direct address field within the microinstruction (address bus)

or the output RAM data output (OR). Memory addresses could have been generated by using registers and direct loading from C-PROM, binary up-down counters or using a computational element for maximum flexibility. The ALU address generator is the latter which also includes data storage for program "nesting" and the interrupt save/restore. A single address counter can also be used but this is a severe limitation on processing capability. Time sharing an address counter creates control phasing problems relative to memory-to-memory transfers, computations and the basic machine cycle. Parallel addressing permits full processing capability with a penalty of additional hardware.

G.1.3 Microprocessor Instruction Set

The microprocessor has two basic instruction types, central processor and multiply. These are further subdivided (Table G-2) into six transfers, which meet in a general sense all algorithm requirements. The arithmetic instructions which include CPU/MPY operations allow users to manipulate data and perform computations. Tests of the results of the operations are implemented using a microcode field. The transfer (includes control) instructions shift data, word parallel, from a source to a destination through multiplexers and data buses. These are a type of register transfer instruction. Branch (or jump) instructions which are address-to-program stack transfers that determine the execution sequence of instructions and subroutines within the microprocessor by testing results of arithmetic manipulation instructions. A microinstruction transfer is used to save addresses as part of an interrupt response and initiate a return when the interrupt has been serviced.

Each instruction listed in Table G-1 requires two cycles for complete execution. the fetch cycle reads the microinstruction from the control PROM to the CPU resources. The second cycle, the execute cycle, decodes and distributes the control and select signals necessary to complete the operation. Each cycle requires 320 nsec for a total of 640 nsec. Each fetch and execute cycle overlaps, except the first fetch for "look-ahead" instruction processing, yielding an effective execution rate of 320 nsec per instruction.

Table G-2. Basic Instruction Set

a) Generalized Transfer Instruction

MEMORY	→	MEMORY
MEMORY	→	REGISTER
FUNCTION	→	MEMORY
FUNCTION	→	REGISTER
ADDRESS	→	COUNTER
FUNCTION	→	COUNTER

b) Examples of Each Type of Instruction

<u>MEMORY</u>		<u>MEMORY</u>
RAM	→	RAM
PROM	→	RAM
<u>MEMORY</u>		<u>REGISTER</u>
RAM	→	A1
RAM	→	M1
<u>FUNCTION</u>		<u>MEMORY</u>
CPU	→	RAM
MPY	→	RAM
<u>FUNCTION</u>		<u>REGISTER</u>
CPU	→	MPY
MPY	→	A2
<u>ADDRESS</u>		<u>COUNTER</u>
C-PROM (ADDR A)	→	XRI
P-STACK	→	P CTR
<u>FUNCTION</u>		<u>COUNTER</u>
CPU	→	XRO

A detailed instruction summary is illustrated in Figure G-5 where the partitioning is by function - the address, central processor unit and control. Each microinstruction is capable of all of these listed operations - address manipulations, computations both arithmetic and logical, and interrupt and branch control. The central processor unit instructions include the CPU and MPY and are tabulated in Figure G-6. The address generator instructions, Figure G-7, include all of the 9405A capabilities. Note the < indicates a transfer from right to left, or the contents on the left is replaced by that on the right. The control instructions, Figure G-8, list all possible interrupt and branch conditions for the interrupt encoder and the program stack.

A microprocessor example is now presented to illustrate the advantage of full parallel and pipeline capability of the MSP. A code tracking loop is shown in Figure G-9. Using standard assembly language for a conventional serial processor, 27 instructions are required. The code tracking loop is part of the set of GPS demodulation programs. The same program can be microcoded in the MSP in 10 instructions as shown in Figure G-10. The symbols used are the type of assembly language used by the MSP assembler. The prefix X indicates an address counter, M = MPY, R = RAM's, CP = CPU and etc.

G.1.4 Control PROM Microinstruction Formats

The control PROM microinstruction formats (Figure G-11) require a 96-bit PROM word. The word capability is 256 and can easily be expanded in 256 word by 96 bits/word blocks. The word fields have a direct relationship to the central processor resources and are structured as program modules into two types of instructions. The central processor microinstruction (CP) contains CPU control and the memory and data transfer control together with a direct address field for memory accesses. The entire C-PROM word is read out simultaneously allowing parallel operation and control in a single readout. The operations code identifies the type of operation to be executed - whether central processor or multiply microinstruction.

<u>ADDRESS</u>	<u>CENTRAL PROCESSOR UNIT</u>	<u>CONTROL</u>
INCREMENT/DECREMENT	ADD	INTERRUPT
DIRECT	SUBTRACT	CP BRANCHES
INDIRECT	MULTIPLY	INDEX BRANCHES
ADD	LOGIC	INDIRECT BRANCHES
LOGIC	SHIFT	NESTED SUBROUTINES

Figure G-5. Instruction Summary

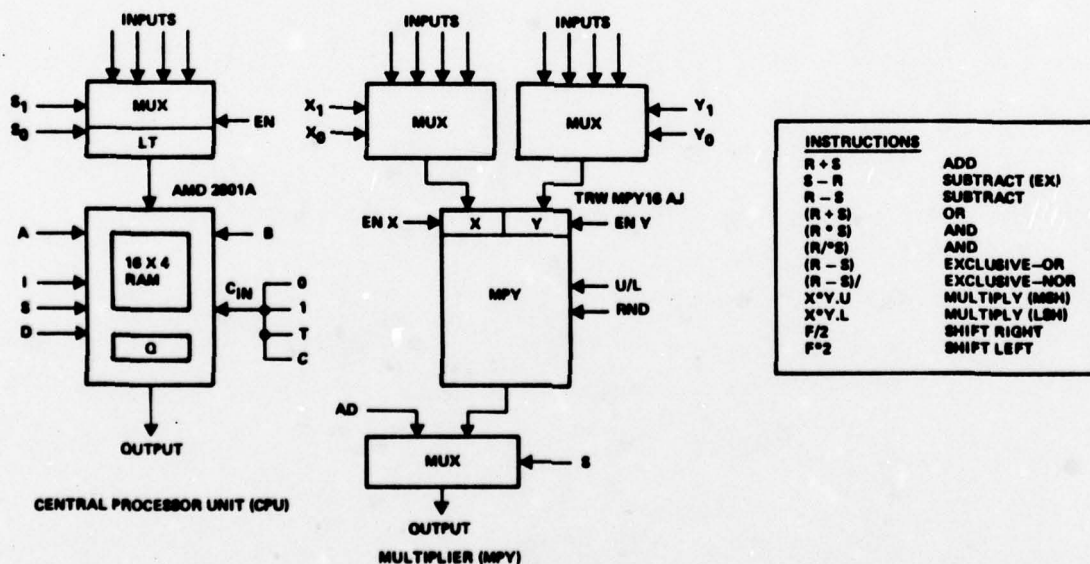


Figure G-6. Central Processor Unit Instructions

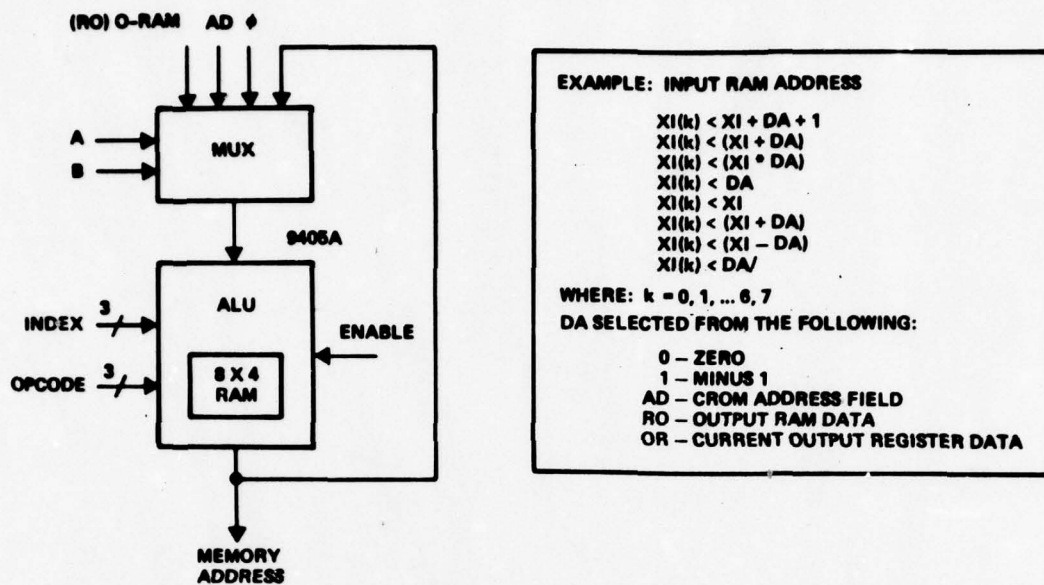
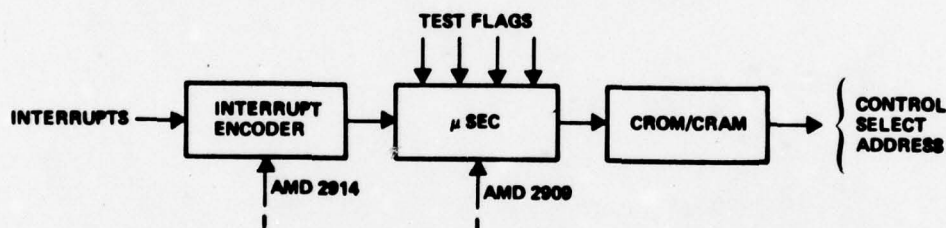


Figure G-7. Address Generator Instructions



INTERRUPT ENCODER

MASTER CLEAR
 CLEAR ALL
 CLEAR FROM MASK
 CLEAR FROM BUS
 CLEAR LAST VECTOR
 READ VECTOR
 READ STATUS
 READ MASK
 SET MASK
 LOAD STATUS
 BIT CLEAR MASK
 BIT SET MASK
 CLEAR MASK REGISTER
 DISABLE INTERRUPT
 LOAD MASK
 ENABLE INTERRUPT

NEXT ADDRESS

JUMP TO ZERO
 CONDITIONAL CALL
 JUMP TO INDIRECT
 CONDITIONAL JUMP
 PUSH STACK; LOAD COUNTER
 REPEAT LOOP; CNT \neq 0
 REPEAT ADDRESS; CNT \neq 0
 CONDITIONAL RETURN
 CONDITIONAL JUMP; POP
 LOAD COUNTER
 TEST END LOOP
 CONTINUE
 UNCONDITIONAL JUMP

BRANCH CONDITIONS

.EQ., .LT., .GT.
 .NE., .GE., .LE.
 OVERFLOW
 ZERO, NON-ZERO
 CP POSITIVE, NEG
 MP POSITIVE, NEG
 XI ZERO, NON-ZERO
 XO ZERO, NON-ZERO
 XT ZERO, NON-ZERO
 STATUS OVERFLOW

Figure G-8. Control Instructions

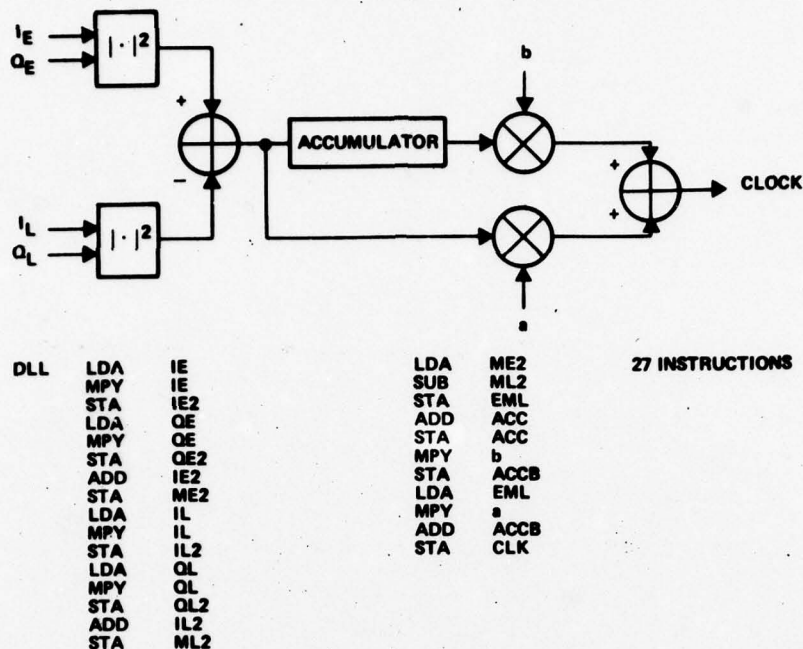


Figure G-9. Sequential Assembly Language Example (Code Tracking Loop)

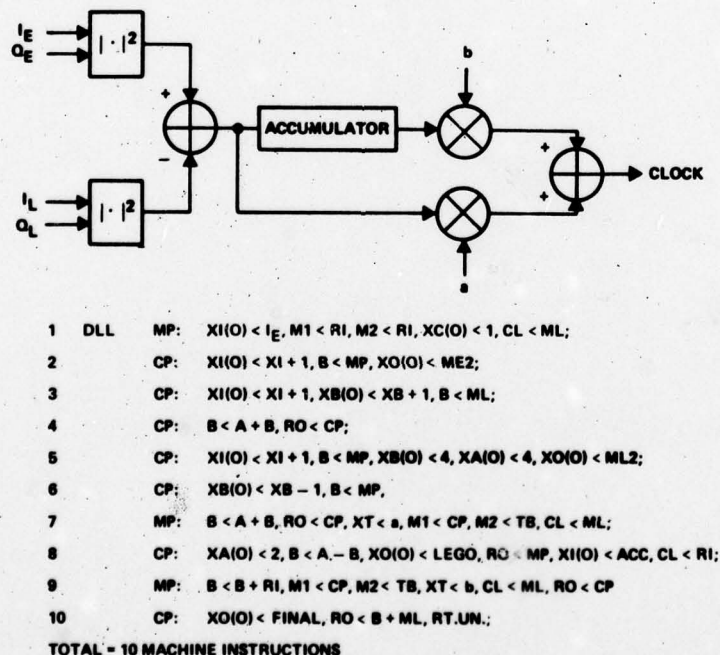


Figure G-10. Microcode Example (Code Tracking Loop)

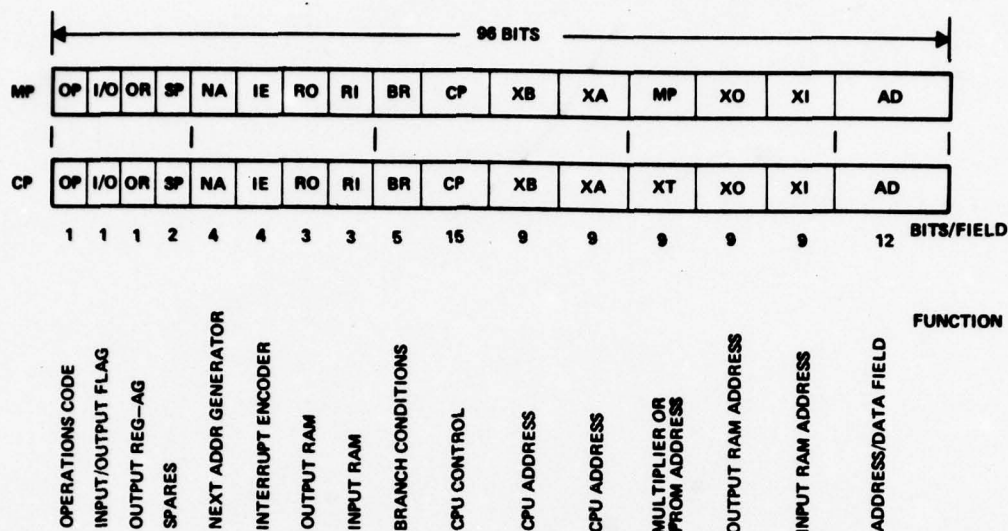


Figure G-11. Control Word Microinstruction Format

The multiply microinstructions (MP) have memory and data transfer control fields with the PROM address replaced by the multiplier control. The address field can change pointers in the address generators. The branch (or jump) instructions contain the destination address and, if conditional, the address to go-to. The branch requires an arithmetic microinstruction executed during a fetch cycle. No execute cycle is required for the branch.

The philosophy used for the control PROM was to create a fast, simple fetch and execute cycle operation and distribution. This required horizontal or nonencoded fields (other than addresses) and a hardware microprogram jump capability. Central processor resources can now be controlled in an array or pipeline manner where the RAM's, CPU, PROM, and MPY can be doing operations in parallel on a noninterfering basis. The memory address generators and the program stack can also be controlled simultaneously. This effectively increases the instruction execution rate by a factor of 8 to 25×10^6 instructions per second ($8 \times 3.125 \times 10^6$ ips).

G.1.5 Microprocessor Control Cycles

Flexibility in instruction cycle time or operating speed is incorporated in the MSP pipeline processor. It is designed for oscillator clocks over a range of frequencies near dc (if desired) to 25×10^6 Hz. This permits technology substitutions, aids microprocessor test and evaluation, and enhances the capability for multiple applications. The MSP will operate synchronously up to the limit of the technology implemented. All operations, computations, and data transfers occur synchronously at the clock rate.

The complete instruction cycle consists of a fetch cycle and an execute cycle (refer to Figure G-12). The fetch cycle reads the microinstruction from the control PROM. The execute cycle does the operation

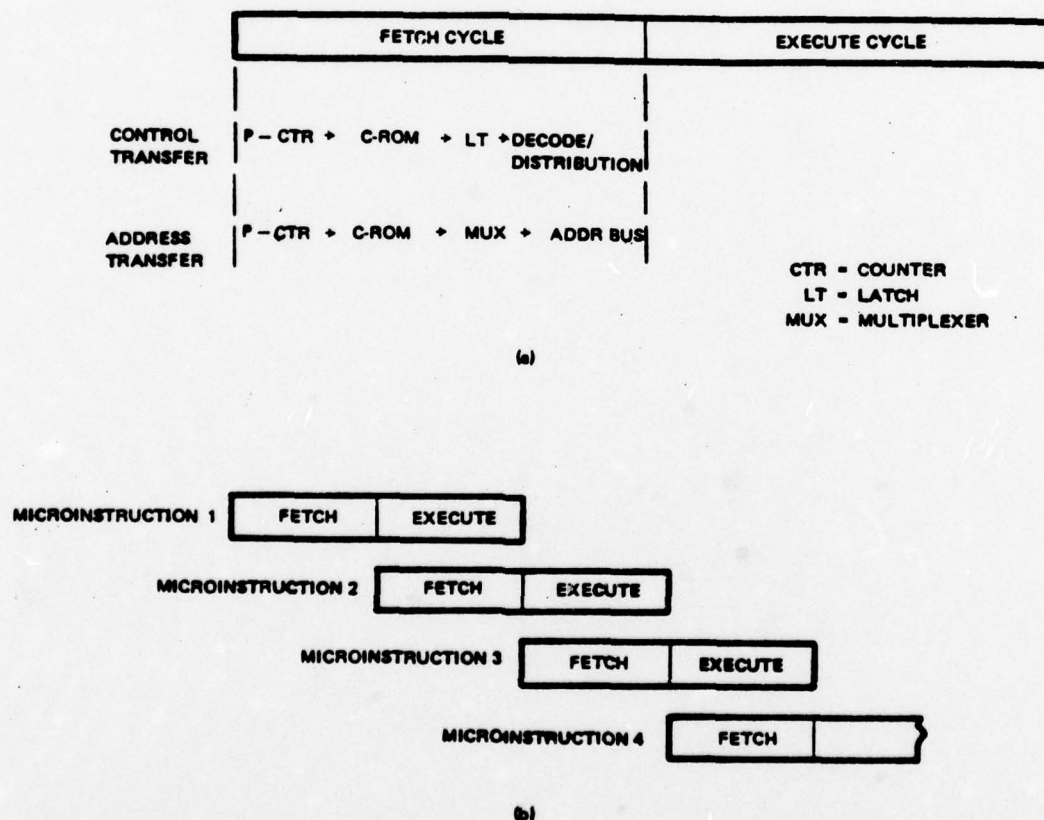


Figure G-12. Fetch Cycle and Multiple Executions

requested. Each cycle is a minimum of 320 nsec. The fetch cycle description shows time as a horizontal axis and the corresponding operations in time, such as counter increment. The C-PROM read access for both transfers is allocated 100 nsec. The CTR is incremented for the next microinstruction at the middle of the fetch cycle. The address transfer presets a counter while the control transfer stores and decodes control signals and both can occur together. When the adjoining execute cycle begins, the control signals from the decode/distribution are stable. The fetch cycle can now be overlapped with the execute cycle to produce an effective execution rate of 320 nsec (3.125 MIPS).

The basic microprocessor timing is illustrated in Figure G-13. The basic cycle consists of eight phases labeled T1 to T8. Each phase is 40 nsec in duration. Each microinstruction requires a fetch and an execute cycle. The fetch reads the microinstruction from the C-PROM at the selected address. The "instruction register" or latch is clocked at the following T1 time. Address generator increments also occur at this time. The address bus can transfer a single address during each cycle. All computations are done during T1 through T4 of the execute cycle, while memory reading is done at T5 and T6 and memory loading at T7 and T8. The latter provides the data transfers from memory to memory. The "look-ahead" technique is used on the fetch cycle as the next sequential fetch cycle occurs concurrently with the on-going execute cycle.

G.1.6 MSP Firmware/Software

The MSP software package consists of three basic elements: a microprocessor cross assembler, a microprocessor emulator, and the microprocessor firmware. This section contains a brief narrative on the design philosophy common to all four elements, followed by a presentation of the basic characteristics and features for each element.

The basic software design philosophy employs a system of cross-verification between elements in the package; i.e., output from one element is used as input to the next element. The motivation for this technique is to ensure logical design consistency in the four elements of the package. Figure G-14 illustrates the interaction between elements. The result of these interactions is to impose a closed verification chain on the entire software package.

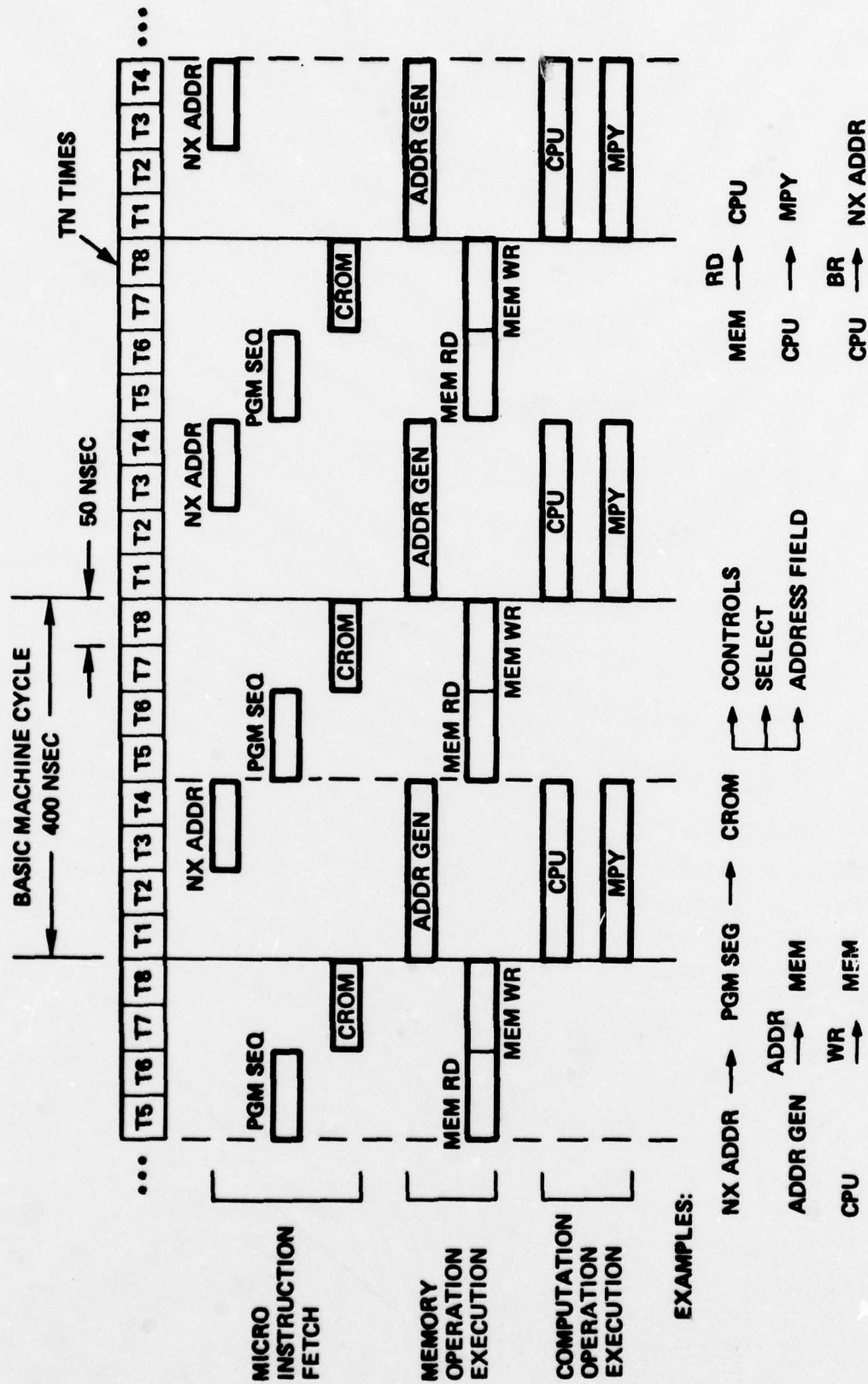


Figure G-13. MSP Basic Timing

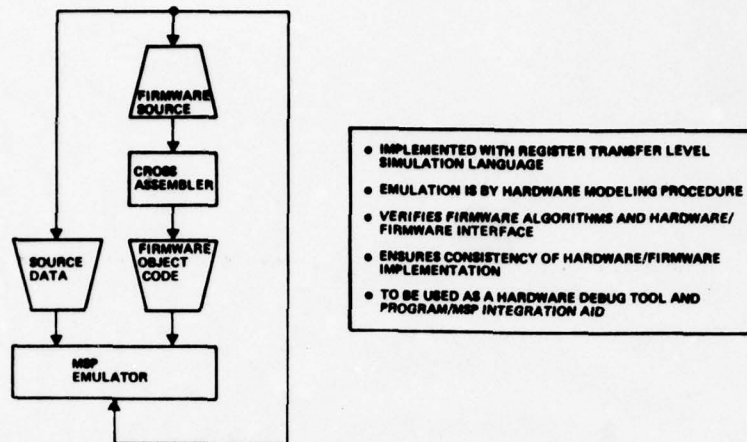


Figure G-14. MSP Emulator Program

Cross Assembler

The microprocessor cross assembler defines a programming language for the MSP. This language is register transfer oriented and reflects the parallel nature of the microprocessor by allowing the specification of multiple operations in a single "composite" instruction. Each composite instruction is translated from the mnemonic of the programming language to the 96-bit binary control word of the microprocessor. The assembler has several additional capabilities which facilitate programming and documentation functions and do not affect generation of control words. Included in these capabilities are symbolic constant and address definitions, list options for assembled control words, intermixed instruction mnemonics and documentation text in source input, and options for object paper tape file generation. The cross assembler design characteristics are as follows:

- Multiline assembly instructions, free format
- Table driven control word generation
- Assembly rate, 15,000 instructions/minute

- Symbolic address expression translator
- Control word error analysis
- Documentation facilities which allow intermixed mnemonics and documentation text
- Facilities for object paper tape file generation
- List options for assembled binary control words
- Pseudo-operations which allow the specification of arbitrary symbolic constants, listing titles, control address origin, etc.

The basic assembly algorithm is on a 2-pass basis. The first pass defines symbolic address values and performs limited error analysis. The second pass performs mnemonic recognition, control word generation, and detailed error analysis. Error analysis is implemented by assuming an initially undefined control word and each mnemonic in a composite instruction defines a fixed control field. Control fields are defined whenever a mnemonic is recognized and an error occurs if any single control field is defined more than once. The assembler is summarized in Figure G-15.

- TWO-PASS ALGORITHM
- TABLE-DRIVEN
- IMPLEMENTS COMPOSITE INSTRUCTIONS FOR PARALLEL CONTROL WORD (MICROINSTRUCTION)
- IMPLEMENTS PARALLEL CONFLICT AND ERROR ANALYSIS
- GENERATES CONTROL WORD OUTPUT ON PAPER TAPE
- GENERATES BINARY CONTROL WORD LISTING AND SOURCE LISTING
- HOST COMPUTER - 6000 SERIES CDC COMPUTER SYSTEM

Figure G-15. Assembler Summary

The list output of the assembler may be generated with or without assembled binary control words. Figure G-16 illustrates the output format with assembled binary. The last two lines are deleted in the output without binary; otherwise the two formats are identical.

The number at the far left of the example is an octal control address; i.e., the assembled instruction resides at this octal address in microprocessor control memory. RGN13 is the branch tag and AR: is the opcode specification. The remaining text on the first two lines is the operation subfield specification. The third line is the assembled binary control word broken into functional control fields. The control bit sequence is for this group of 63 to 0 from left to right. The last line is assembler-generated mnemonic text which describes the respective control fields.

Microprocessor Emulator

The microprocessor emulator functionally models microprocessor hardware at a register transfer level. Emulation is accomplished by loading firmware object code directly into the modeled control memory and executing the firmware object code according to the model specification.

The hardware model was constructed using a register transfer simulation language processor (Computer Design Language) which was already available. This language contains most of the constructs, including implicit parallelism, necessary for the modeling procedure and facilities for output of hardware microprocessor states at each time increment during the emulation. The result is a complete listing of microprocessor register contents at the completion of each instruction during the execution of firmware object code. This listing allows a comparison of algorithm results from the FORTRAN simulation with algorithm results as implemented in firmware. Hardware checkout is also facilitated by the apriori knowledge of what machine registers should contain at a given point in algorithm execution. The emulator design characteristics are as follows:

- Emulation is by hardware modeling procedure in an existing register transfer simulation language
- Verifies firmware algorithms and hardware/firmware interface
- Knowledge of register contents at given times aids hardware checkout
- Hardware modeling procedure ensures consistency of hardware/firmware implementation
- Hardware model is easily modified, allows rapid comparisons between alternative hardware configurations
- Typical emulation is a 500 line program

In addition to firmware and hardware checkout capabilities, the microprocessor emulator provides the link which closes the verification chain illustrated in Figure G-16. The hardware modeling exercise also ensures consistency between actual hardware and assumptions used in developing firmware.

```

RGN13 AR: M1 < C2(D), M2 < T8(D), A2 < MP, C1(D) < (A1-A2),
          XJ(D), BR.JN.RGN13)
11 0 0 11 0 0 0 0 1010 010110 11 00 00 11 11 11 000 111 00 001 101 111 000 000101111011
OP P I UM X K B A BRCH ALUOP XJ XI XR XT X2 X1 C2M C1W MW M2L M1L A2L A1L ADDRESS B

```

Figure G-16. Assembler List Output Example

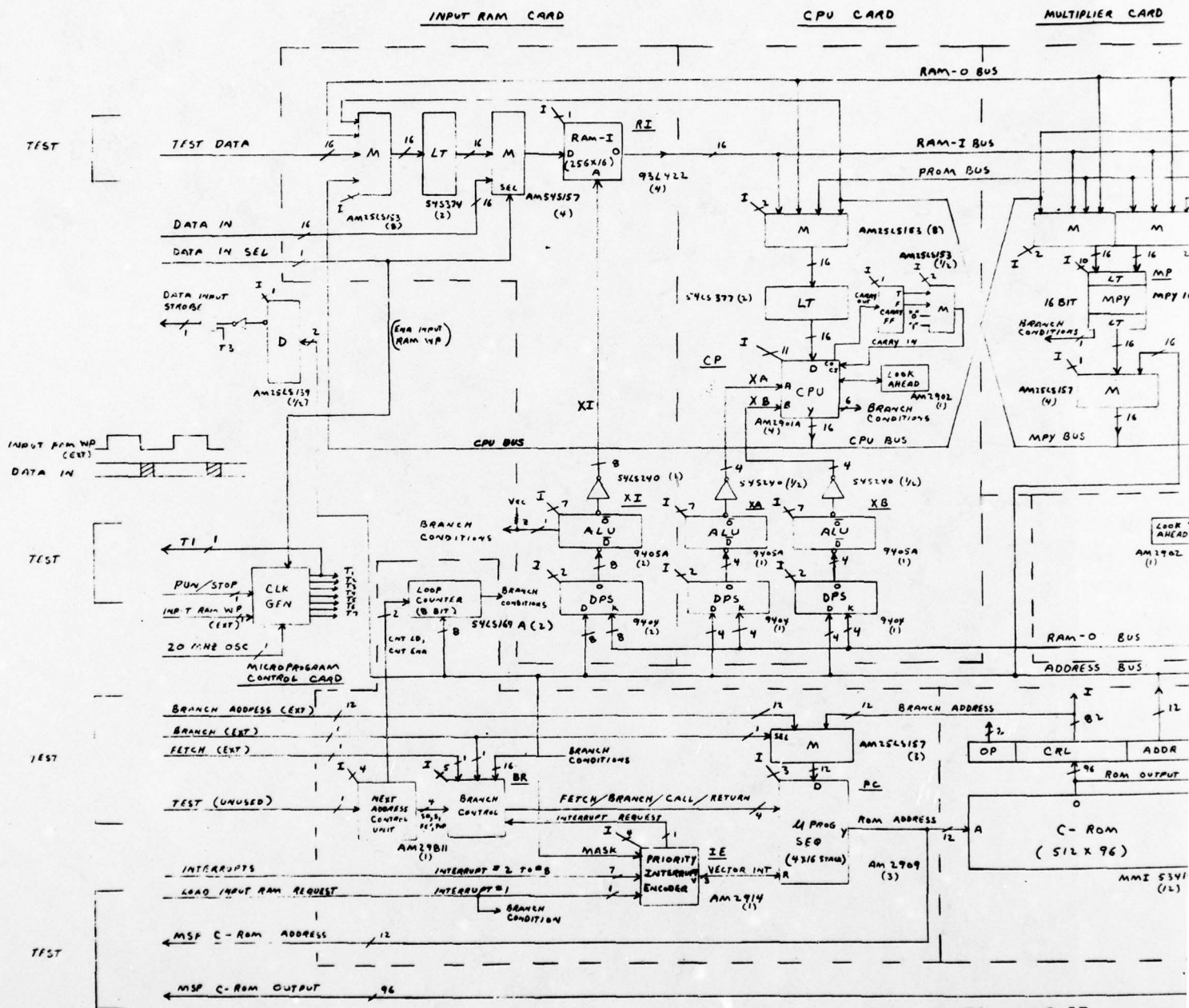
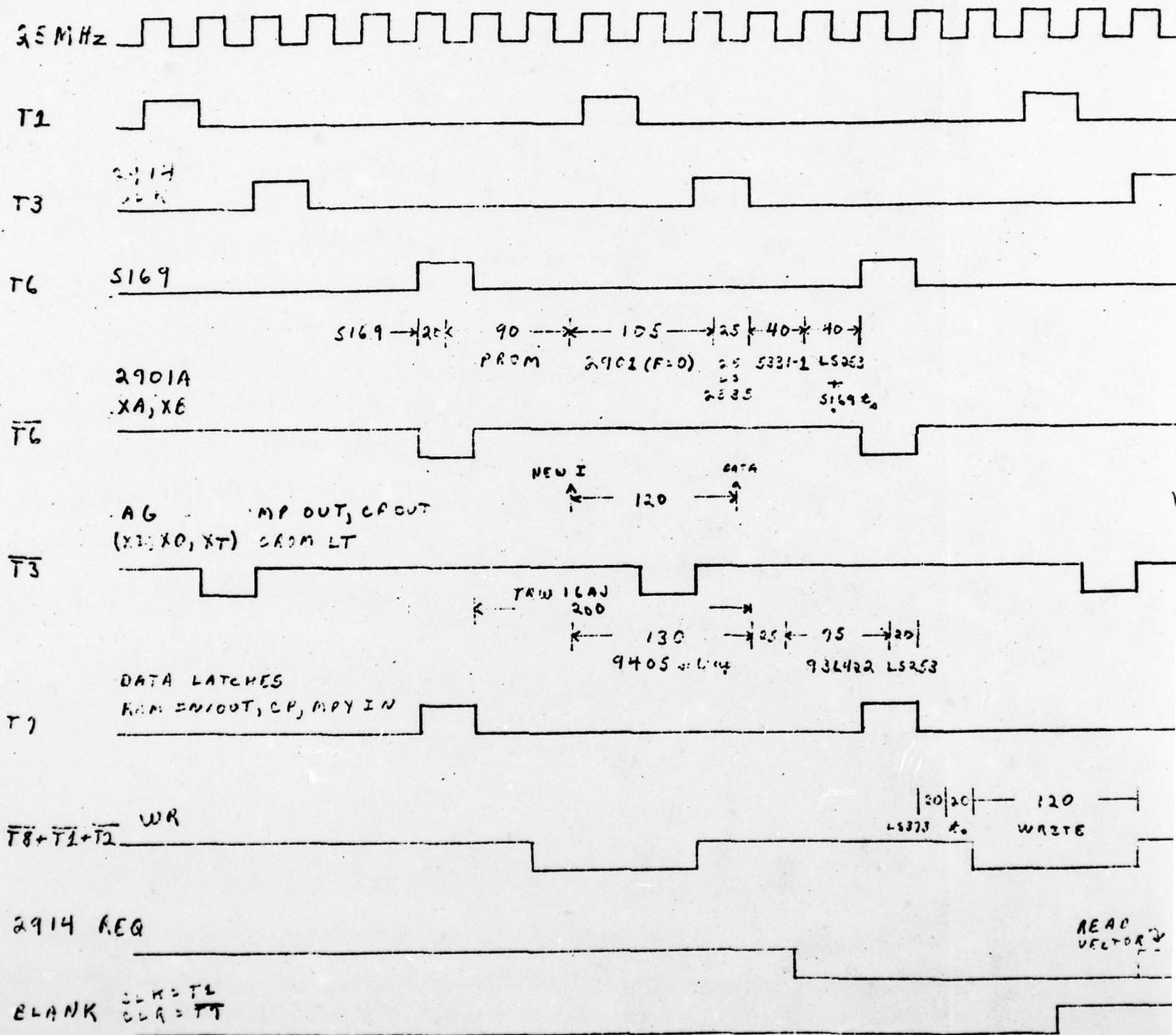


Figure G-17
MICRO-SIGNAL-PROCESSOR B.

MSP BASIC TIME



SP BASIC TIMING

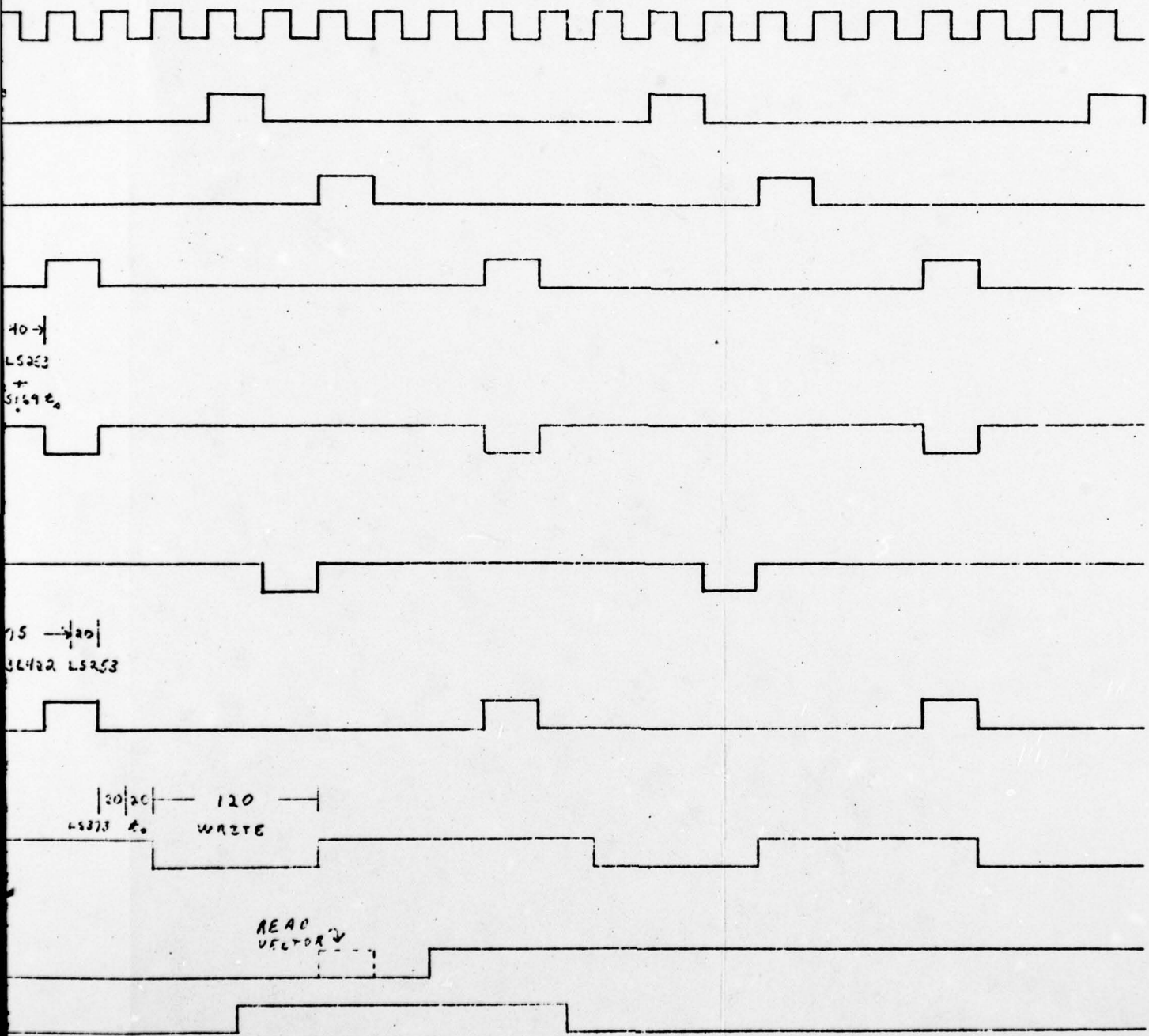
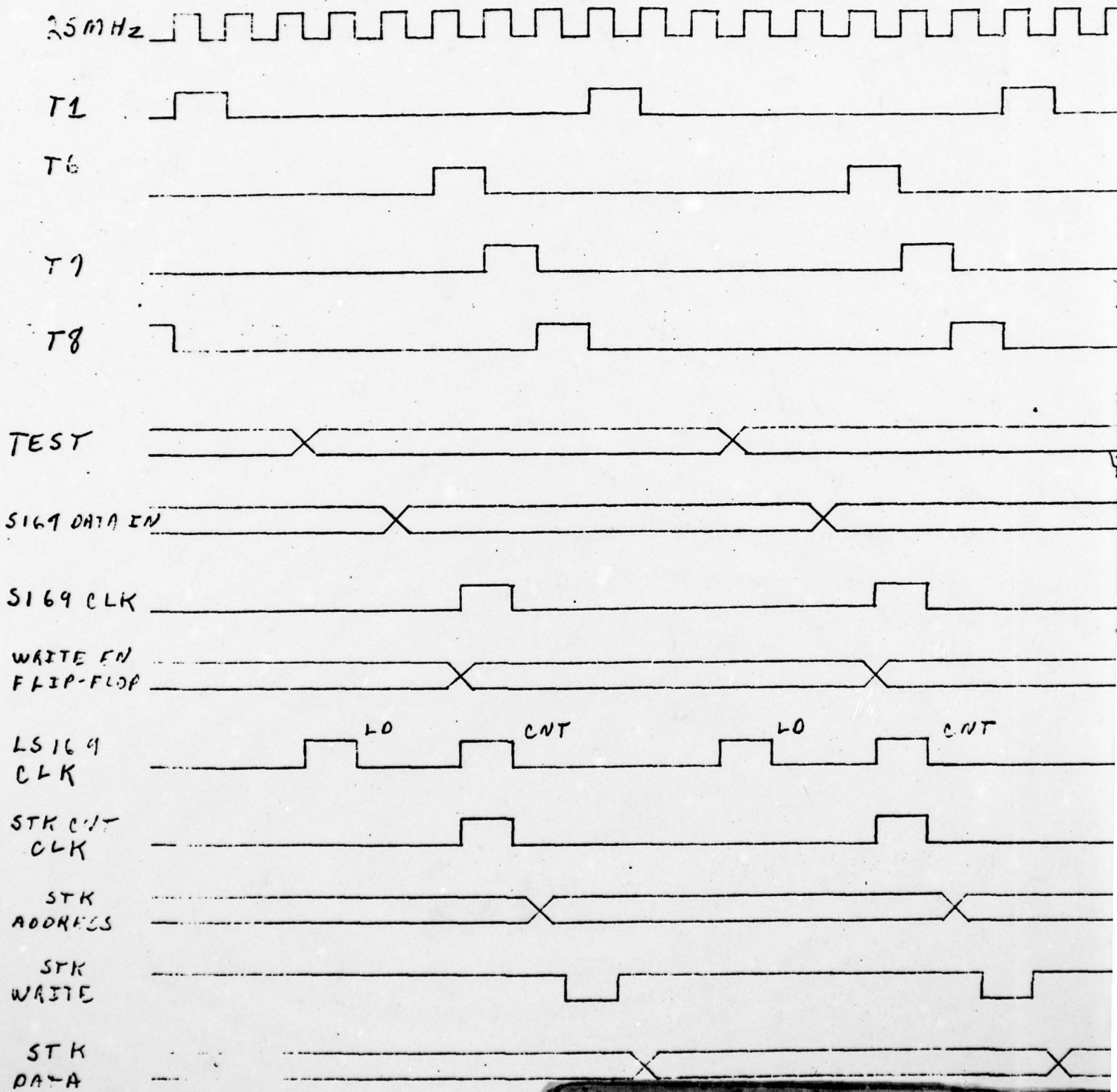


Figure G-18

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DETAILED CONTROLLER T



ROLLER TIMING

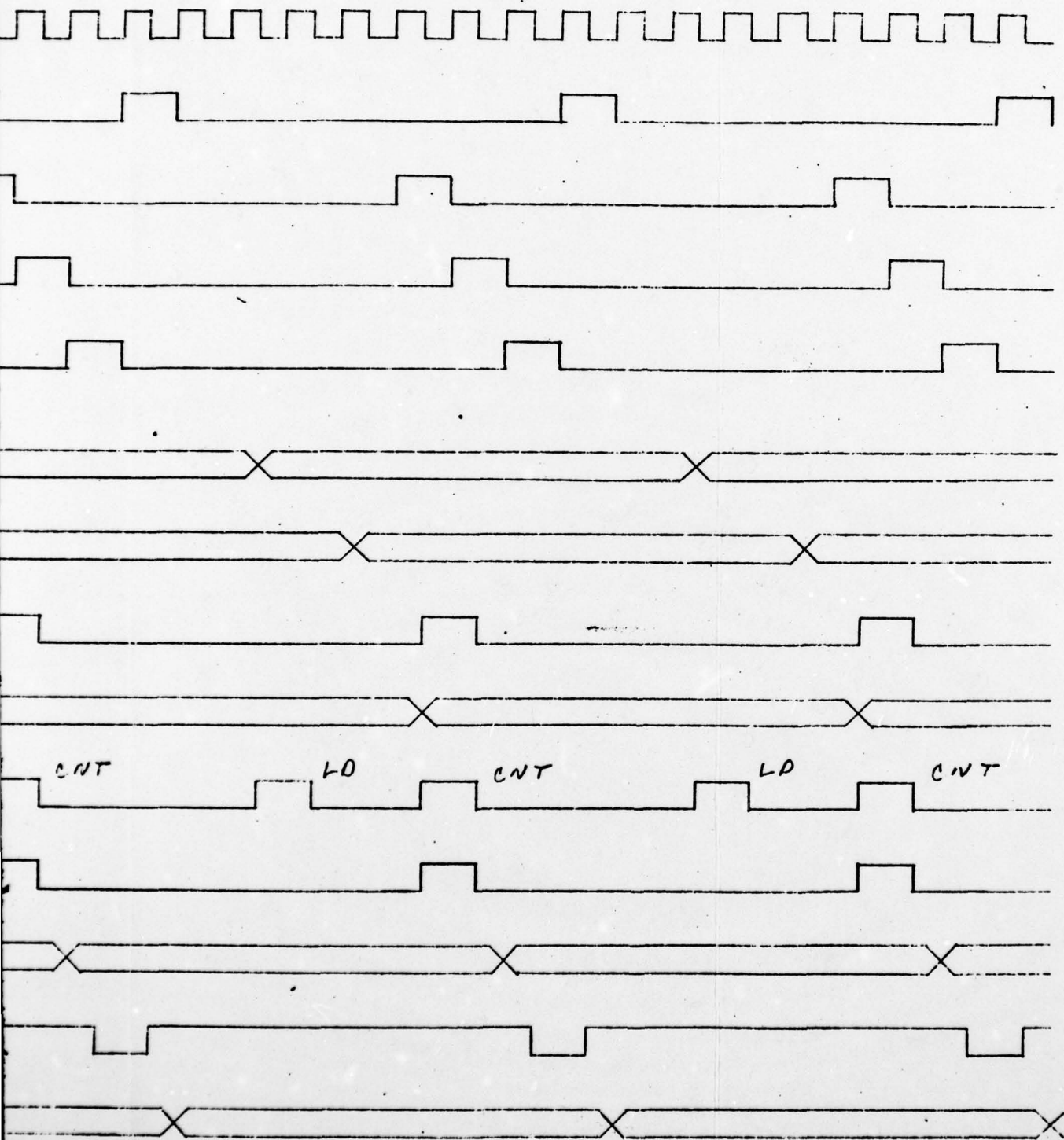
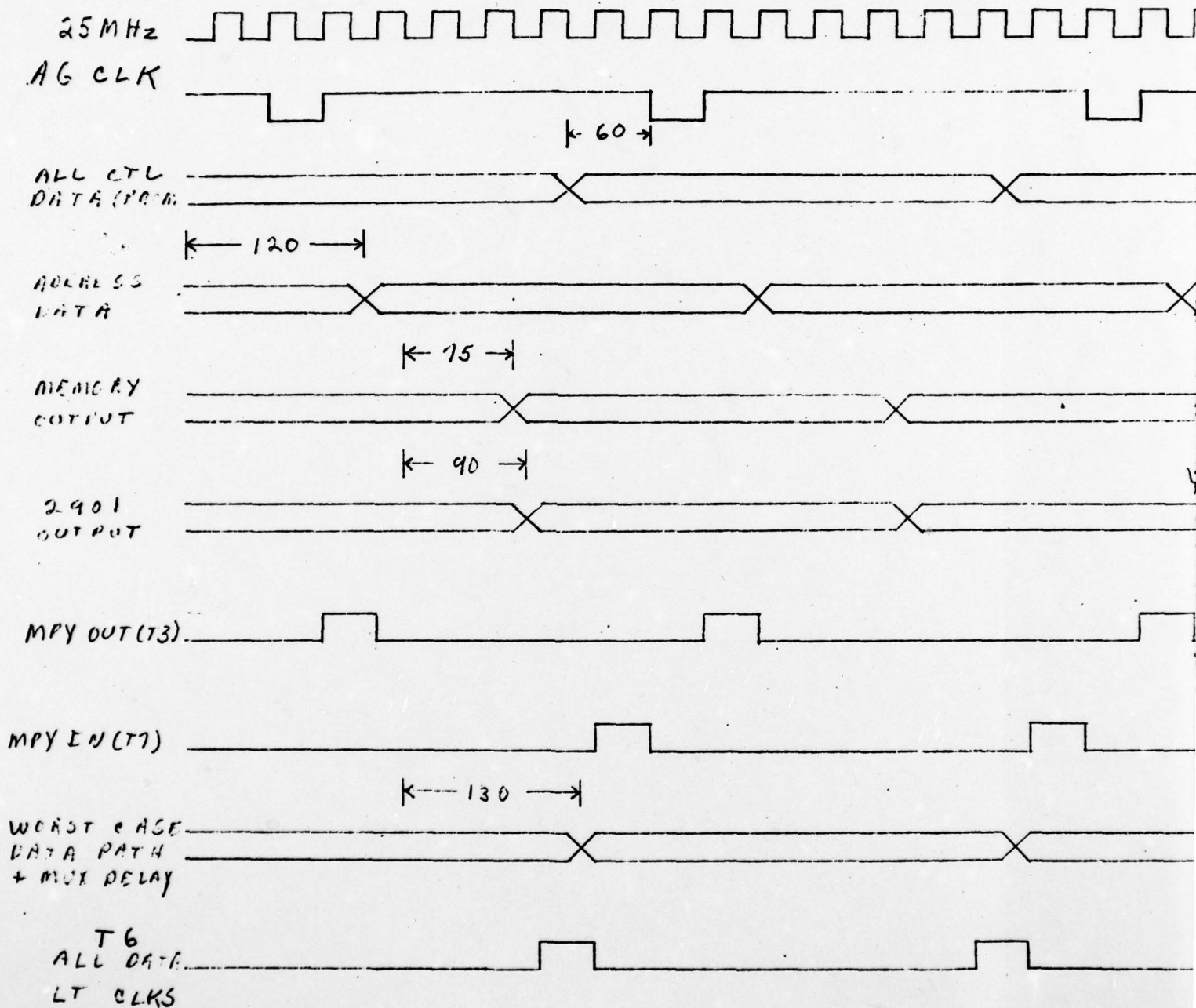


Figure G-19

DETAILED CPU TIMING



2 TIMING

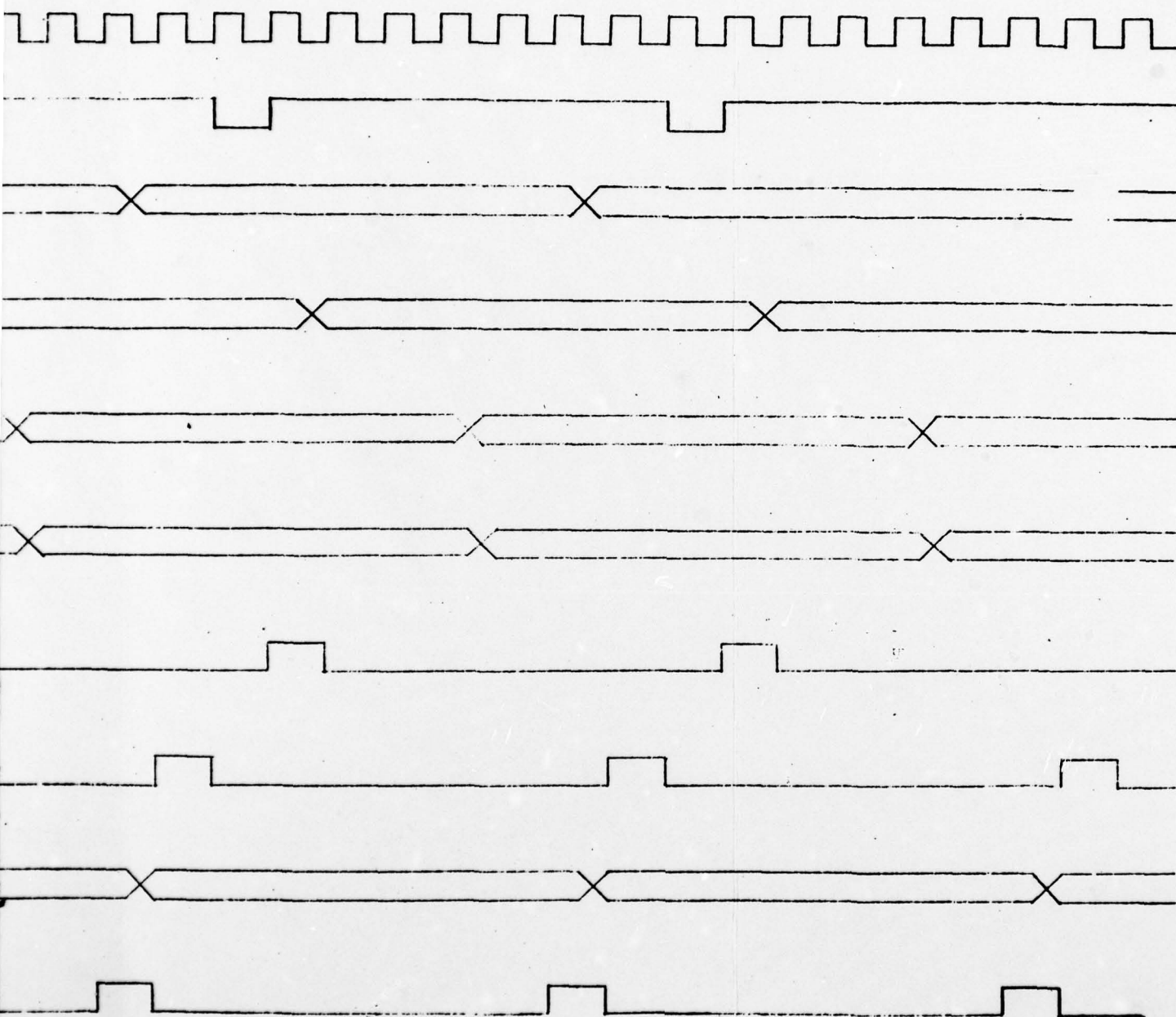
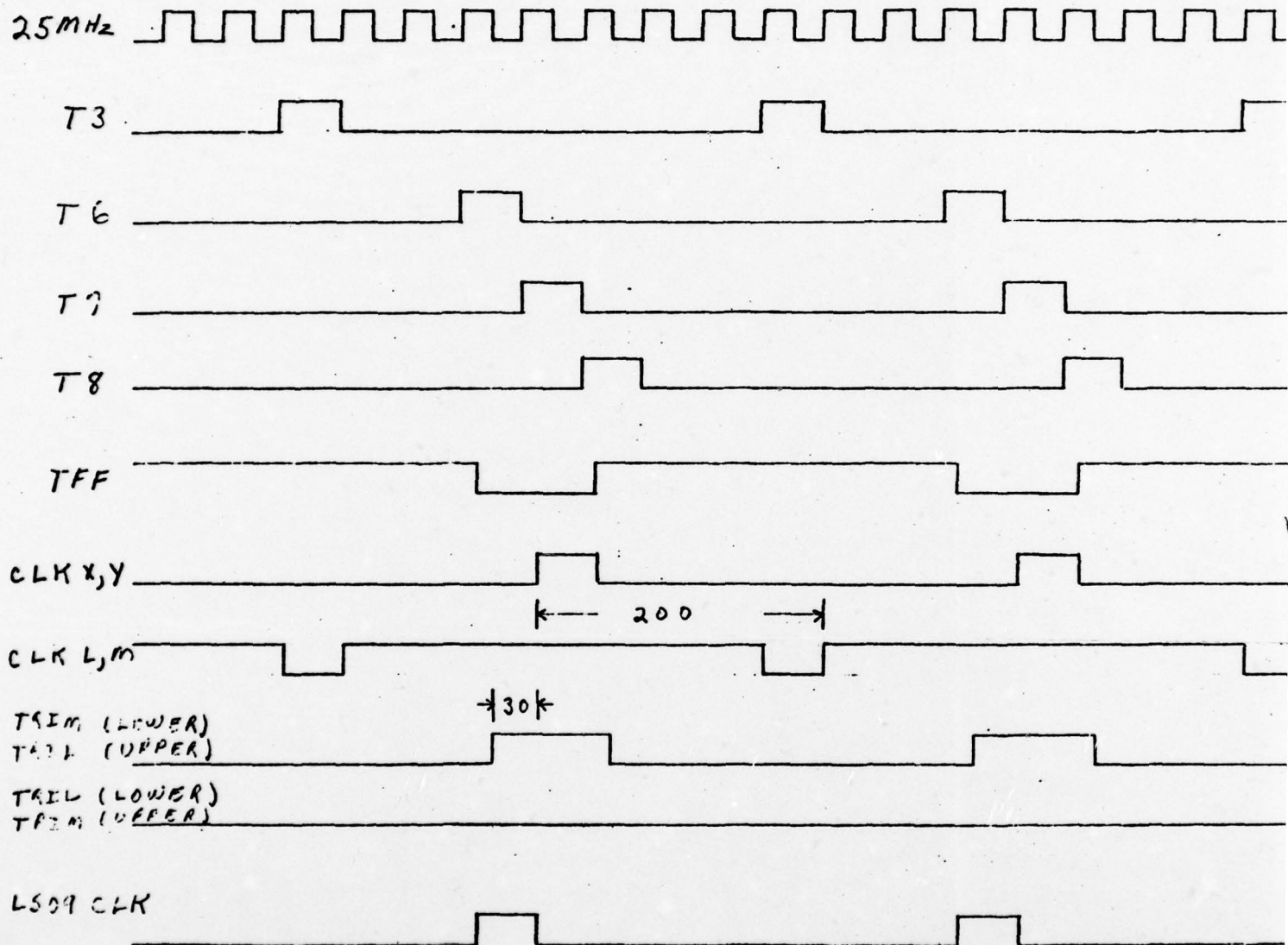


Figure G-20

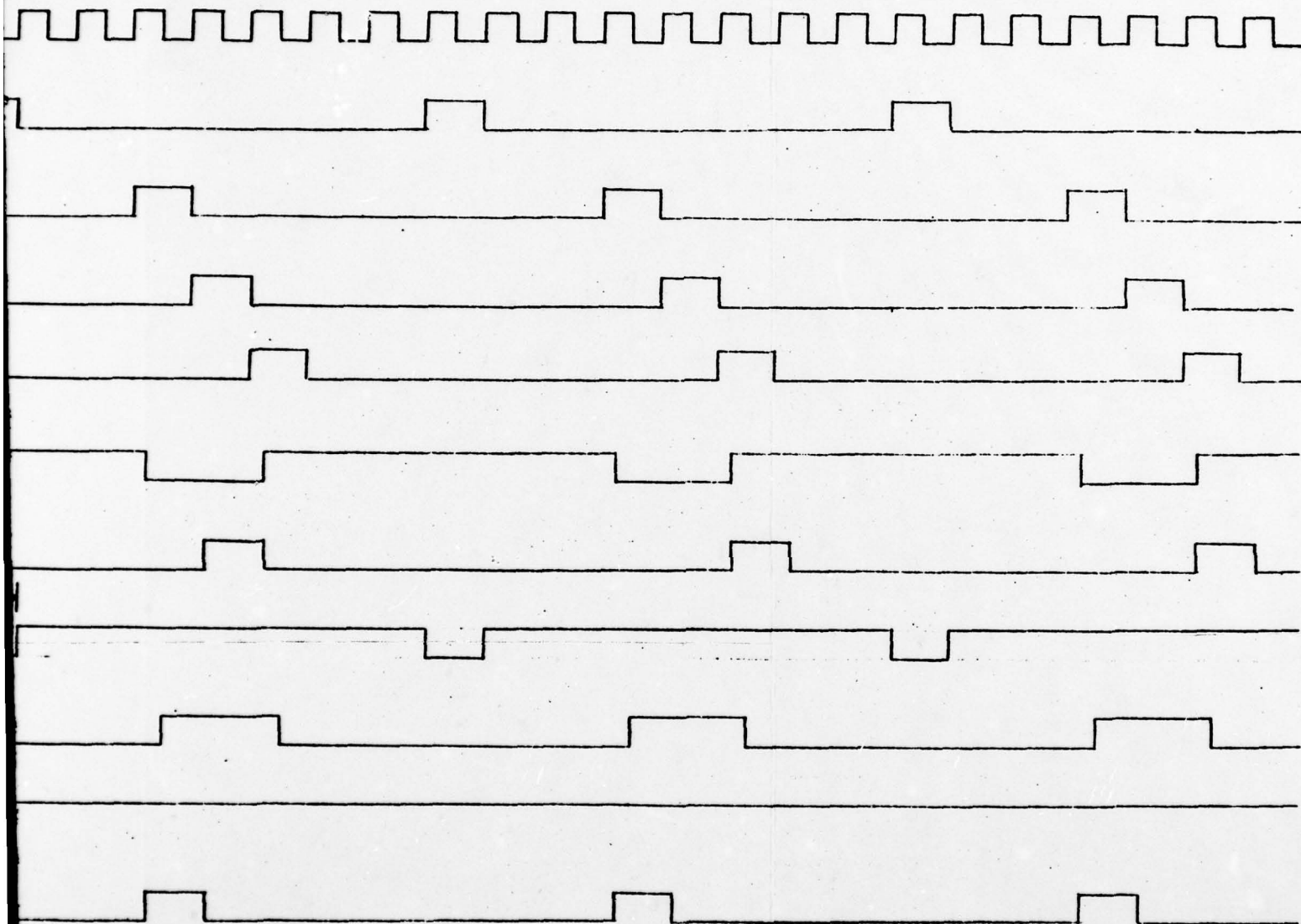
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2

DETAILED MULTIPLEX



DETAILED MULTIPLIER TIMING

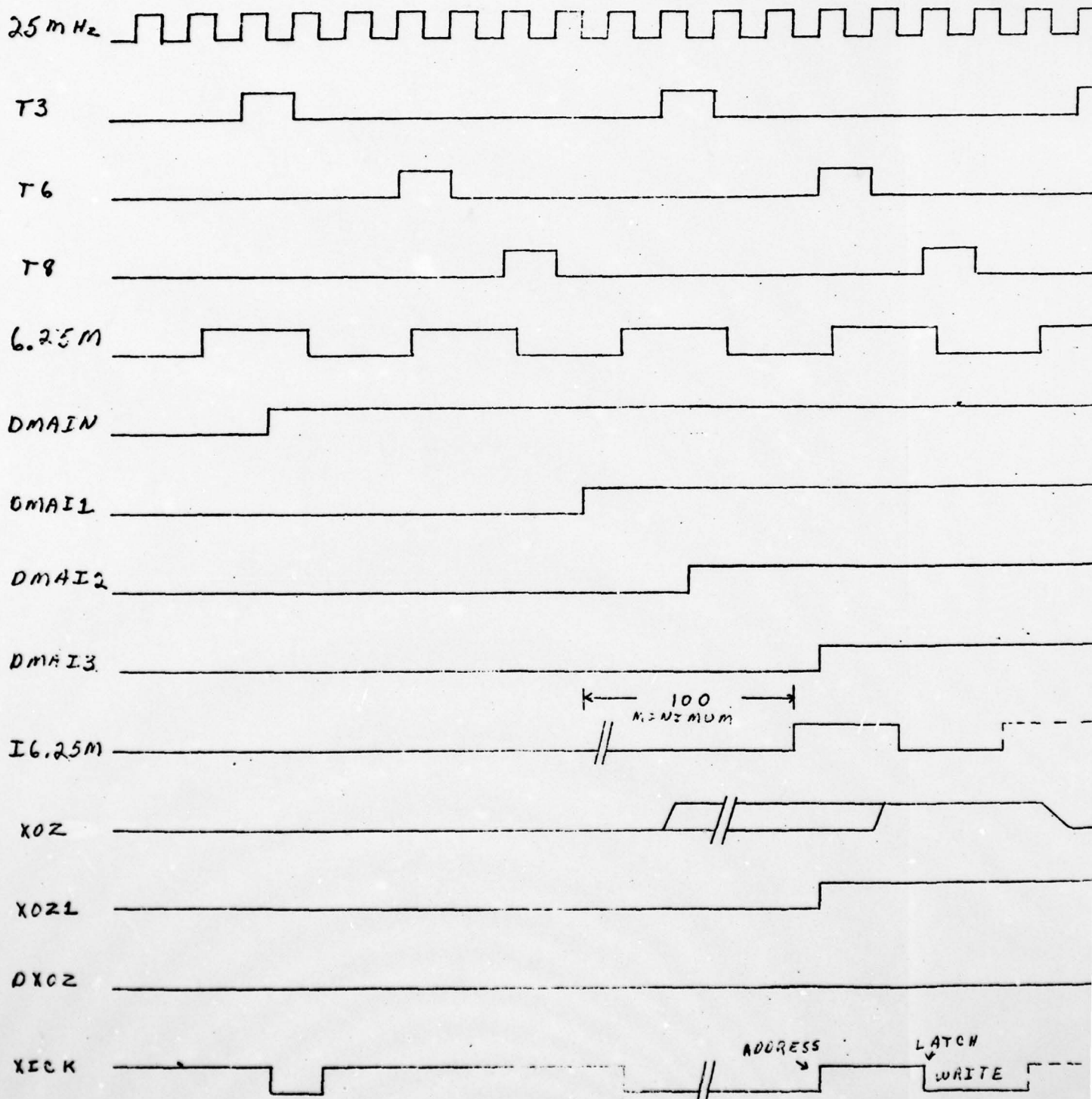


2

Figure G-21

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INPUT DMA TIMING



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STANDARD AVIONICS MODULES (SAM) FOR EXISTING MODEMS. (U)
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DMA TIMING

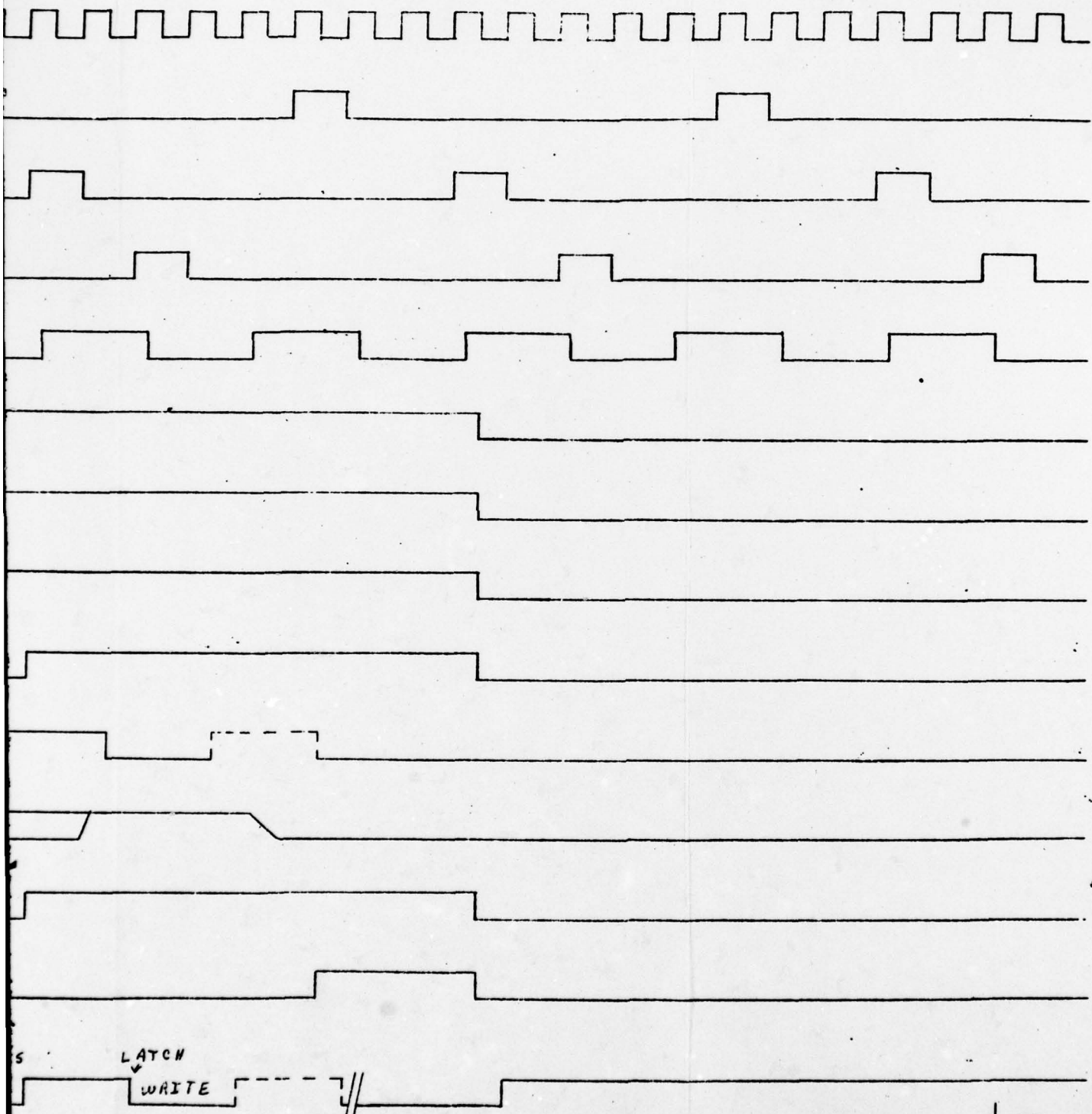


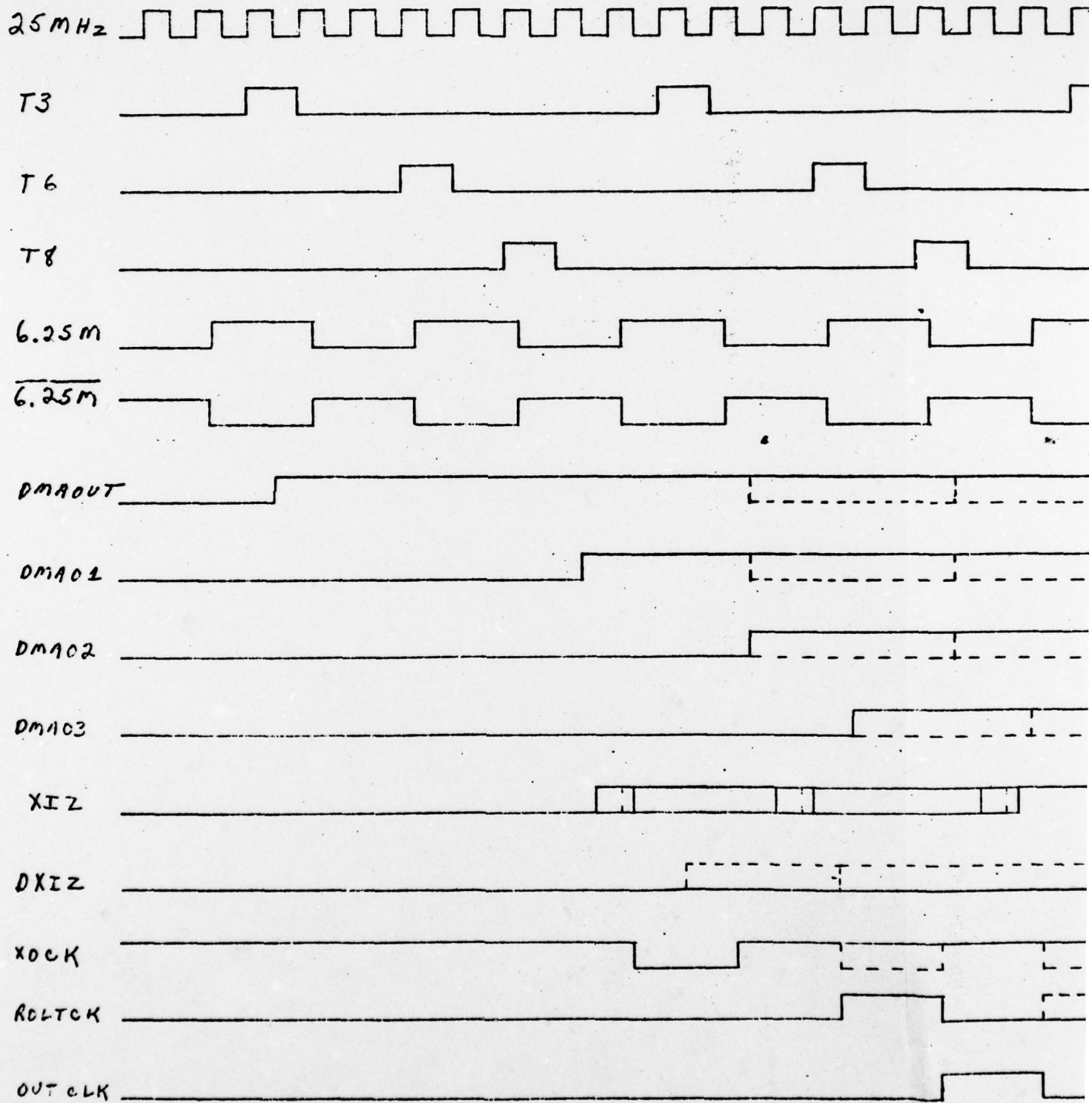
Figure G-22

275

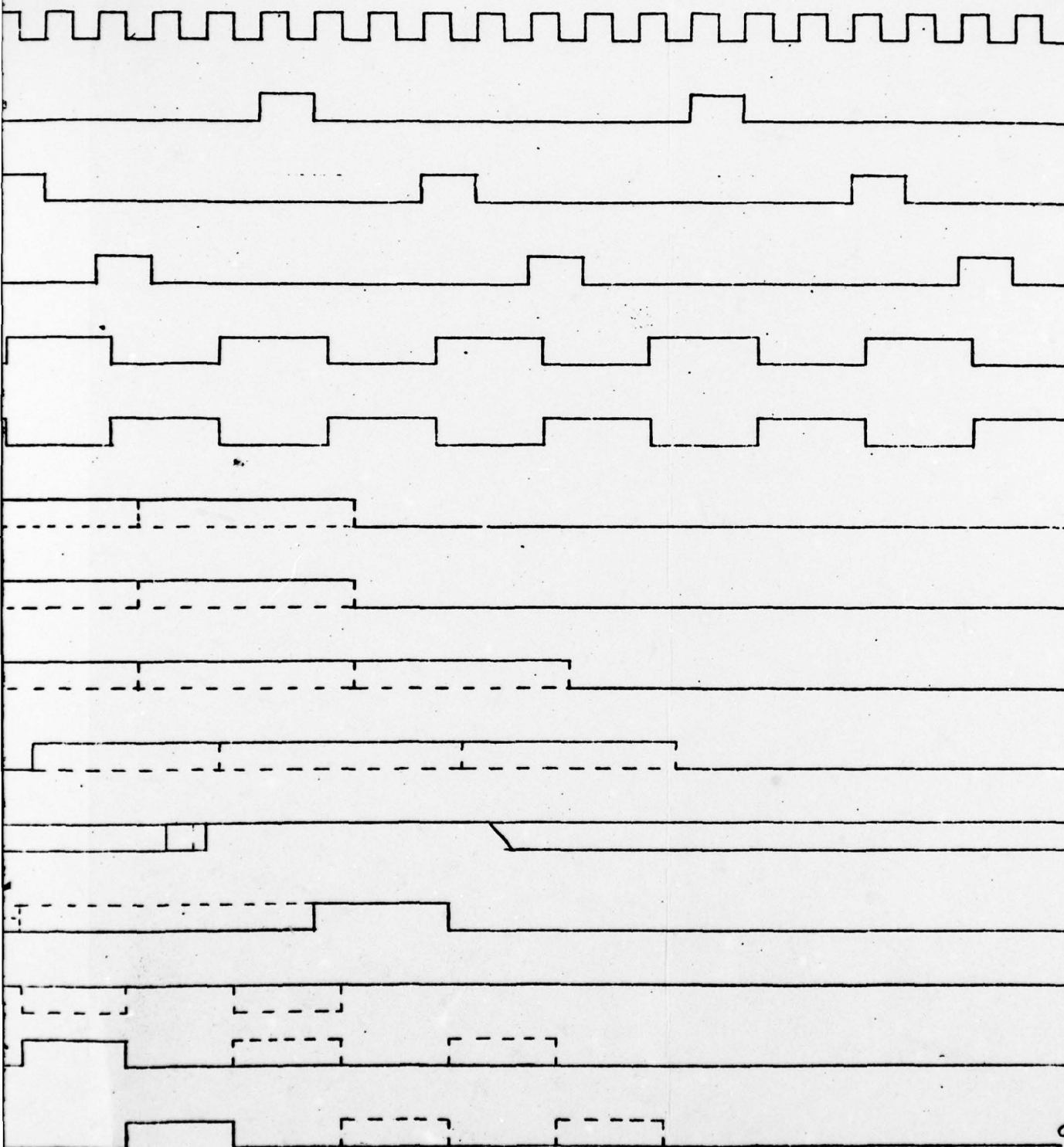
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OUTPUT DMA TIMING



T DMA TIMING



LRS

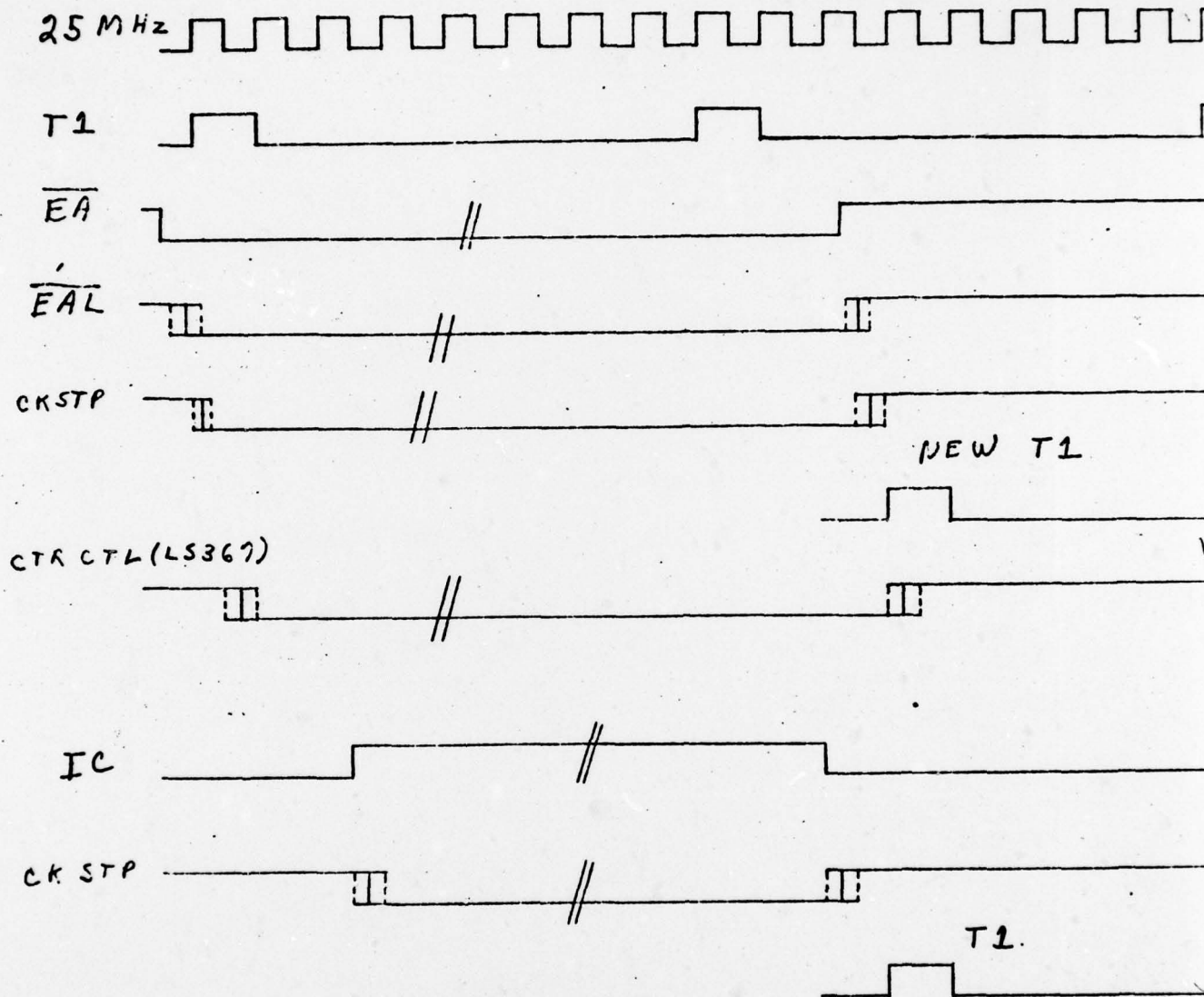
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Figure 6-23

2

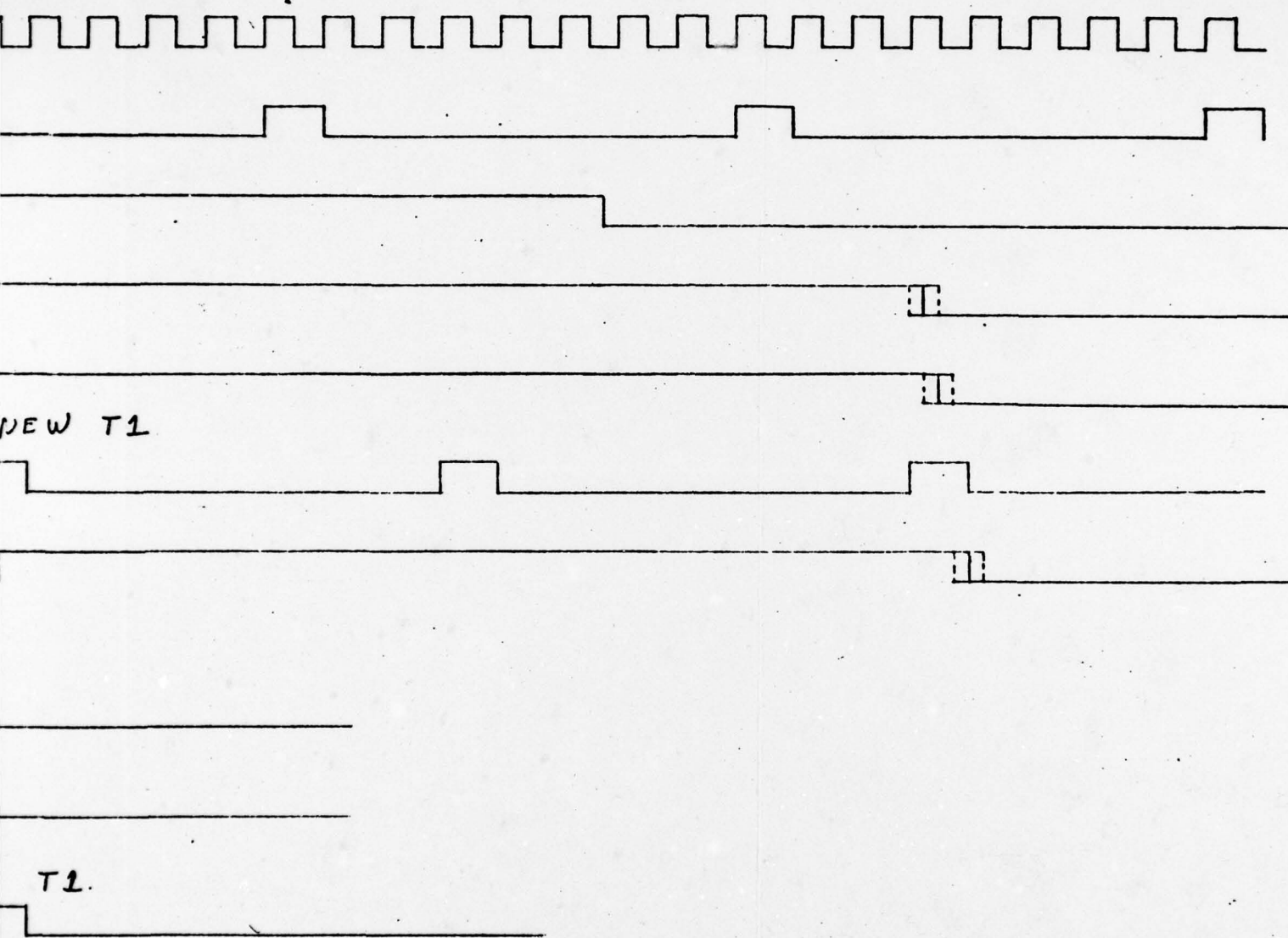
CONT

EXTERNAL ADDRESS - 1



CONTROLLER

ADDRESS - INITIAL CONDITION TIMING

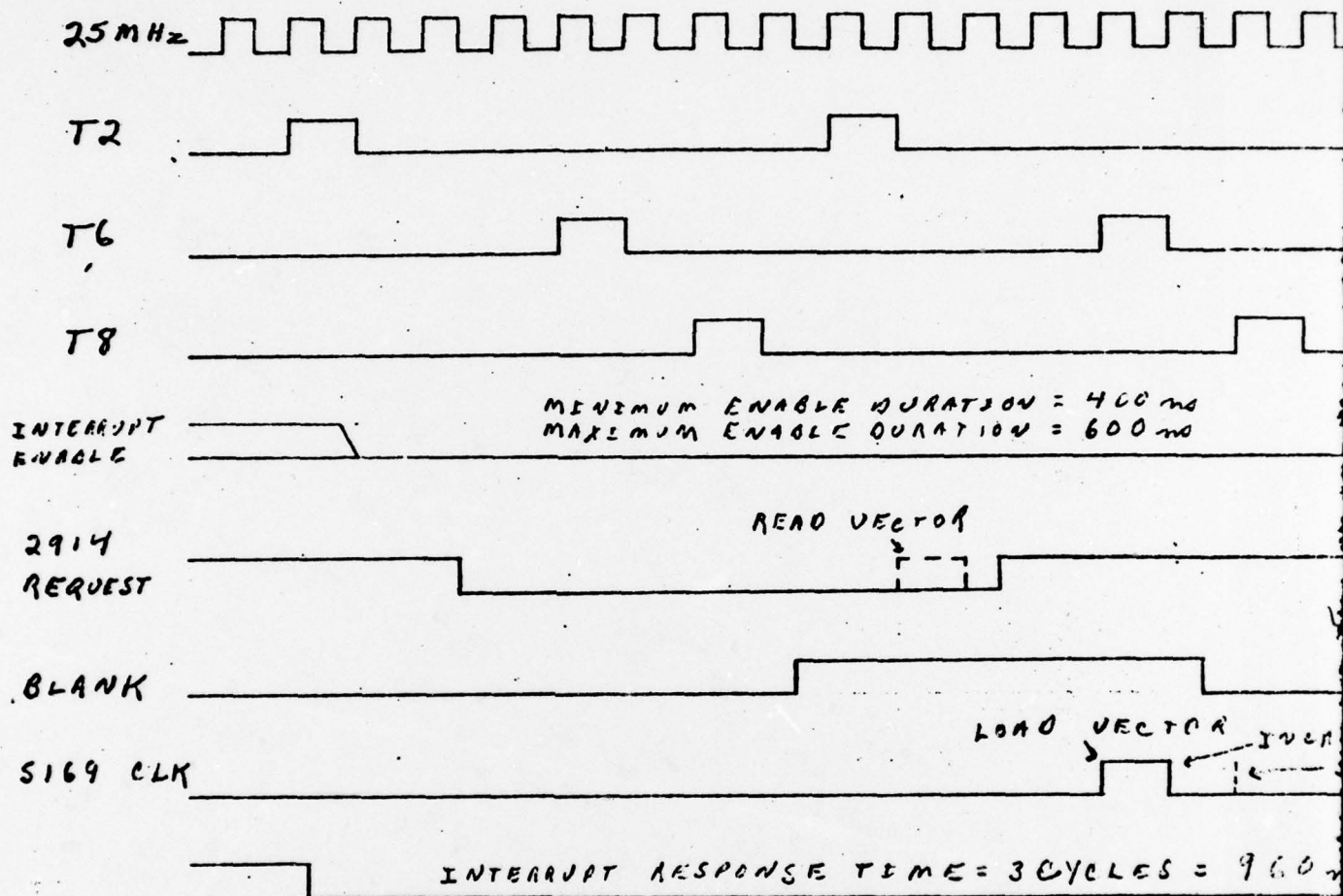


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Figure G-24

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INTERRUPT



INTERRUPT TIMING

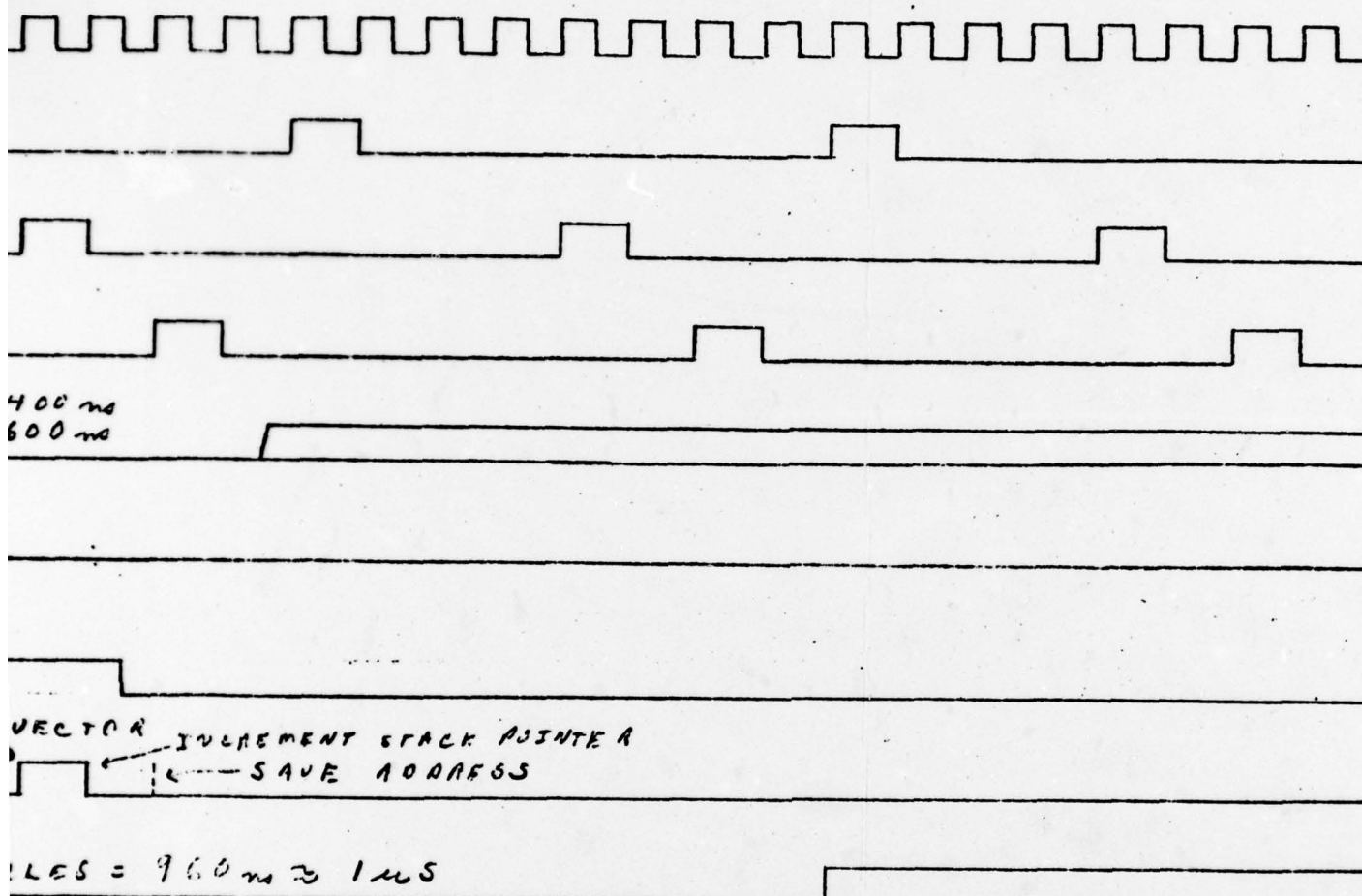


Figure G-25

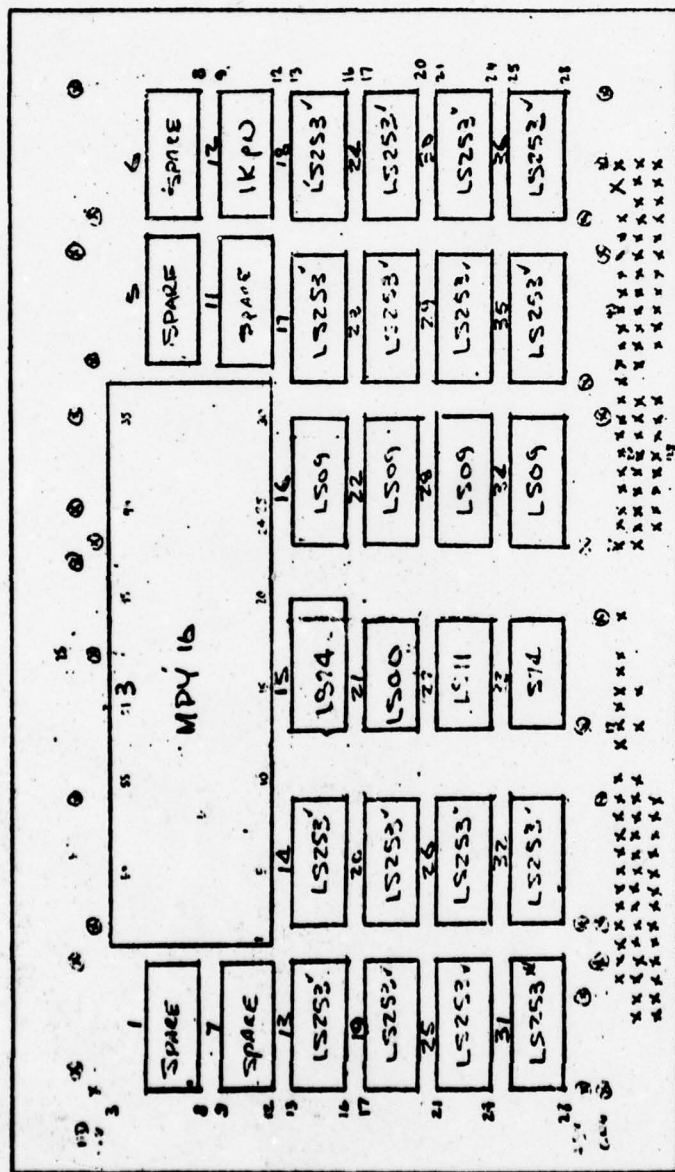
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CARD LOCATION

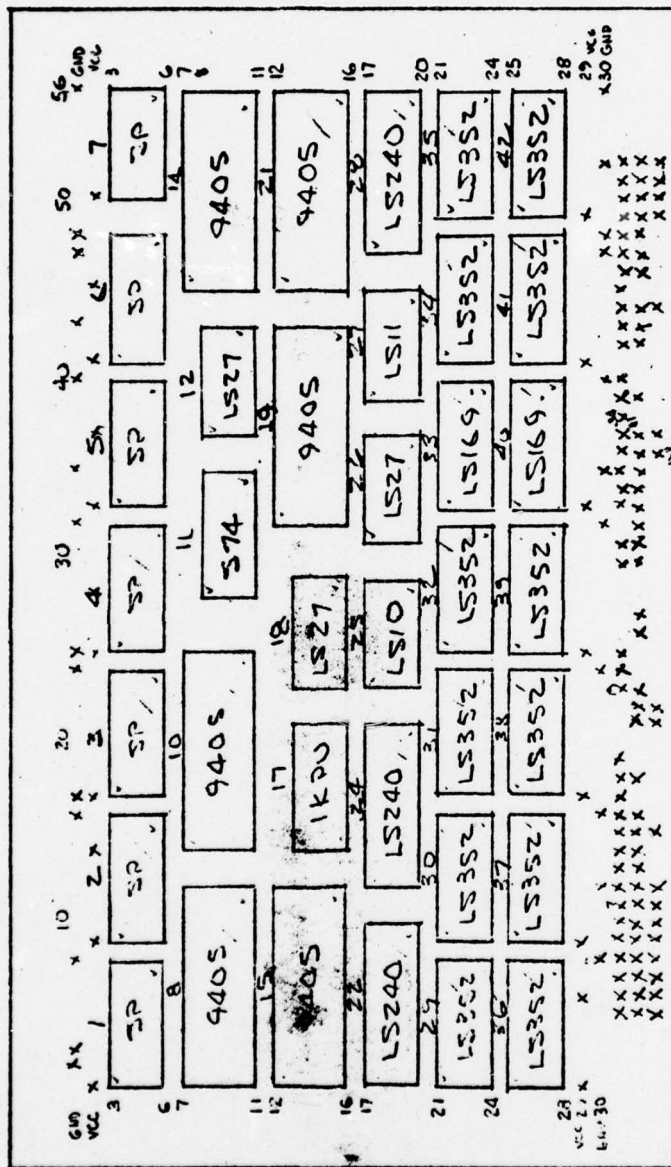
<u>NAME</u>	<u>DISCRIPTION</u>	<u>CONNECTOR NO.</u>
1. CRAM 1	CONTROL RAM	23
2. CRAM 2	" "	22
3. CRAM 3	" "	21
4. IRAM	INPUT RAM	20
5. ORAM	OUTPUT RAM	19
6. CONT	CONTROLLER	18
7. I/O	INPUT/OUTPUT	17
8. AG	ADDRESS GENERATOR	16
9. CPU	CPU	15
10. MPY	MULTIPLIER	14

Zil 11KPy



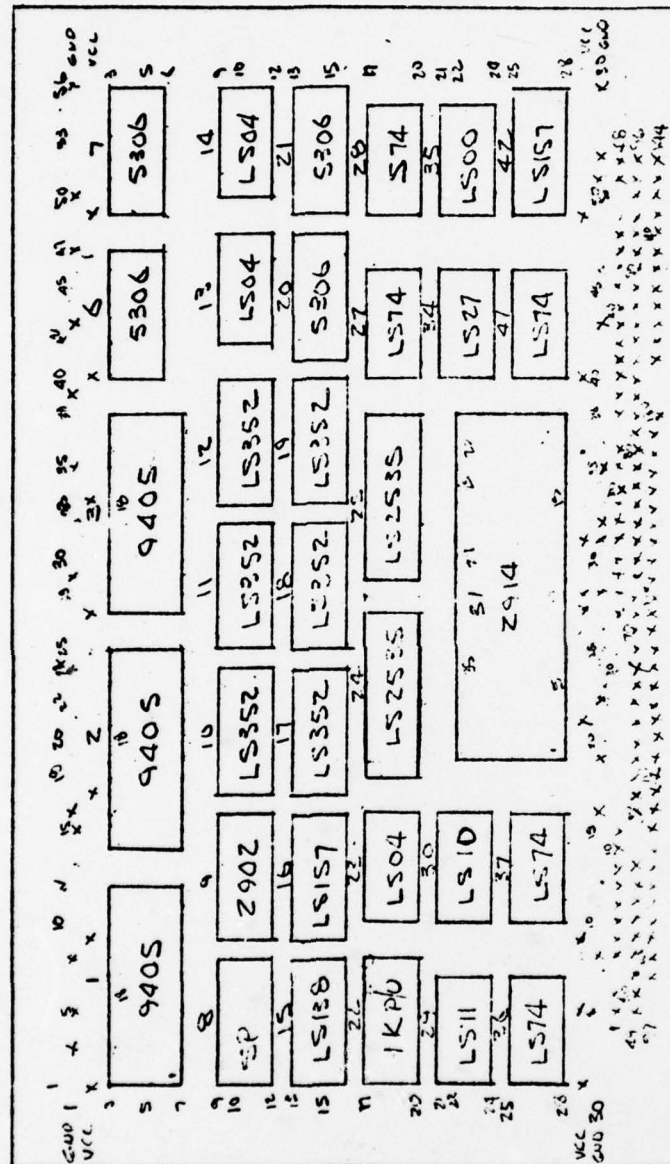
LOCATION CHART

MPV



LOCATION CHART

ADD GEN



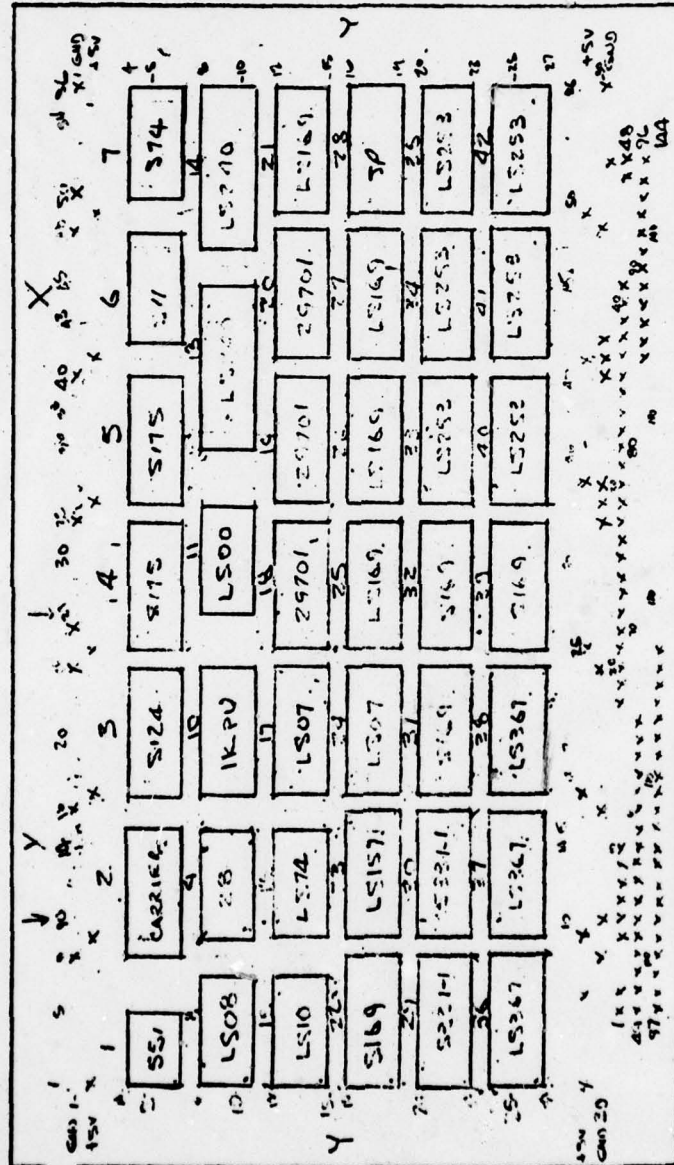
NOT SPARE PAPER

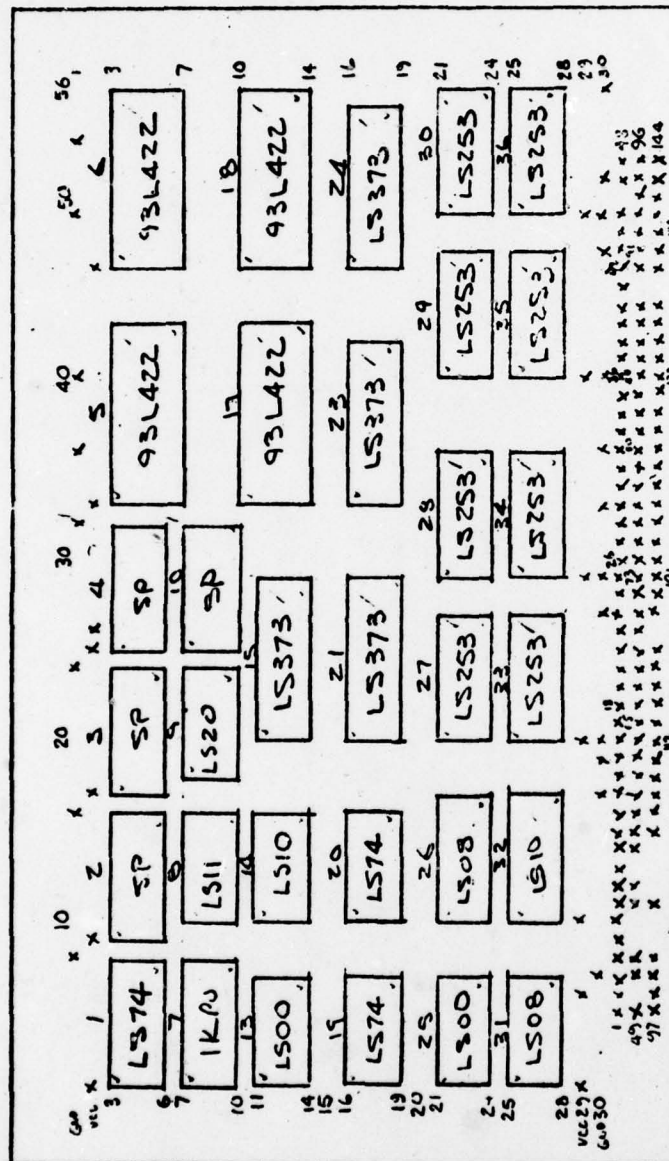
24 25

LOCATION CHART

I/O

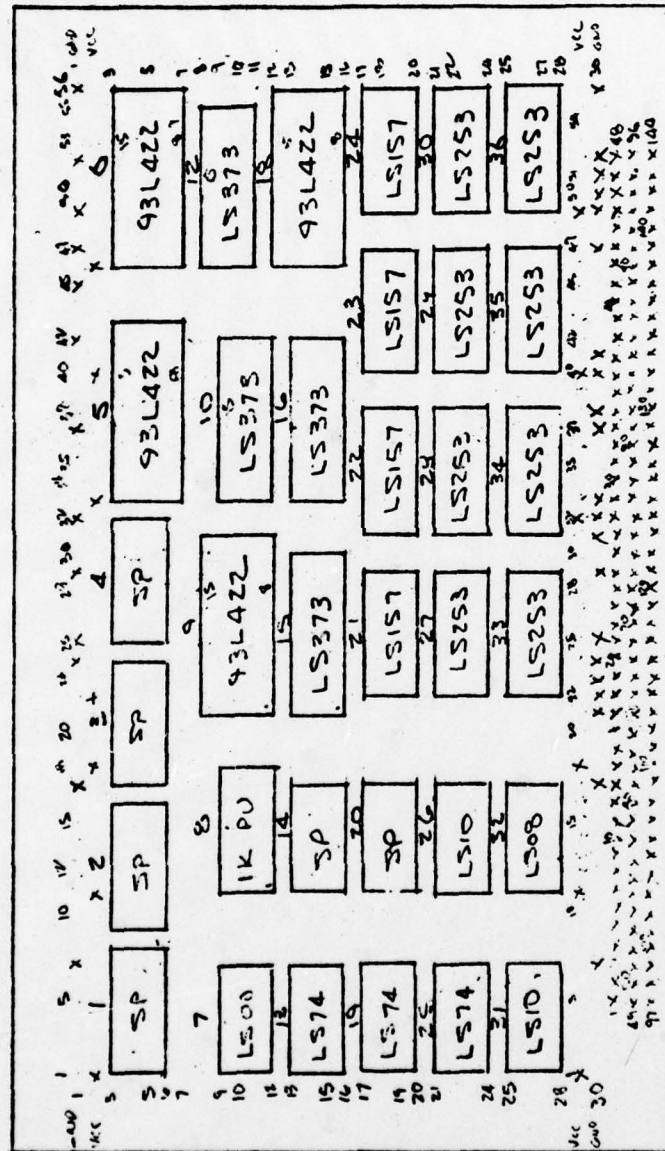
LOCATION CHART
CONTROLLER





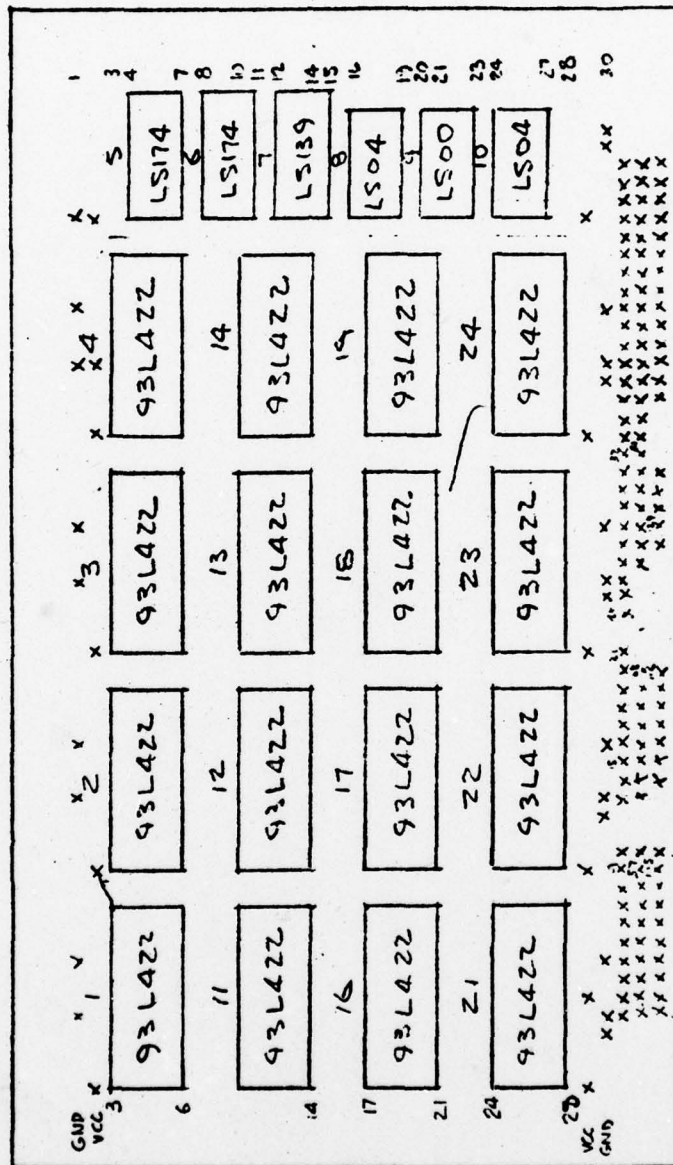
LOCATION CHART

OUTPUT RAM



LOCATION CHART

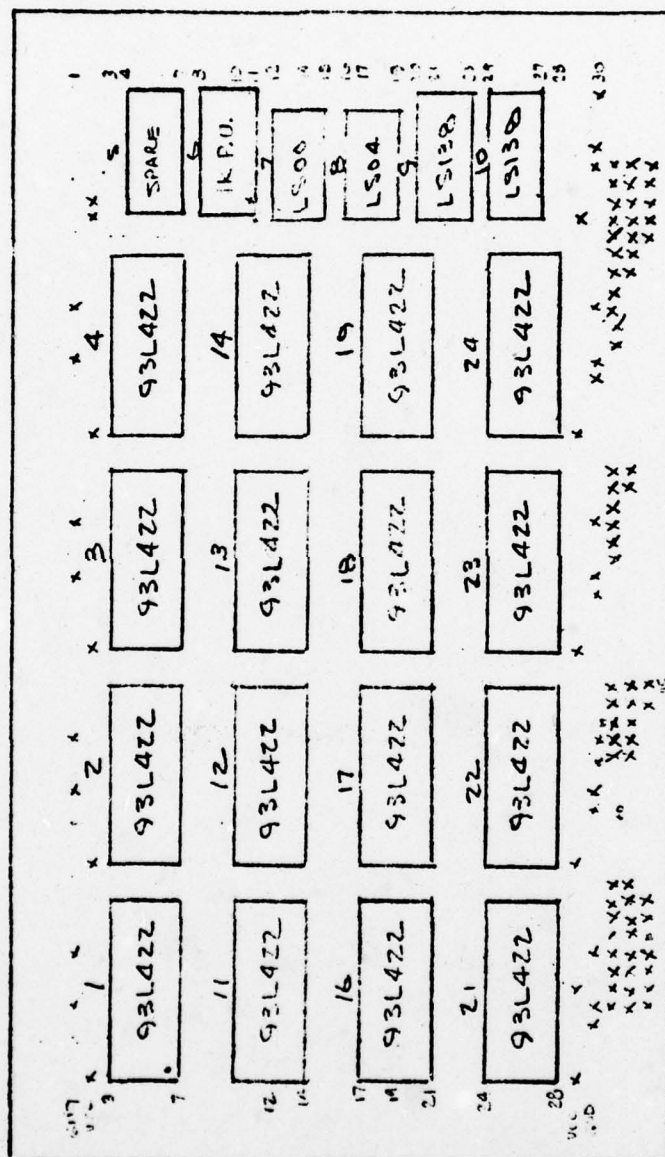
INPUT RAM



LOCATION CHART

GRAM 3

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8 LS138 (16)	9 LS74 (14) 59	10 LS04 (14) 246 81012	11 LS169	12 LS169	7 LS367 (16) 357 91113	8 LS74 (14) 59	9 LS00 (14) 36 811	10 1K (16) 15	11 1K (16) 14	12 LS04 (14) 246 81012
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ENGINEERING SKETCH

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SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

MSP TEST ADAPTER
LOCATION CHART

SIZE

CODE IDENT NO.

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COMPONENT S

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13	14	15	16	17	18
LS00 (14) <u>3 6</u> <u>8 11</u>	LS04 (14) <u>2 4 6</u> <u>8 10 12</u>	LS367 (16)	4.7K (16) <u>12</u>	LS04 (14) <u>2 4 6</u> <u>8 10 12</u>	LS04 (14) <u>2 4 6</u> <u>8 10 12</u>
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LS251 (16)	LS251 (16)	LS251 (16)	LS251 (16)	LS157 (16)
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LS251 (16)	LS251 (16)	LS251 (16)	LS251 (16)	LS367 (16)
13	14	15	16	17
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ENGINEERING SKETCH

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ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

MSP TEST ADAPTER
LOCATION CHART

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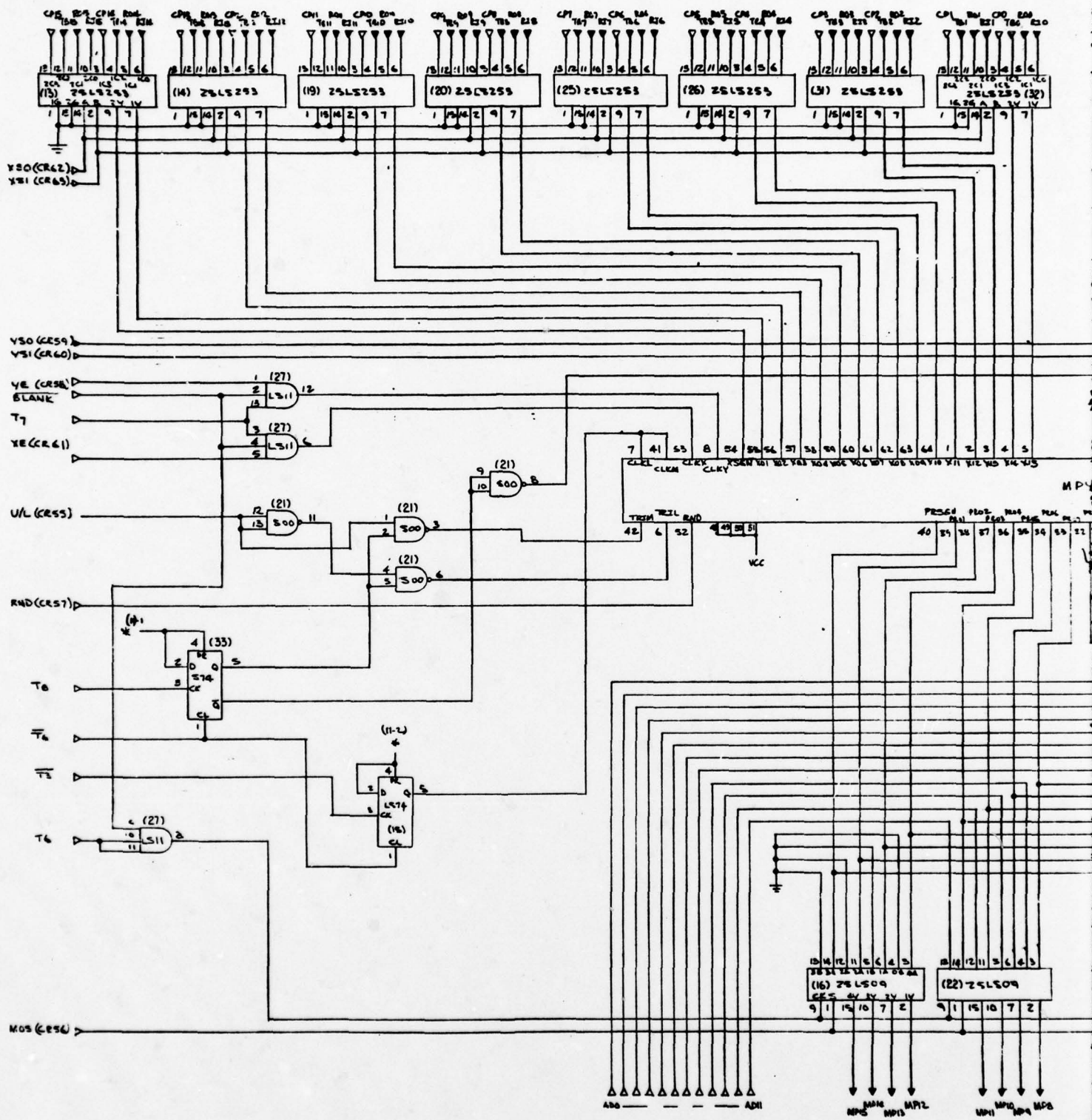
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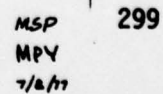
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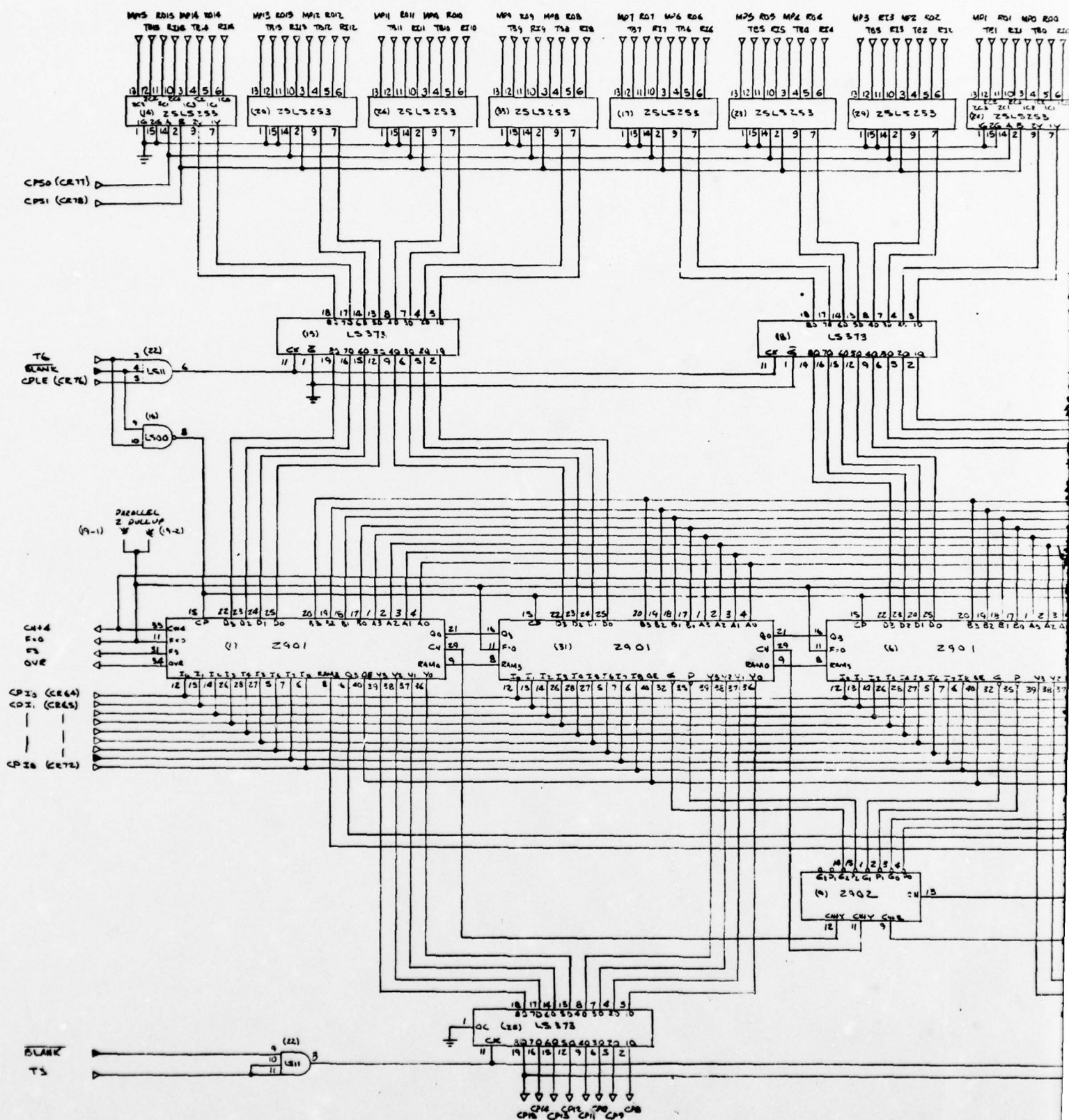
SHEET 2 OF 2

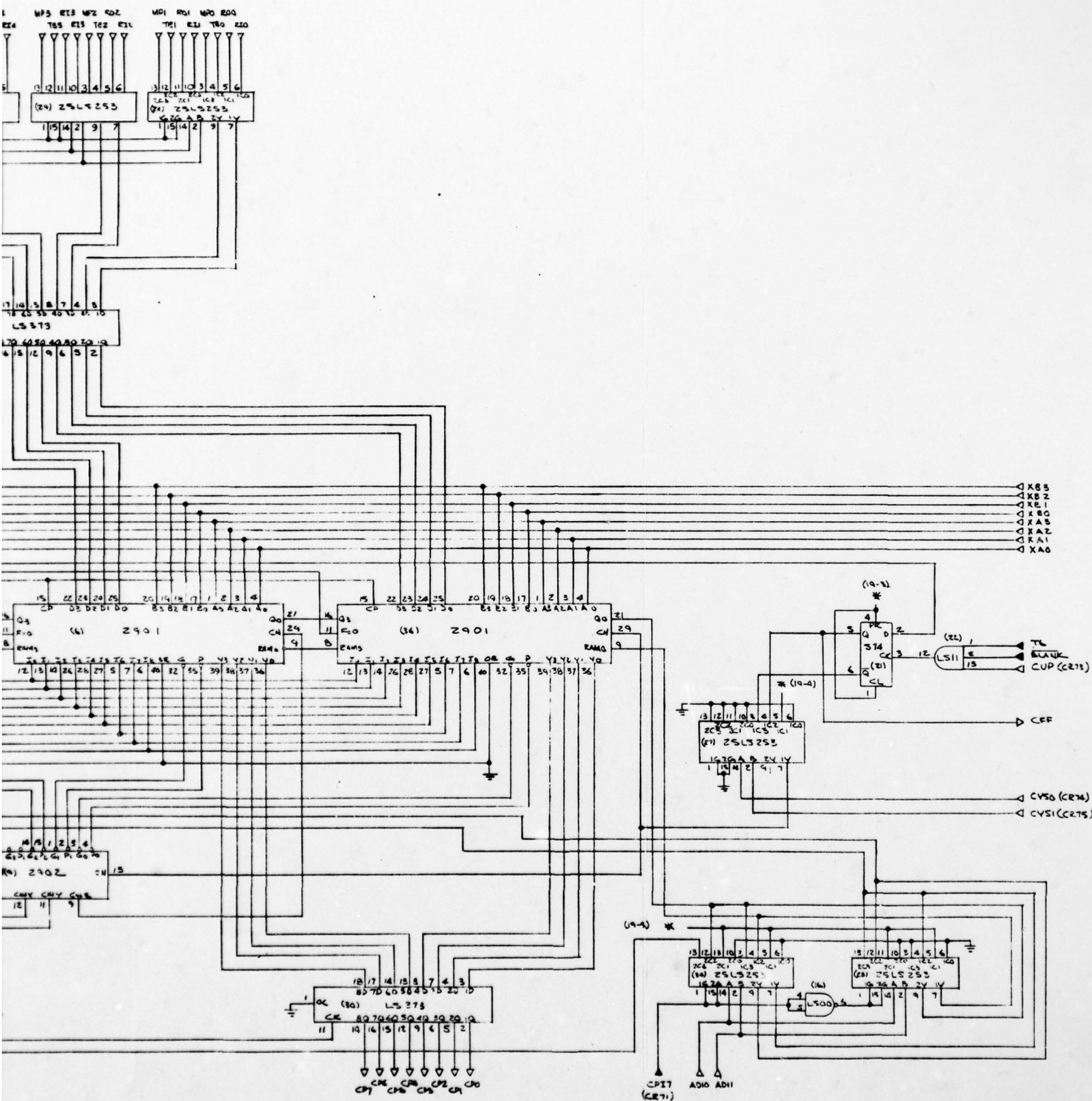
SYSTEMS 3663 REV. 12-71





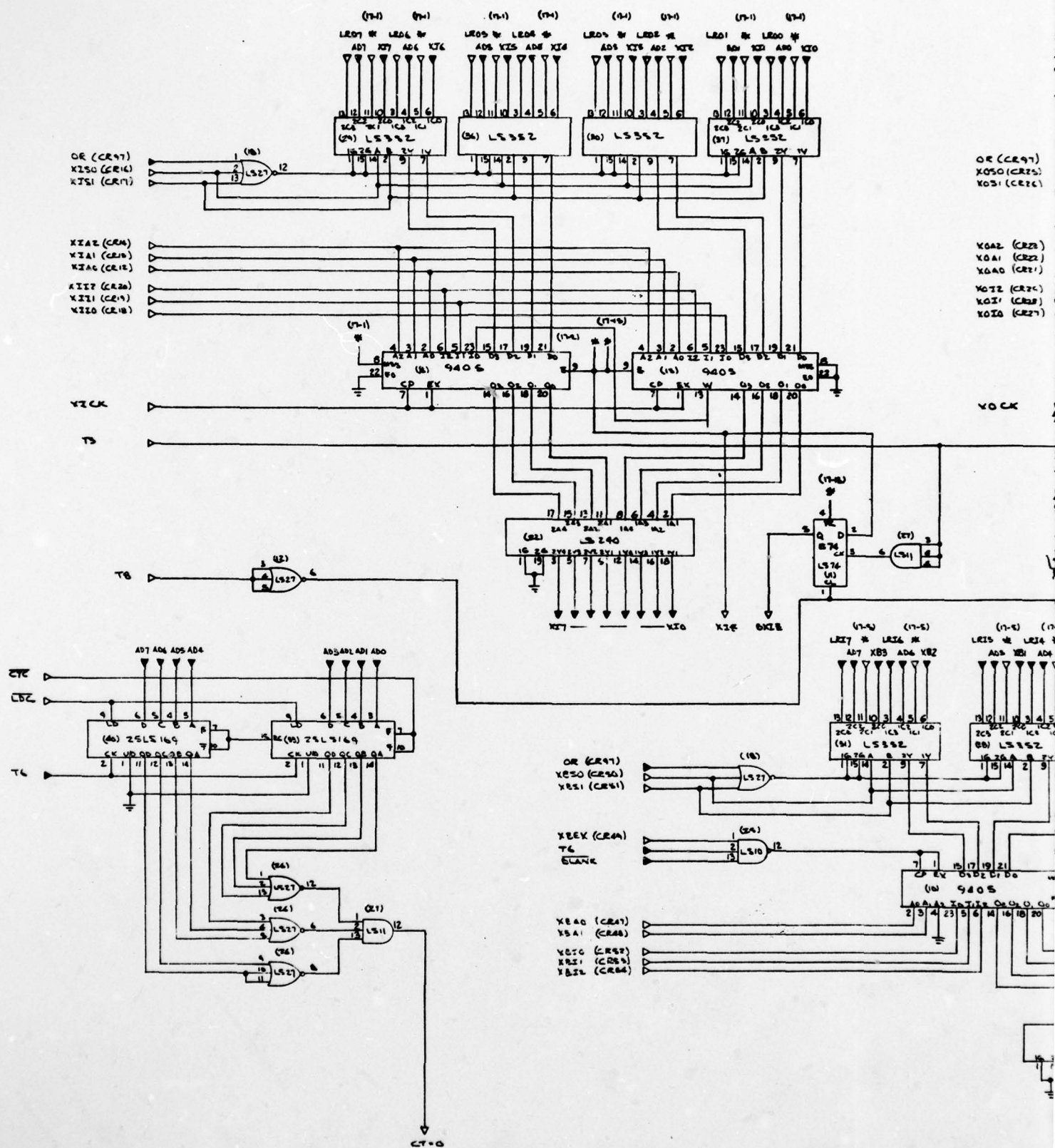
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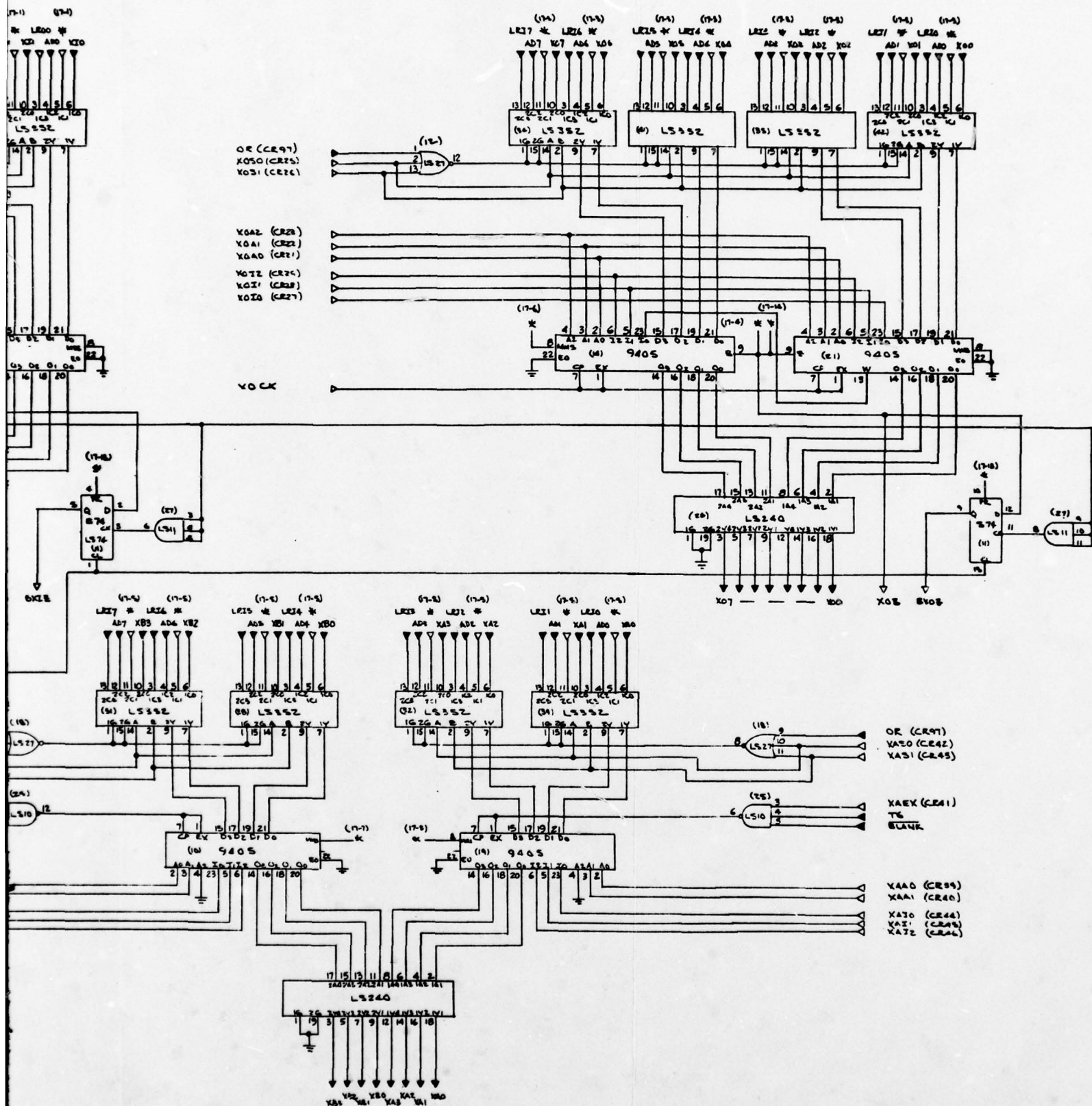


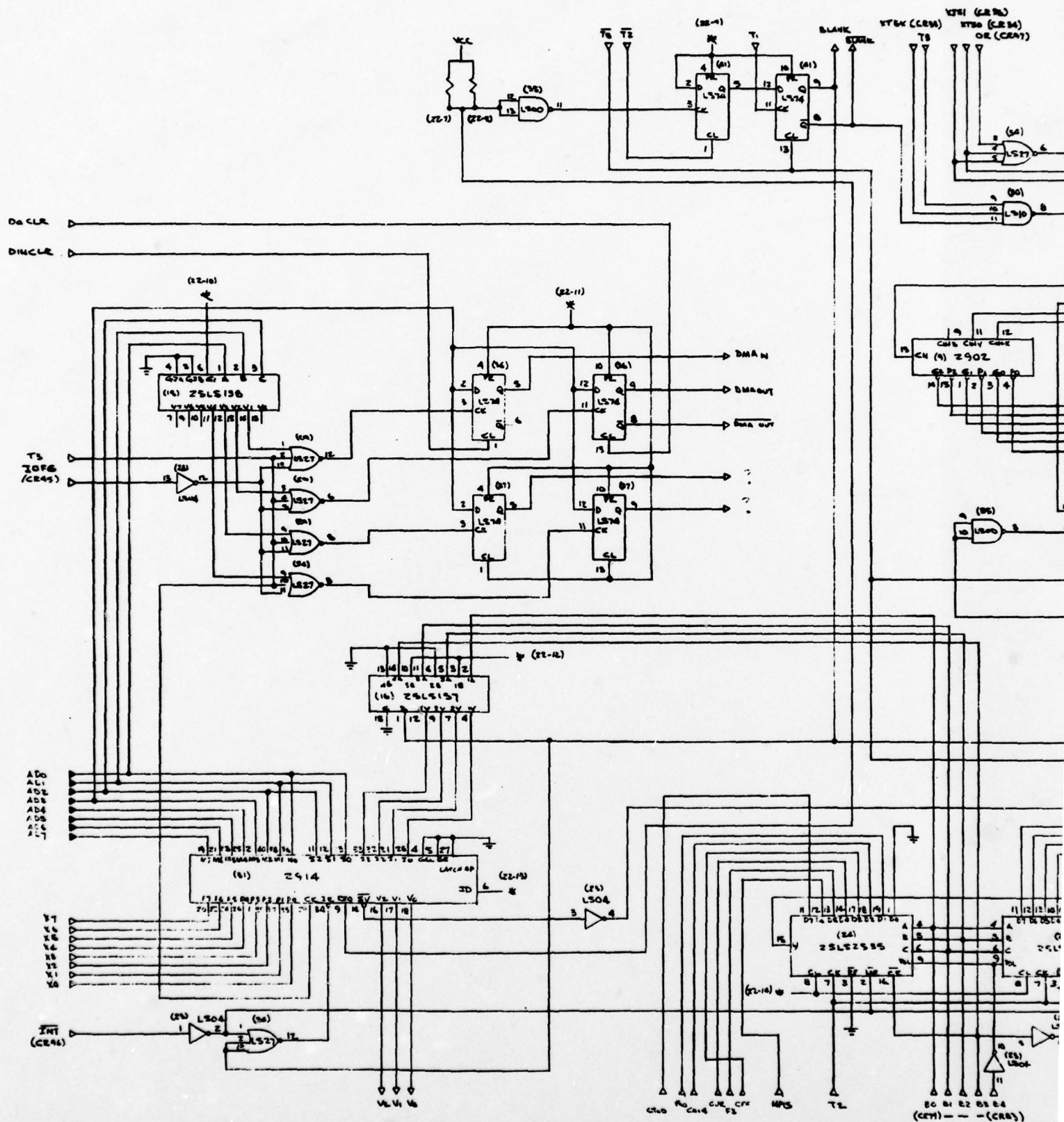


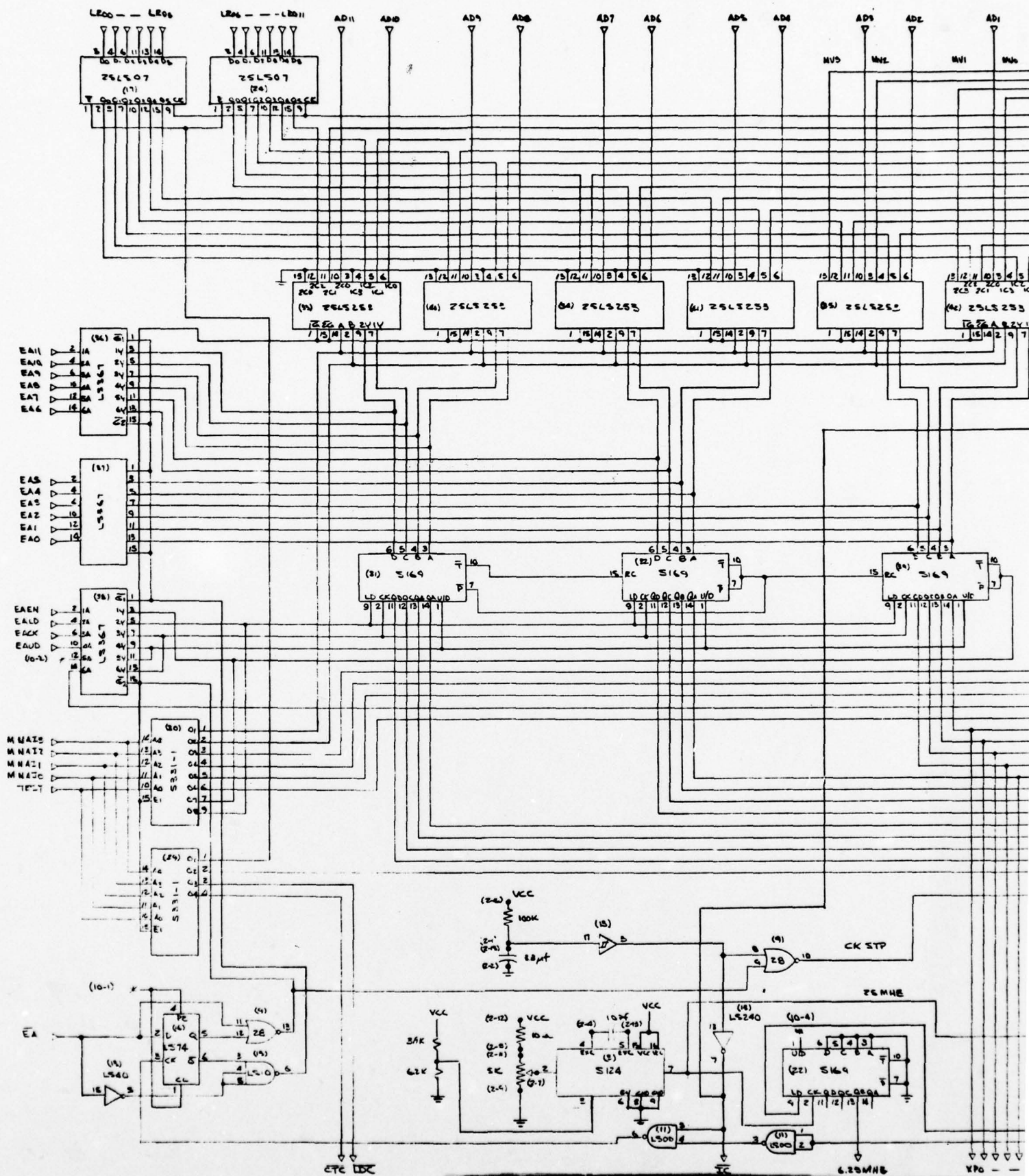
MSP
CPU
7/6/77

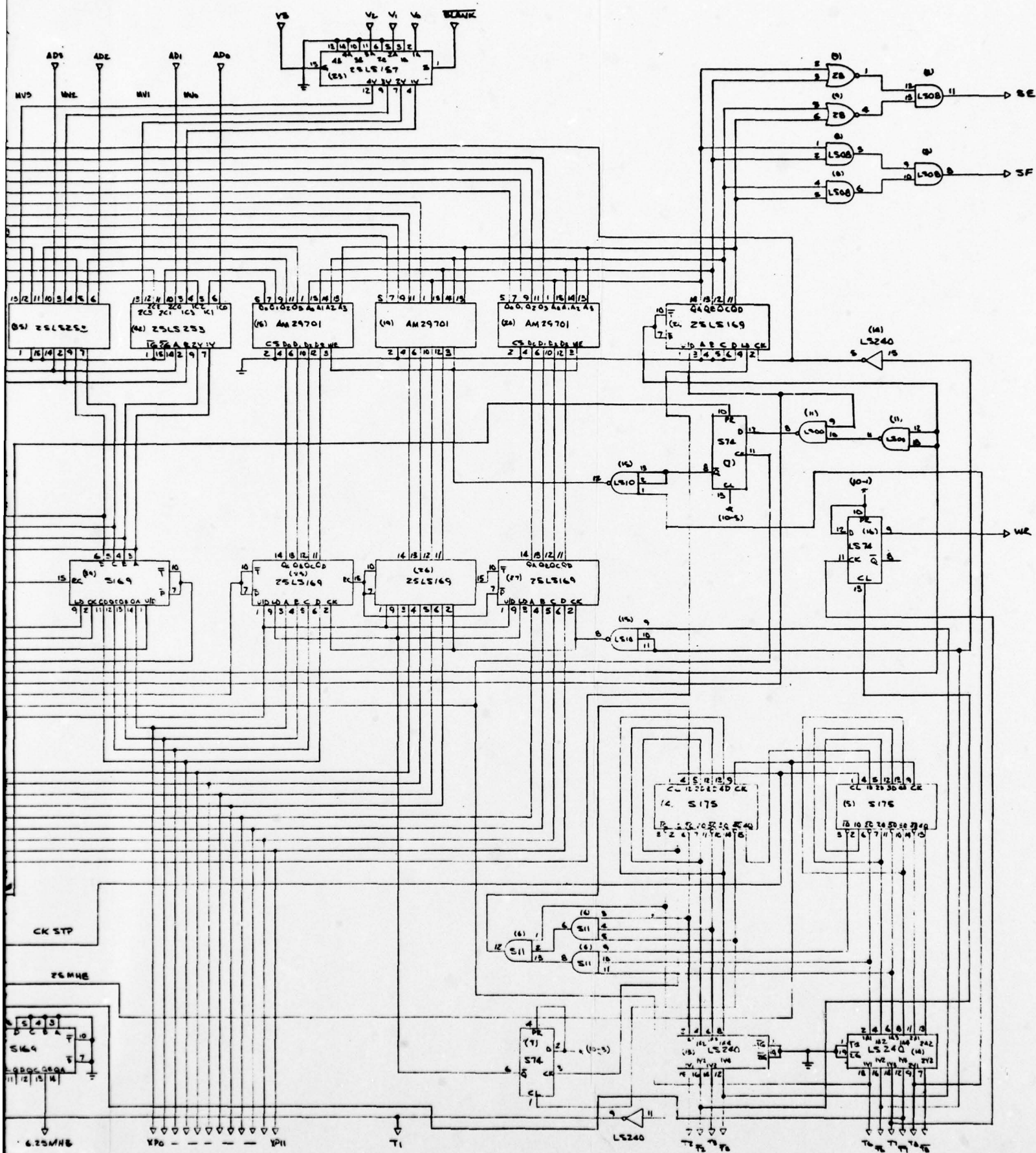
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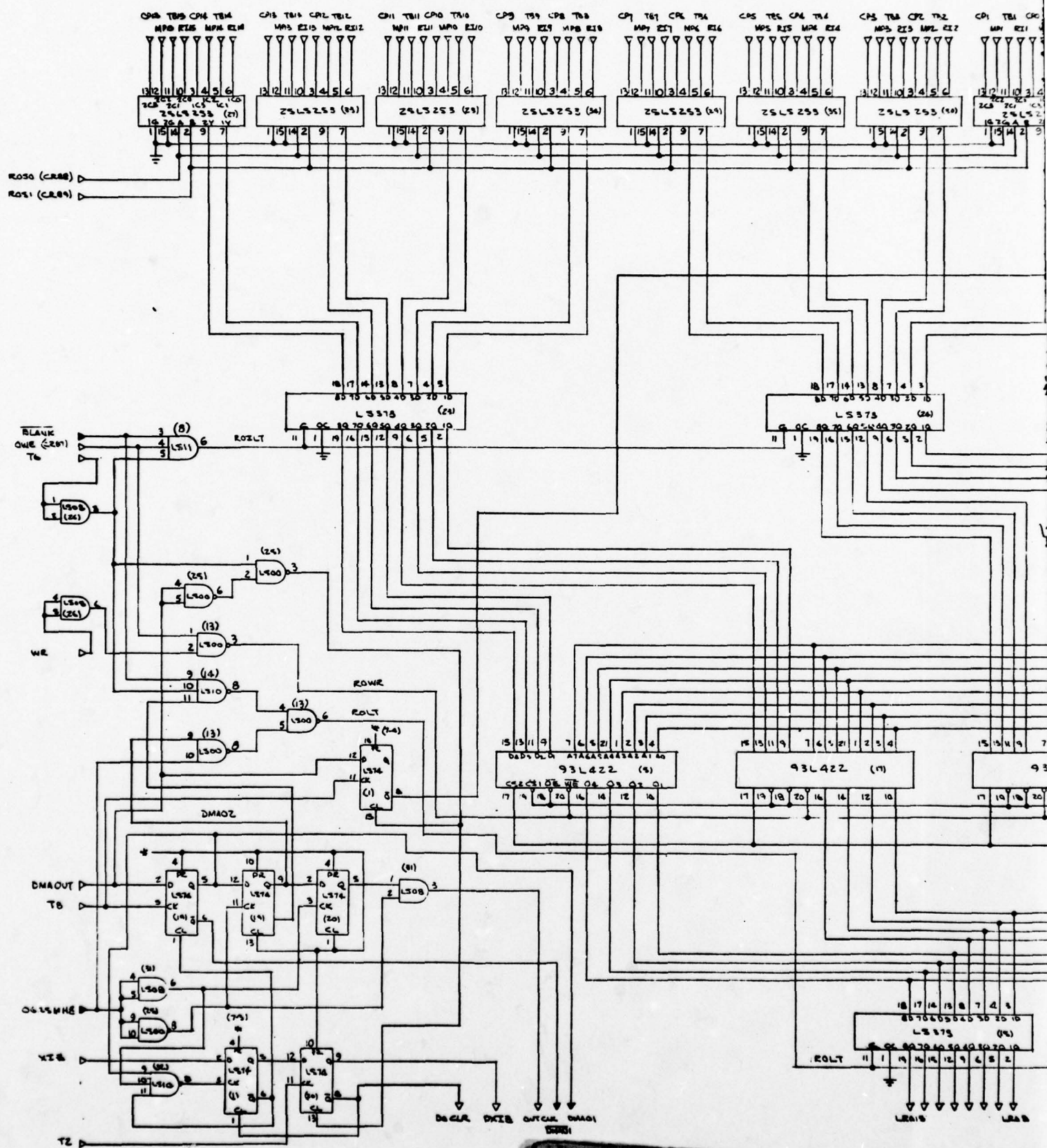




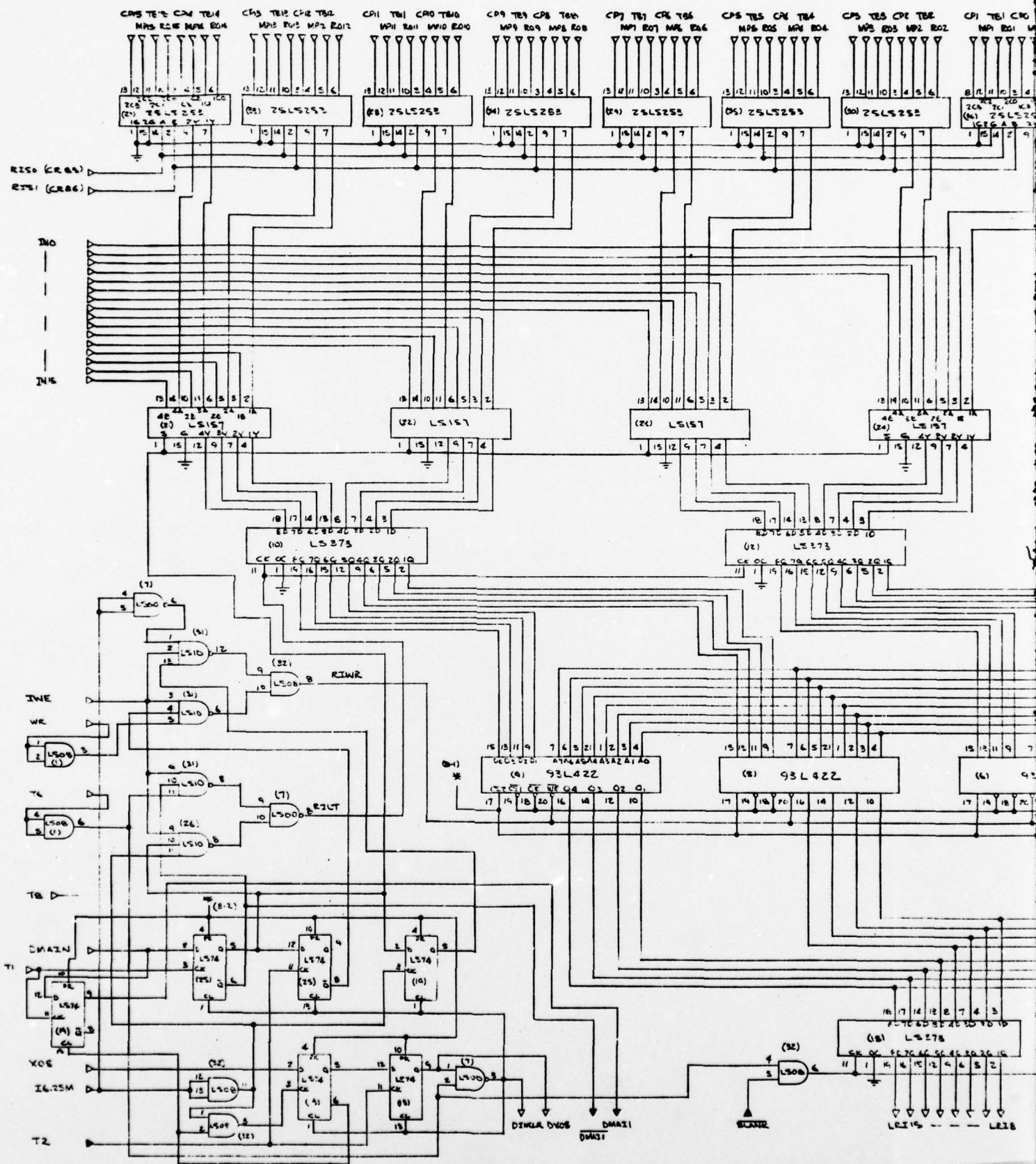




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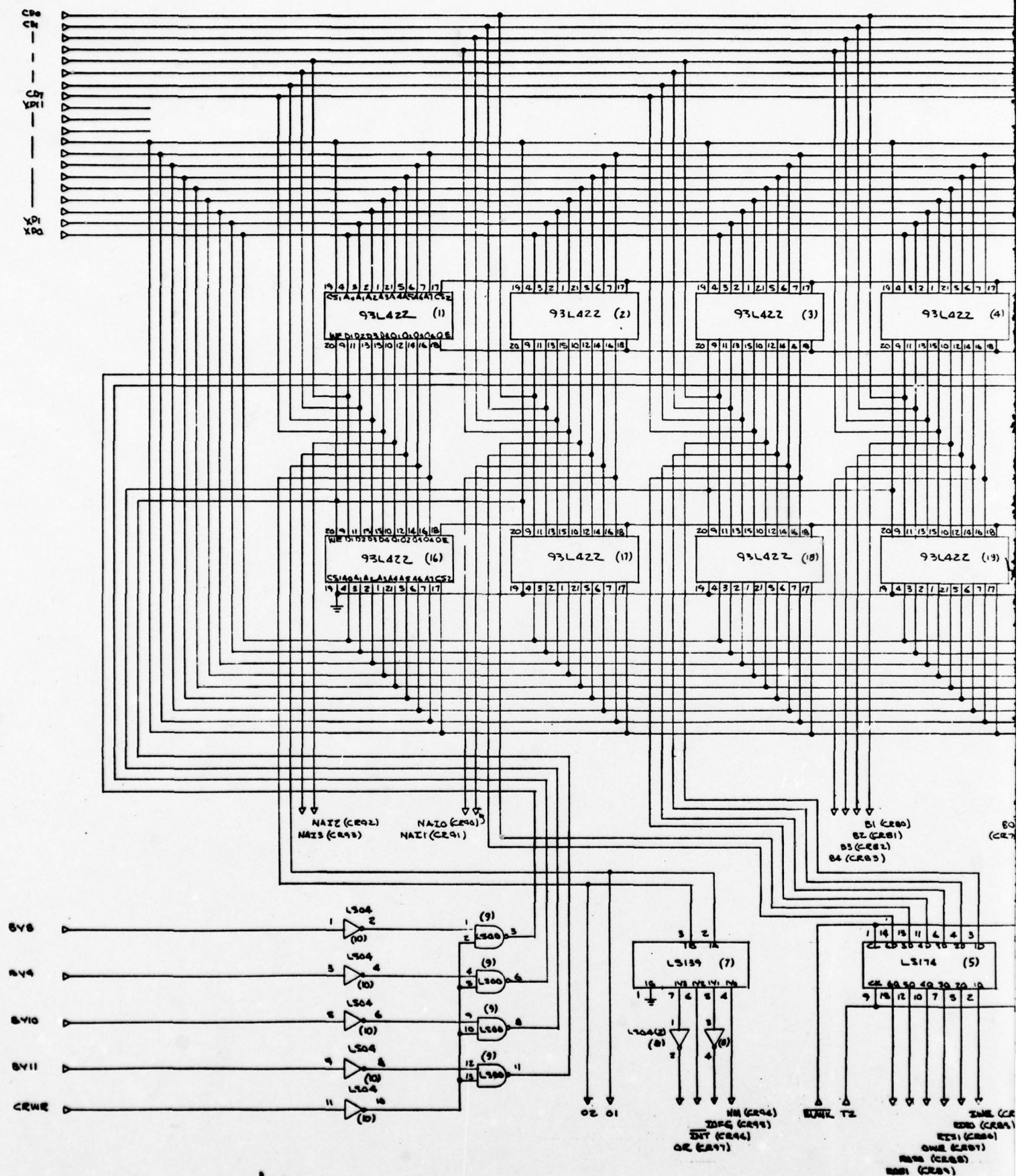


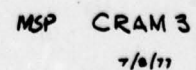
MSP OUTPUT RAM
7/8/77

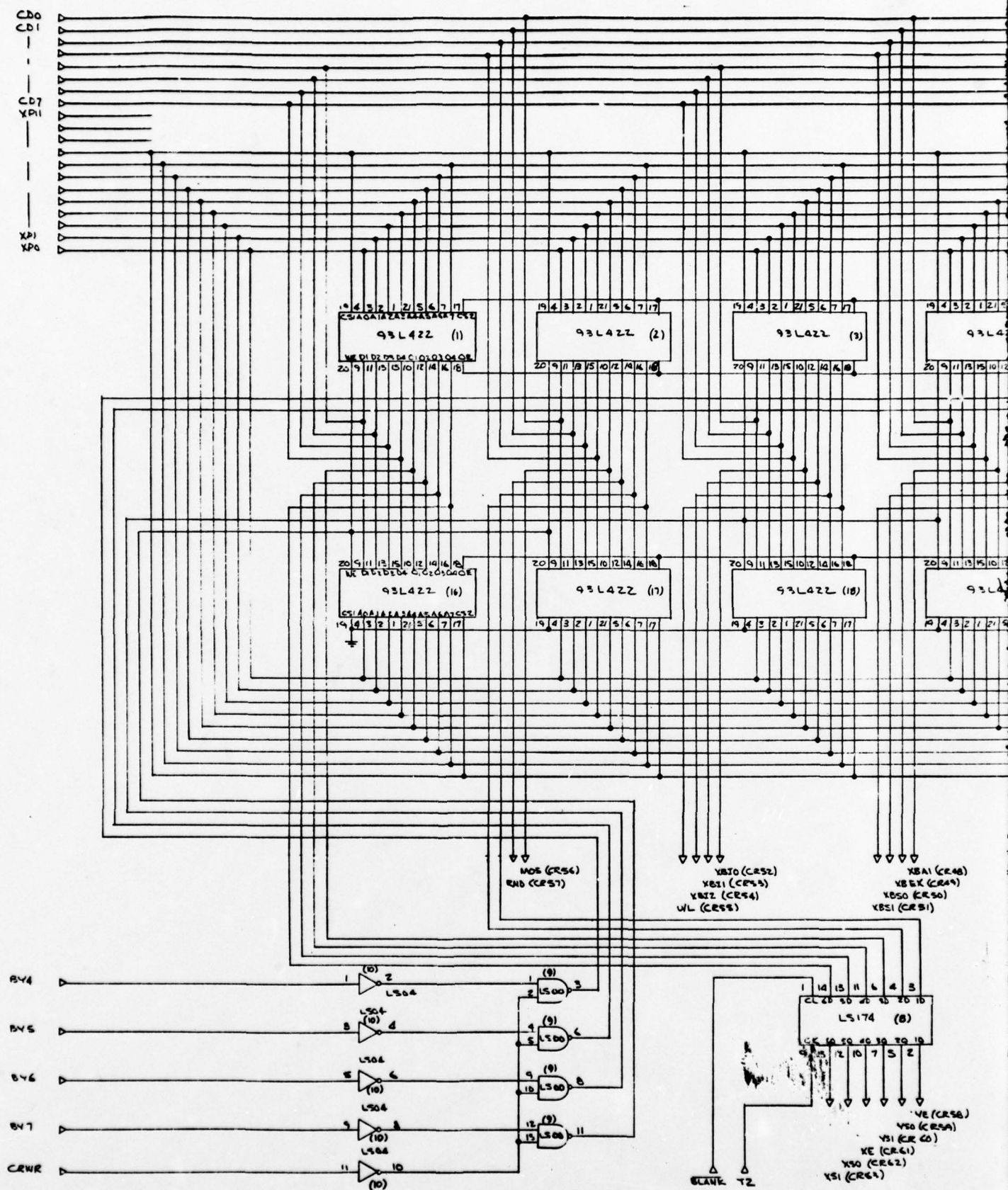


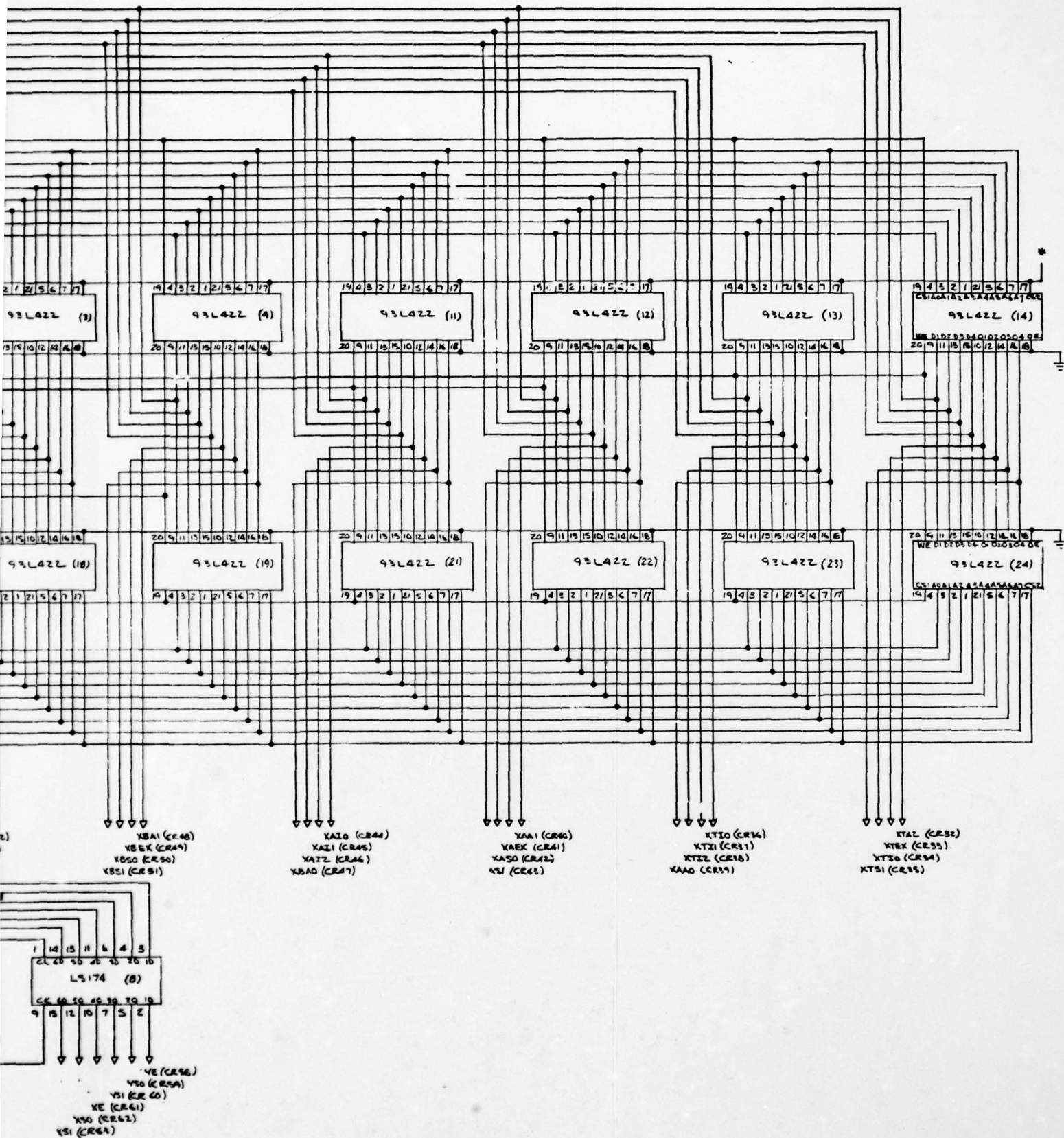


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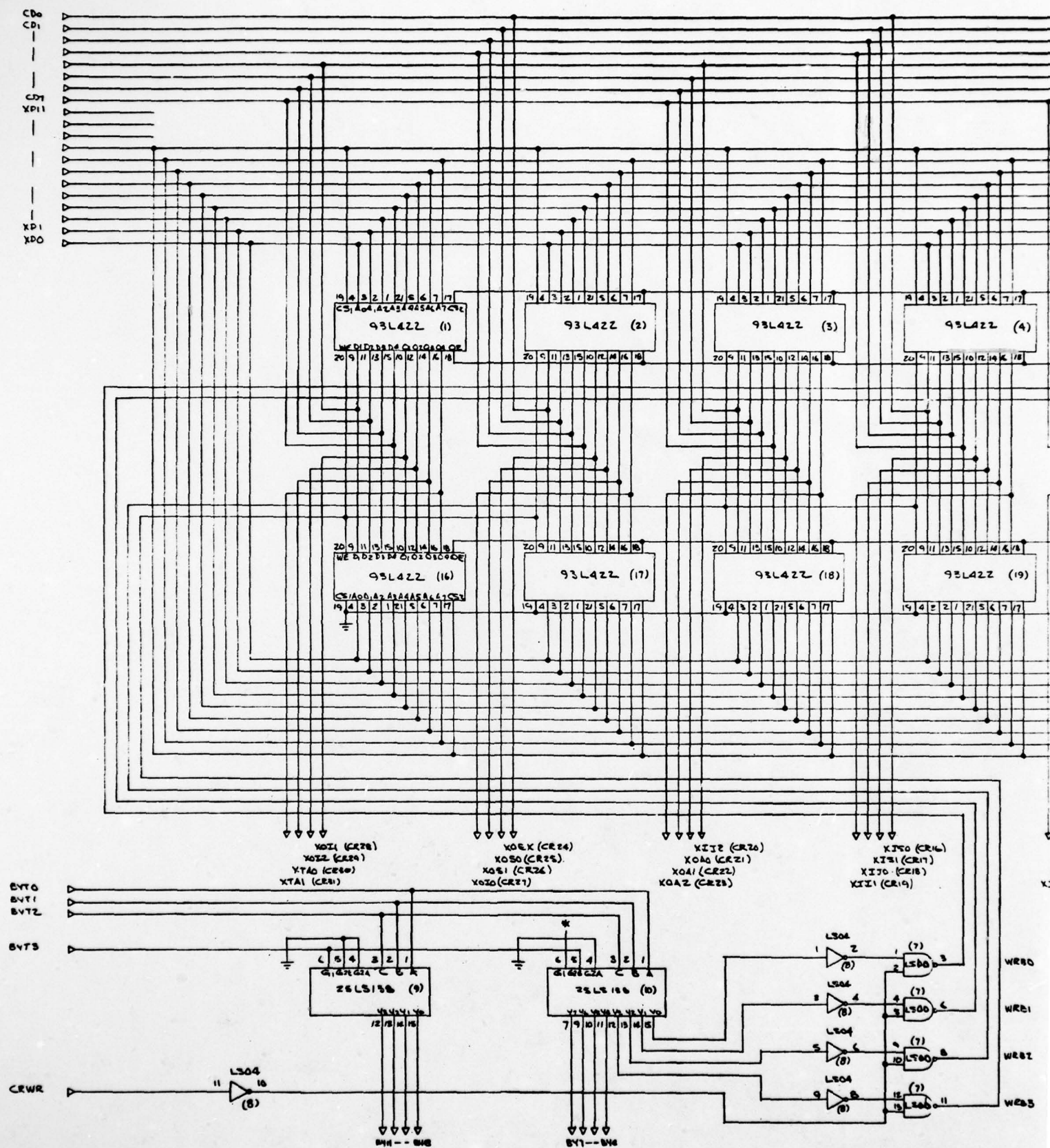


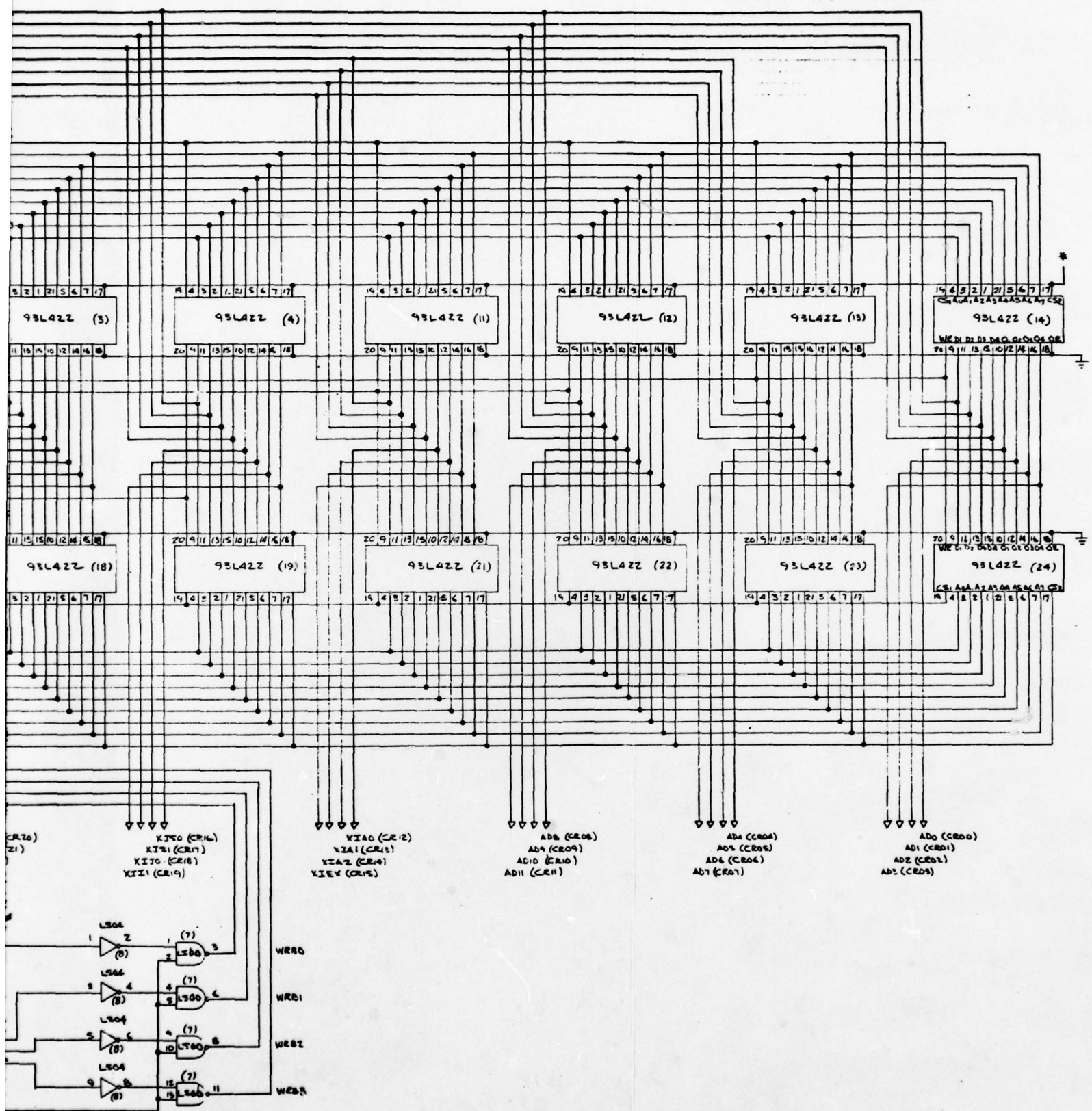




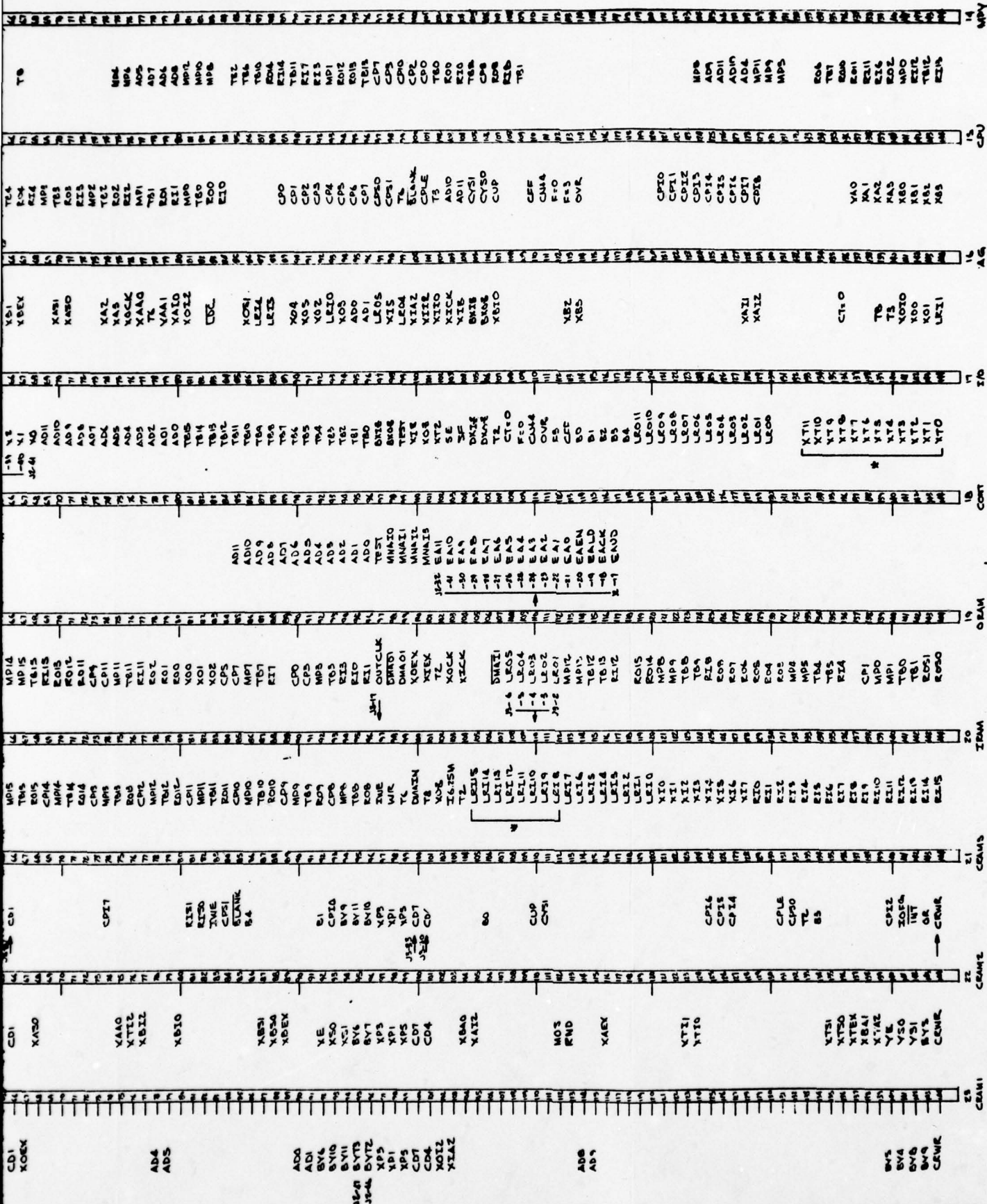
MSI CRAM 2
7/8/77

2





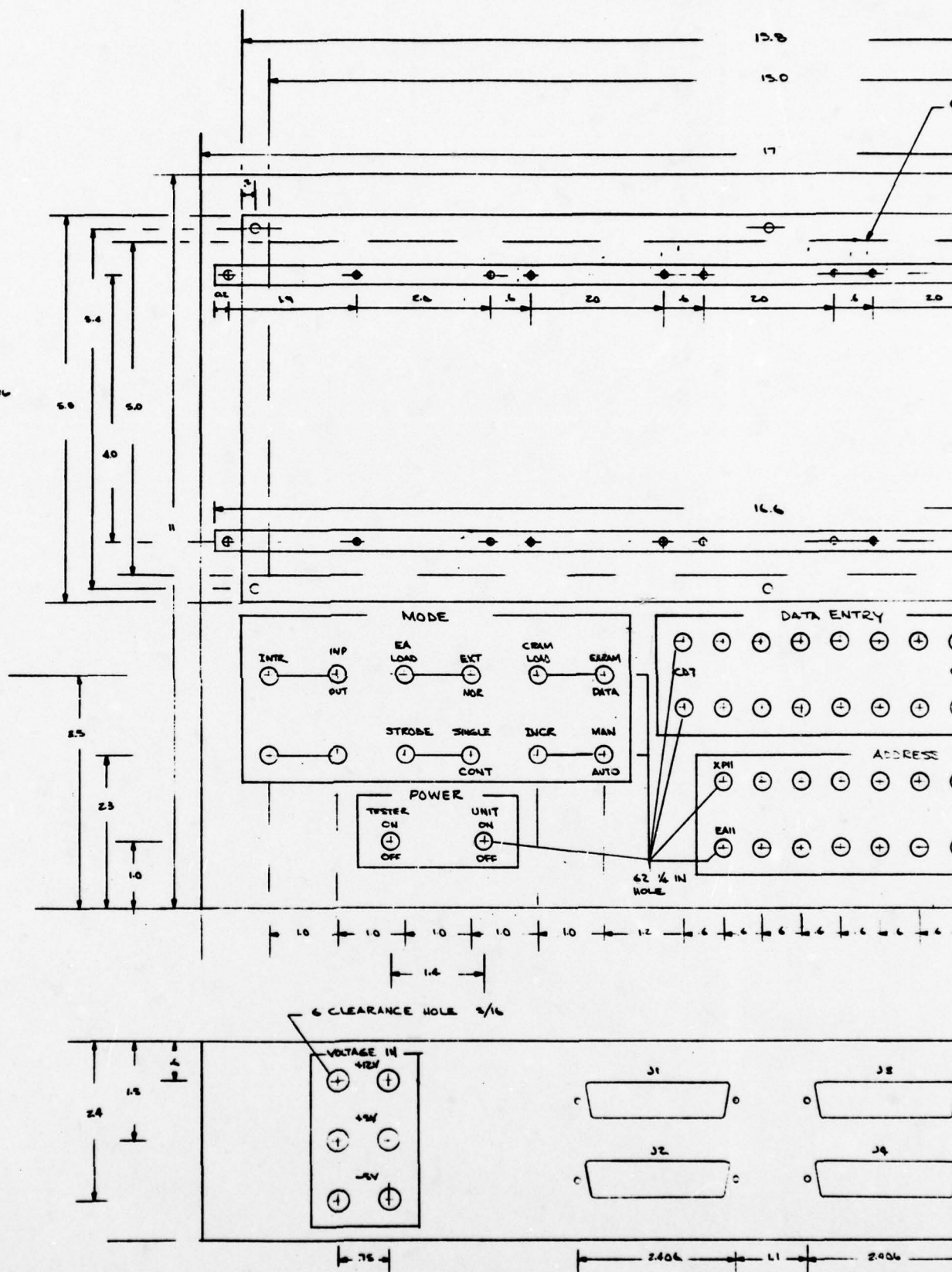
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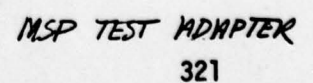


MSP INTERCONNECTION :
BACK PLANE

2

6 CUT OUT 80 PIN CONN.
 1 CUT OUT 15X5
 1 COVER 18.8X5.8-THICK 1/16
 2 STRIPS 16.6X.8
 6 MACHINE SCREW





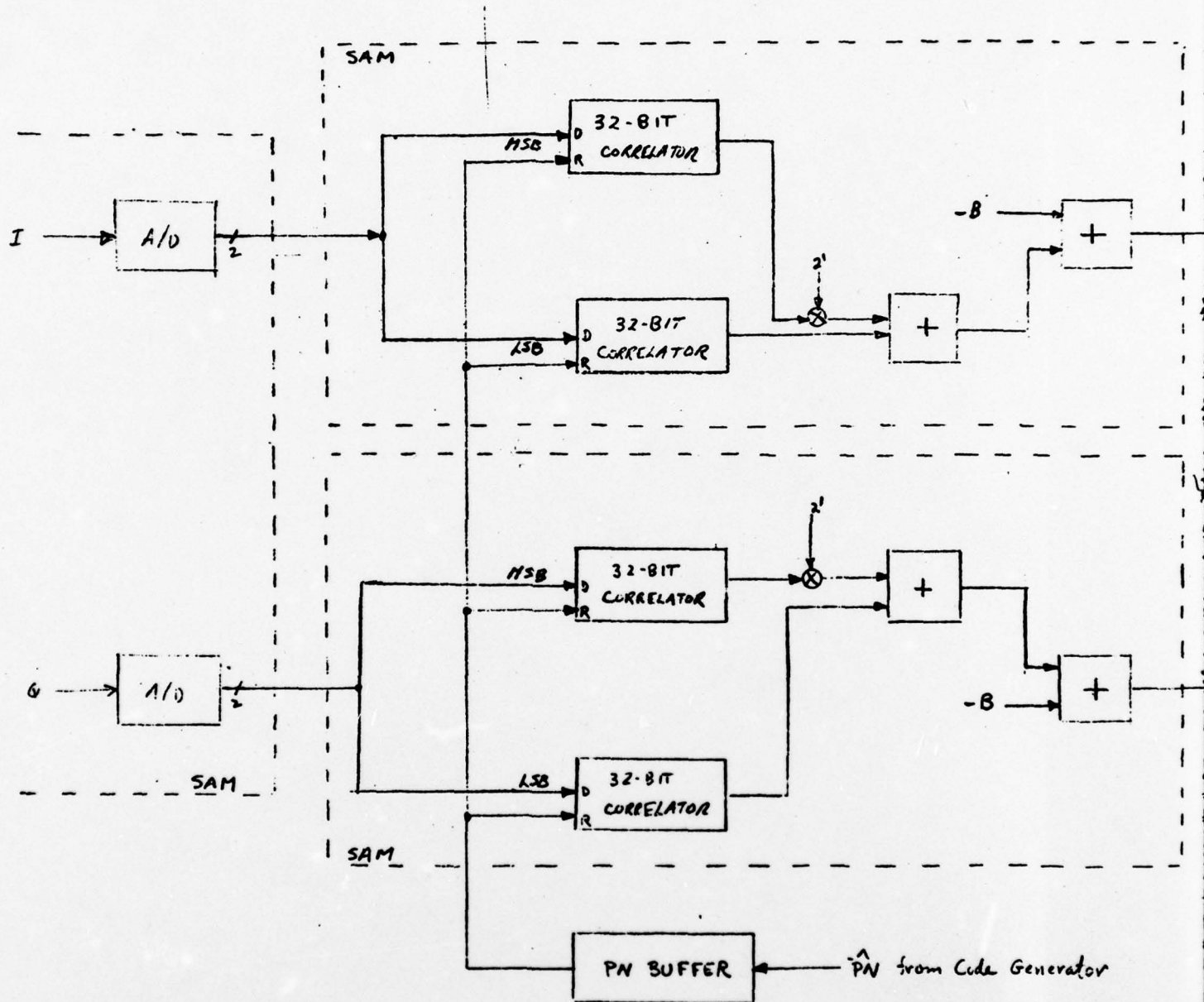
APPENDIX H

PRE-PROCESSING AND CORRELATION

H.1 Overview

This report deals with the conceptual design of the special purpose digital hardware, consisting of the correlator module, the special purpose processor (preprocessor), the code generator, and the controller. The controller generates timing and control signals for the other three units, while the code generator is an essentially independent module which generates the local estimate of the transmitted PN code. A block diagram of the correlator/preprocessor as they are currently envisioned is shown in Figure H-1. (The A/D converters are not included.) The design shown is oriented principally toward the implementation of a GPS receiver, and it is applicable to the generic PSK waveform with parallel acquisition. The 2-bit outputs from the I and Q A/D converters are correlated against the reference PN waveform by the TRW 32-bit fast parallel correlators (32-DOC). The reference is burst loaded every 32 sample times and then is allowed to remain stationary so that in effect correlations are computed for 32 relative phases of reference and data. Only 16 of these phases are utilized due to hardware considerations (see below). During acquisition the 16 phases may be considered simultaneously, thus allowing a factor of 16 reduction in acquisition time. During tracking, 3 of the 16 phases are used to provide the Early, Late, and Punctual estimates for code tracking and data demodulation. Since only 16 estimates are used, the PN reference may be loaded over a half cycle of the correlator (32 sample times = 1 cycle), thus lowering the speed requirements.

The correlation values for each bit are weighted and summed, and the offset binary bias is subtracted to produce the final I and Q correlation values. The 16 phases of correlation are then accumulated 4 times to reduce the rate of the samples into the complex multiplier. This 4 times rate reduction is necessary only for high sample rate applications such as GPS.



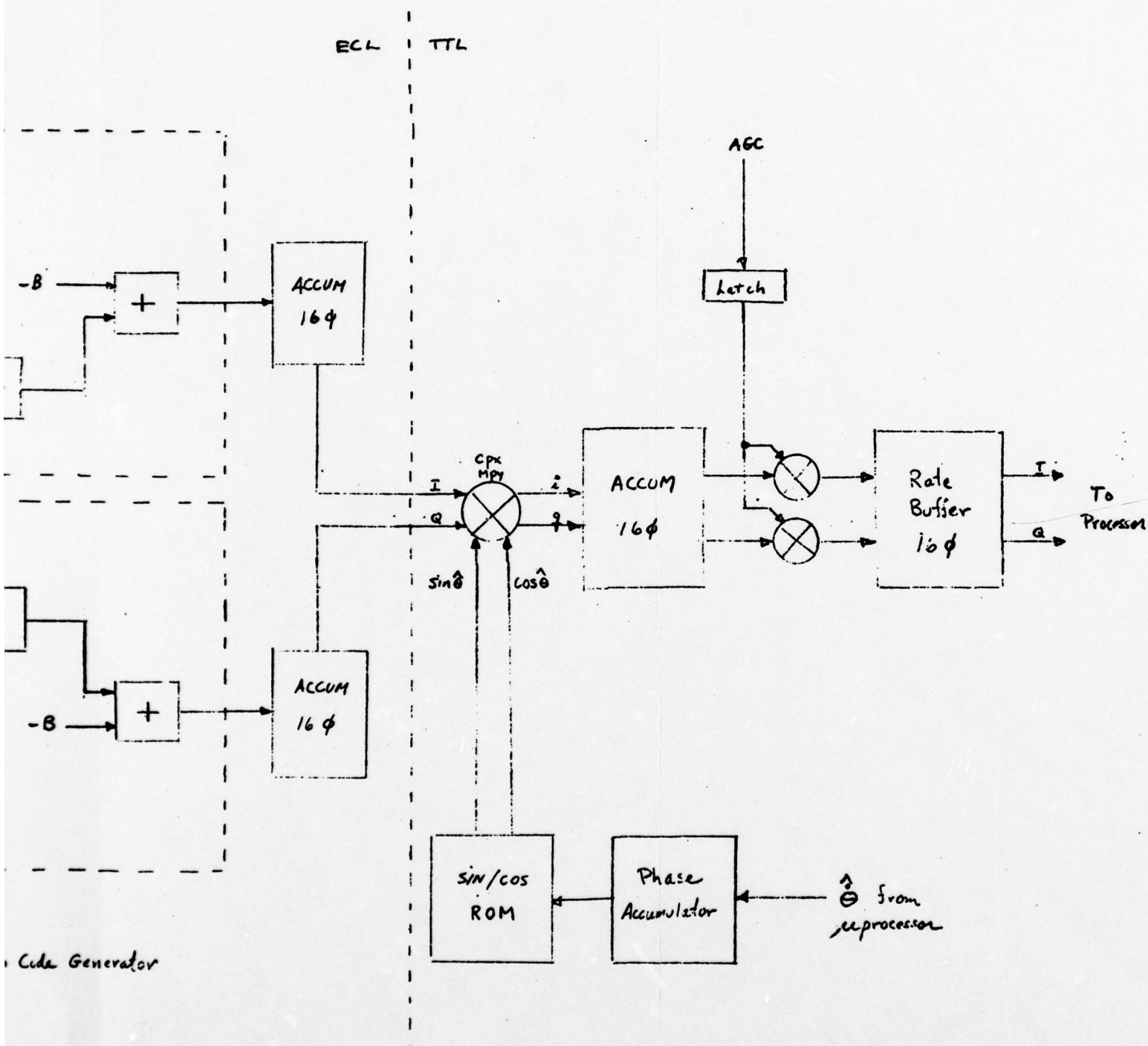


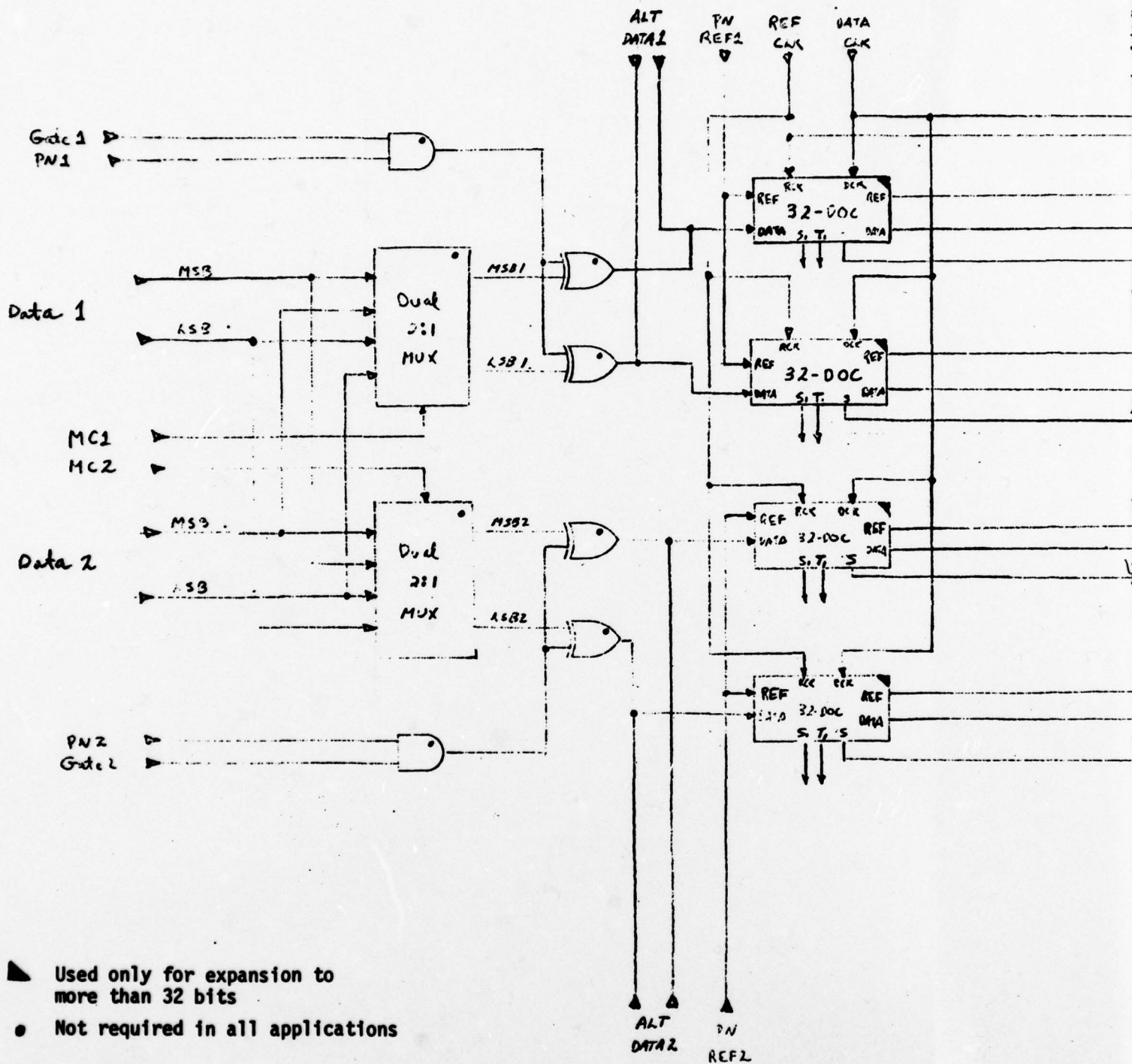
Figure H-1. GPS Correlator/Preprocessor Block Diagram

H.2 Correlator Module (SAM)

A schematic of the proposed correlator module is shown in Figure H-2. This device is intended to be a standard module (SAM). Each module will have provision for two data inputs, each consisting of two bits. The capability will exist to multiplex either input to either correlator assembly to allow for applications such as MSK demodulation. Separate PN inputs are provided for each channel, and wipeoff of the PN code may be done externally to the correlators as well. When neither multiplexing nor external wipeoff is required, these IC's may be eliminated and the alternate data inputs used.

Each SAM is configurable as a 64-bit correlator in each channel, and when this is the case, the internal summer of 32-DOC's is used to provide the expansion. Since these summers are capable only of an output of zero to 63, the addition of the extra bit must be done externally. This is performed by running the S_1 and T_1 outputs of the first correlator to a simple bias correction logic network. When the module is used as a 32-bit correlator, the first correlator in each channel may be removed along with the bias correction logic. In this case the REF and DATA inputs on the missing correlators must be jumpered to the REF and DATA outputs. No additional changes are required except that the hardwired bias is a function of the correlator length (48 for 32 bits, 96 for 64 bits). If the correlators are to be expanded to lengths greater than 64 bits, external summation of the partial correlations is required.

Figure H-3 shows a preliminary schematic for 1/2 of the correlator module, although the diagram also includes the PN buffer and the 4 times rate reduction, which are not part of the SAM.



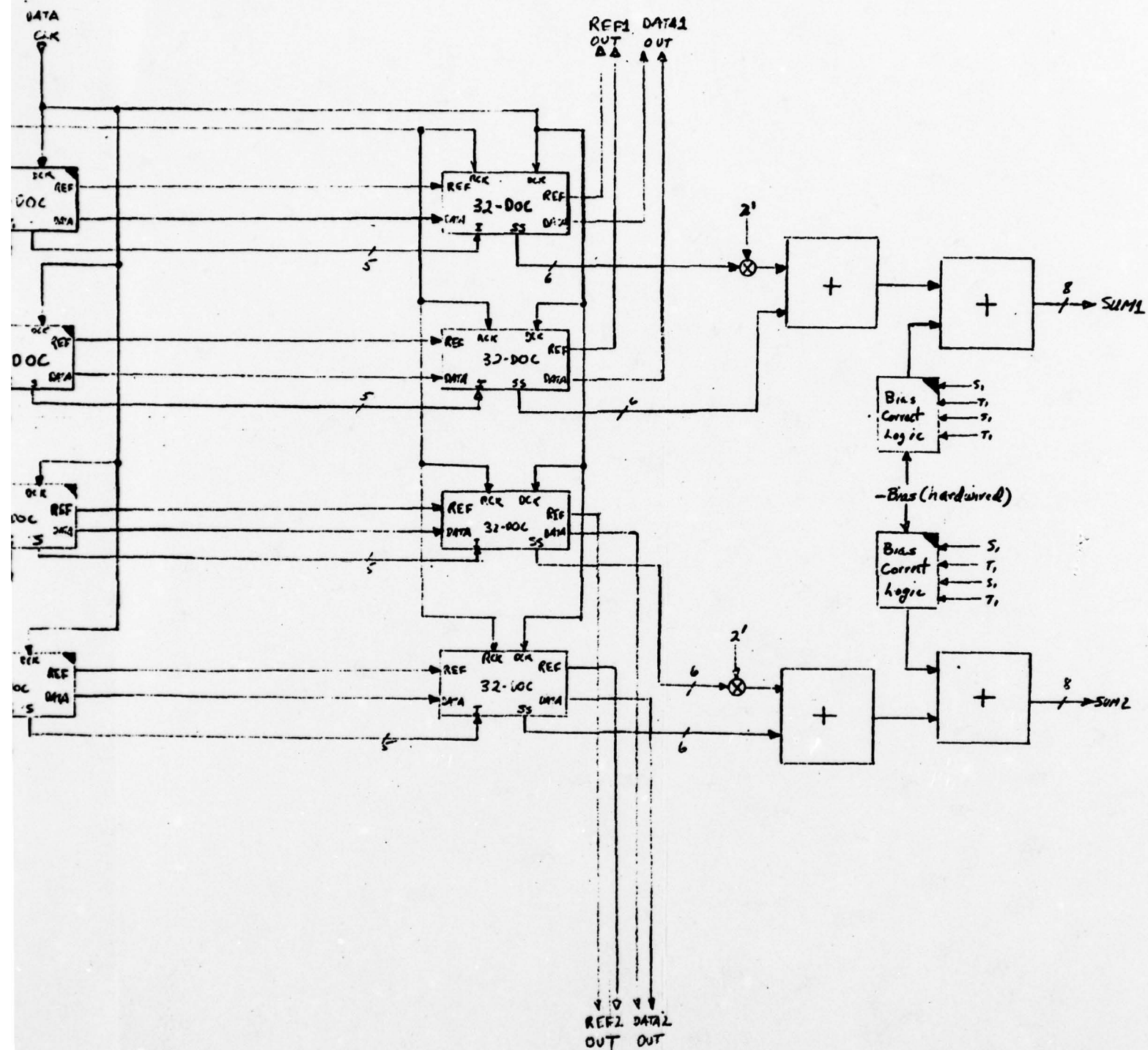
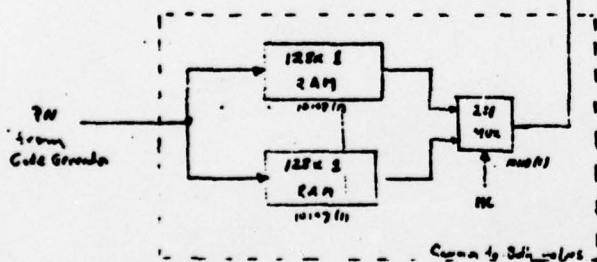
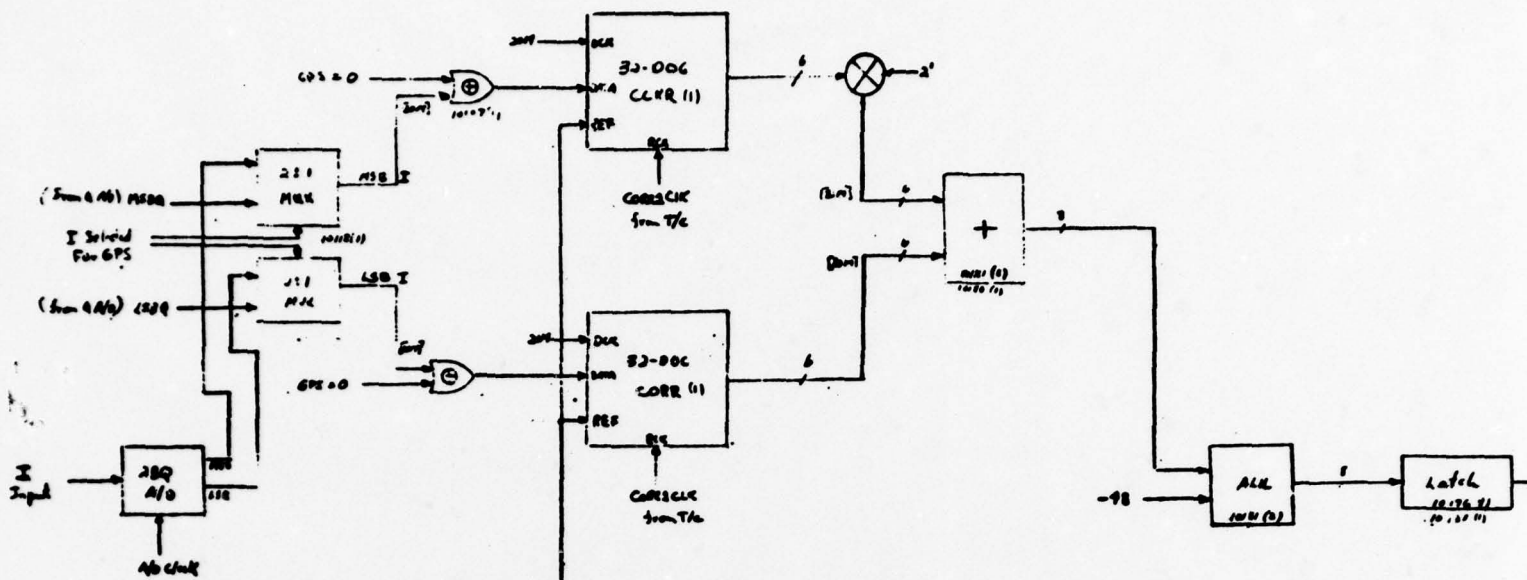


Figure H-2. Correlator SAM Block Diagram



Corridors			
26-00C	2	600	1.20
10112	1K	100	.15
10107	1	110	.11
10107	1	420	.42
28Q	1	750	.75
	6%		8.63

* Shown by the two values

Summers			
10120	1	300	.36
10191	3	400	1.20
10176	1	460	.96
10131	1	235	.24
10103	1/2	100	.05
10119	1/2	40	.07
10195	1	200	.20
	8		3.18

Corridors / A/D		70/-	7810/-
32-DOC	4	400	3.40
10112	1	100	.10
10107	1	110	.11
28Q	1	750	.75
	7		3.36

Totals: IC's 31%

Total 31% 31% Total Power 12.8 mW +20% Load = 15.6 mW

Timing for the correlators is straightforward. Figure H-4 shows the timing involved for a simplified case of a 4-bit correlator with two estimates utilized. In this diagram we have ignored the fact that there are two samples taken (in general) for each PN bit, but this does not represent a conceptual change. In the figure the data samples are taken serially in time and retain the same spatial configuration in the correlator. The data vector moves one slot each sample time. The reference vector is represented spatially on the horizontal axis and chronologically on the vertical axis. The reference must be clocked in at twice the ordinary rate during the idle time of the correlator. Thus, there must be rate-buffered storage between the code generator and the correlator. This produces a delay which must be accounted for in the overall synchronization scheme.

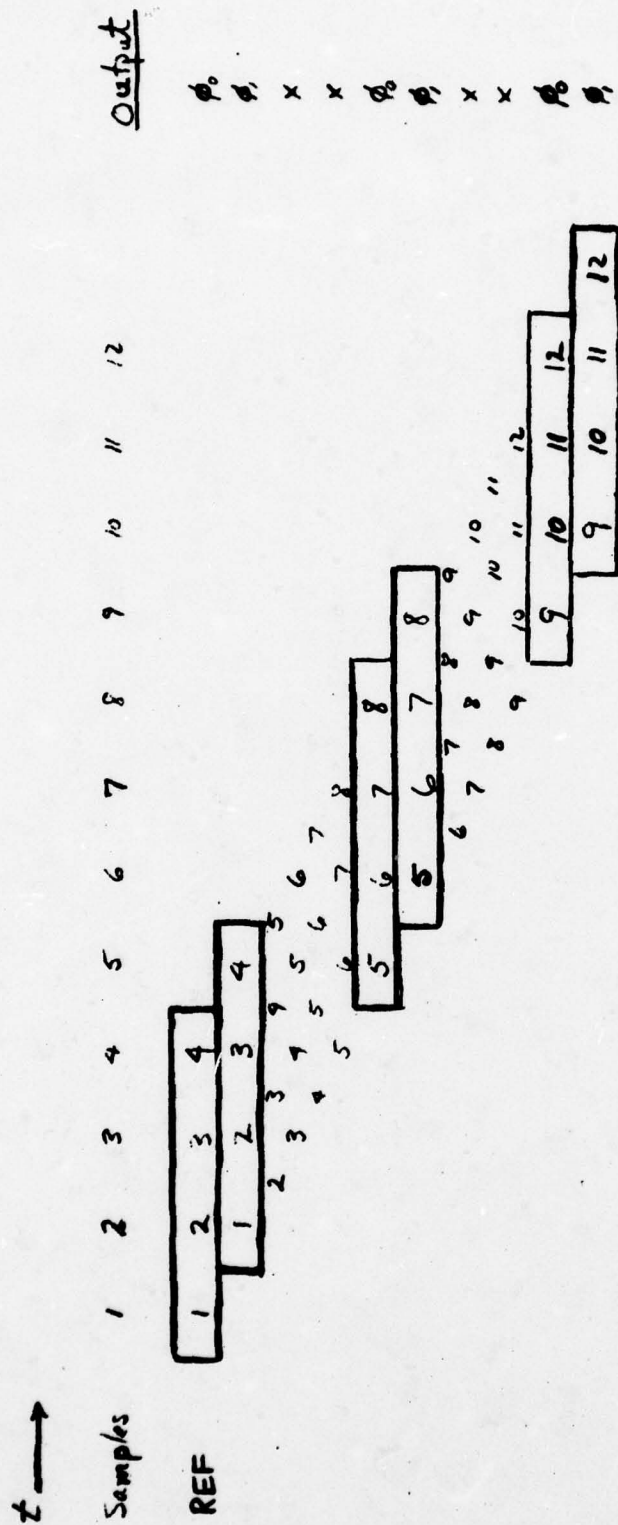


Figure H-4. Correlator Timing (4 bits, 2 ϕ)

H.3 Special Purpose Processor

The special purpose processor, or preprocessor, is shown in Figure H-5, except for the 4 times rate reduction which was shown in Figure H-3. The NCO is a standard design with the sine and cos values consisting of 4-bits including sign. The complex multiplication is done with AM2505's. Multiplication is performed at twice the incoming sample rate to produce the I and Q values. For GPS this represents a multiplication rate of 5 MHz. Timing analysis shows that timesharing of the multipliers was not possible, since even the AM2505's will not operate in an 8 x 4 mode under worst-case conditions at 10MHz. Other known multipliers will not perform the multiply function with lower power consumption, although the TRW MPY-8AJ is being considered as a means of reducing parts count.

The 16-phase accumulation following the complex multiplication is performed using RAM storage. Paralleling of two RAM assemblies (each 16 x 16) allows alternate reading and writing, thus halving the speed requirements on each chip. The S189's have a setup time of 25nsec and the LS174's have a maximum delay time of 30 nsec. At the 5MHz rate this leaves 145 nsec for the 16-bit addition. This is within the worst-case specifications of the LS283's.

The AGC multiplier is implemented with the LS261 multipliers (4 x 2) and an adder. The AGC value (assumed 3 bits) is separated into two MSB's and the LSB. The LSB gates the incoming word and the two MSB's multiply the word. The results are added to produce the final result. Timing analysis of this circuit is not complete. An output latch is probably required.

<u>Cp. Mp.</u>			
AN2505	8	450	3600
LS175	2	45	90
LS283	2	95	190
	<u>12</u>		<u>3880</u>

<u>First Accum</u>			
LS283	1	95	95
LS175	8	375	3000
LS174	3	65	195
	<u>12</u>		<u>3590</u>

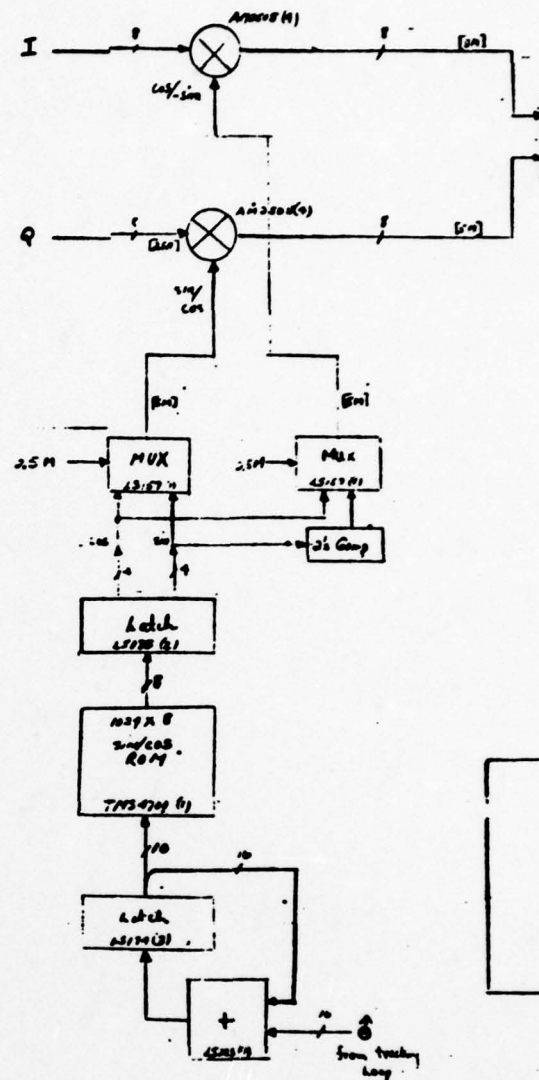
<u>Acc. Mp.</u>			
LS281	3	110	330
LS283	3	95	285
LS08	3	20	60
	<u>9</u>		<u>675</u>

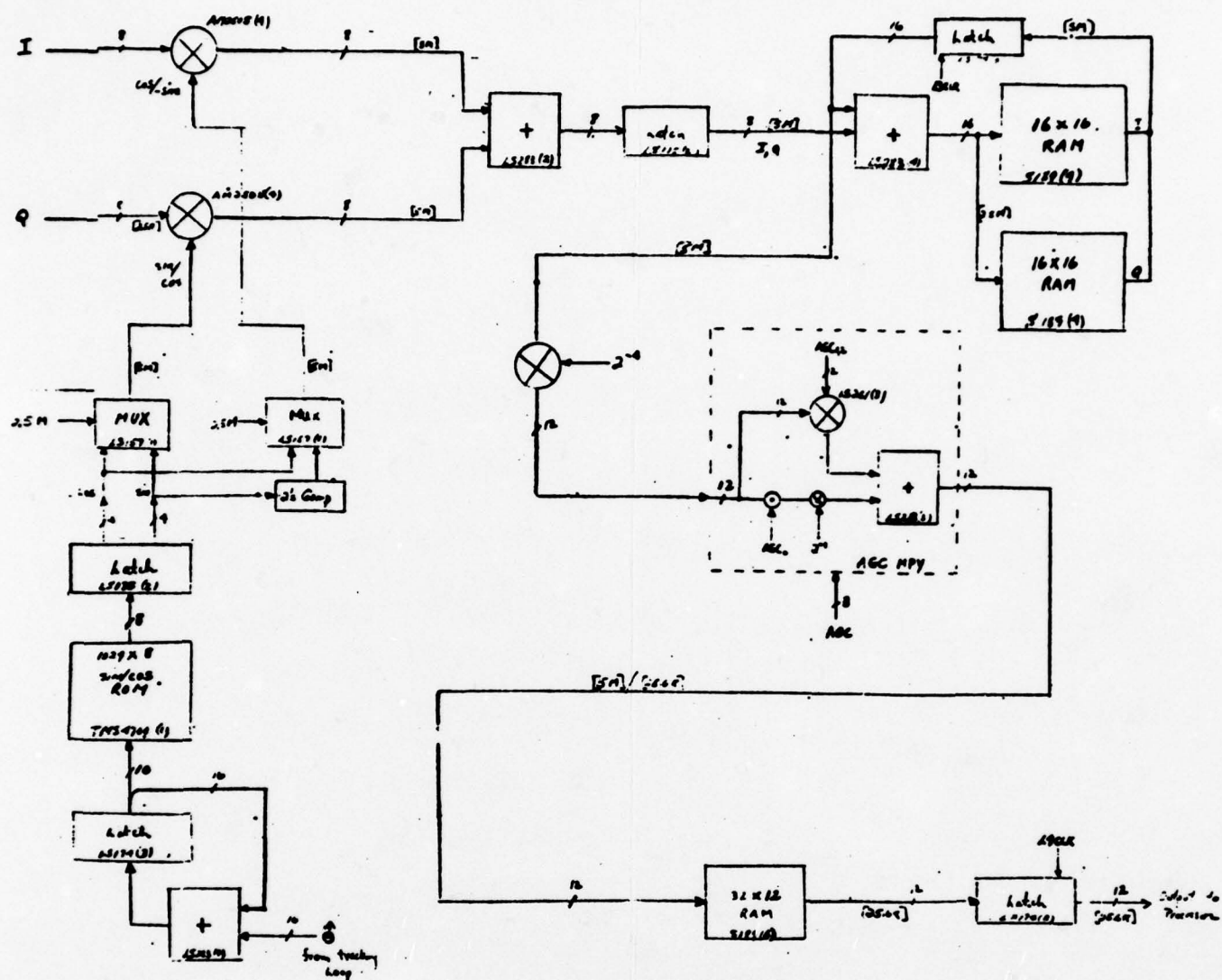
<u>NCO</u>			
LS174	3	65	195
LS283	4	95	380
TPS4700	1	310	310
LS175	2	45	90
LS157	2	50	100
LS283	1	95	95
LS176	1	30	30
	<u>17</u>		<u>1200</u>

<u>Rate. Outlin. / Latch</u>			
LS174	2	65	130
LS189	6	375	2250
	<u>8</u>		<u>2380</u>

Total Ixk : 58

Total Power : 116.8 w





3	65	195
4	95	380
1	310	310
2	45	90
2	50	100
1	95	95
1	50	50
<u>17</u>		<u>1200</u>

2	65	130
6	375	2250
<u>8</u>		<u>2380</u>

Figure H-5. GPS Preprocessor

2

The rate buffering is performed by bursting the 16 I and Q pairs into a RAM at the end of the accumulation time and then reading out at the lower output rate. The advantage of this method is that the read in is in order and is independent of the accumulation time. The RAM storage could be saved by selectively latching the required outputs in order from the AGC multiplier and zeroing the accumulator RAM in the proper location. This method breaks down, however, for short accumulation periods (less than 32 cycles) because more than one word must be read out per accumulator cycle and the output order would have to be scrambled. Saving the RAM storage does not seem to be critical, since it requires only 2.25 w., but further consideration will be given to this circuit. High-speed FIFO's will be considered.

Returning to the 4 times rate reduction in Figure 3, we see that this is also implemented with RAM accumulators but is fully ECL. The speed requirements for GPS are too great to implement this section in TTL logic, since the input rate is 20 MHz worst-case. This could be slowed to 10MHz by sliding the reference in the correlators at half the sample rate, but this would require doubling the number of correlators in order to perform loading. This effect coupled with a minimal power savings of TTL vs ECL makes ECL preferable. Even ECL circuits, however, are not fast enough to permit both reading and writing in one cycle at 20MHz. The combination of setup, addition and latch times is 31 nsec worst case. Thus, alternating RAM's again is required even though in this case it implies a two-fold excess of storage. High-speed FIFO's would provide a speed advantage, but no circuit is known with sufficient speed to work even at 10MHz. Thought was also given to the use of high-speed ECL multipliers in the complex multipliers, thereby eliminating the need for the 4 times rate reduction, but this would require the following accumulator to be implemented in ECL. The end result is an increase in power consumption.

Timing for the 4 times rate reduction is shown in Figure H-6. In order to save further storage rate buffering is performed by direct readout at the 1/4 rate, as shown. This is straightforward but results in scrambling of the output order. This is compensated in the final rate buffering to the processor so that I,Q pairs are read out together in the proper sequence: $\phi 0I$, $\phi 0Q$, $\phi 1I$, $\phi 1Q$, $\phi 2I$, etc. This is another reason for the more flexible rate buffering scheme described above.

With the above tradeoffs in mind an attempt was made to characterize the hardware requirements vs. the number of phases computed in acquisition. Values of 1 to 32 were considered. The single-phase case represents a straight serial acquisition but still requires computation of 3 phases for Early/Punctual/Late. The 32-phase case represents the fastest acquisition but requires doubling the number of correlators, multipliers and RAM storage chips (except in the 4 times rate reduction) due to the increased speeds involved. Sixteen phases is efficient due to the general availability of 16 x 4 RAM's. The following list summarizes the parts and power requirements for the correlator and processor vs. the number of phases considered during acquisition.

<u>No. ϕ</u>	<u>IC's</u>	<u>Power (w)</u>
1	69	27
4	89	31
16	106	41
32	156	56

The 16-phase approach was selected for the baseline system as being the best tradeoff between hardware requirements and speed of acquisition.

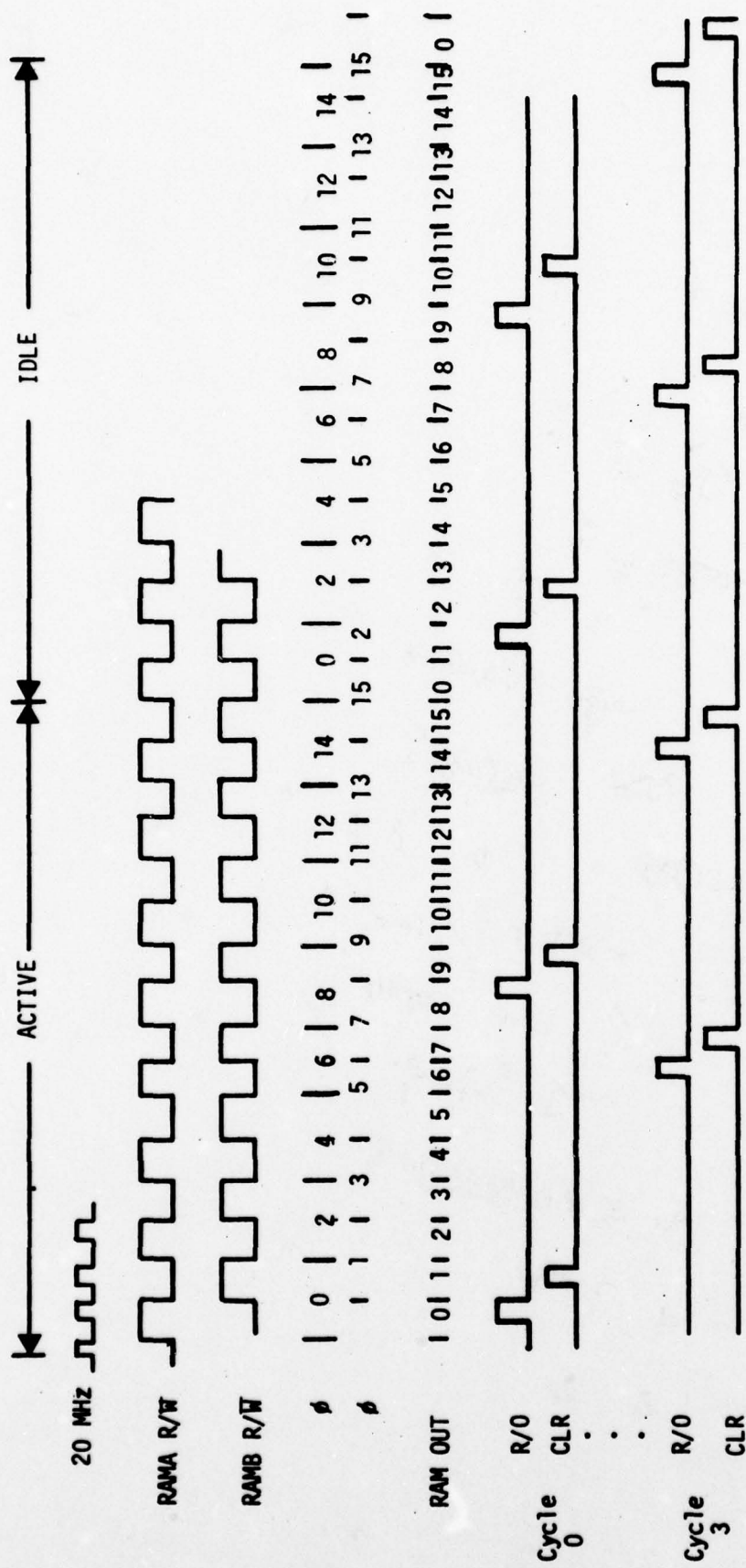
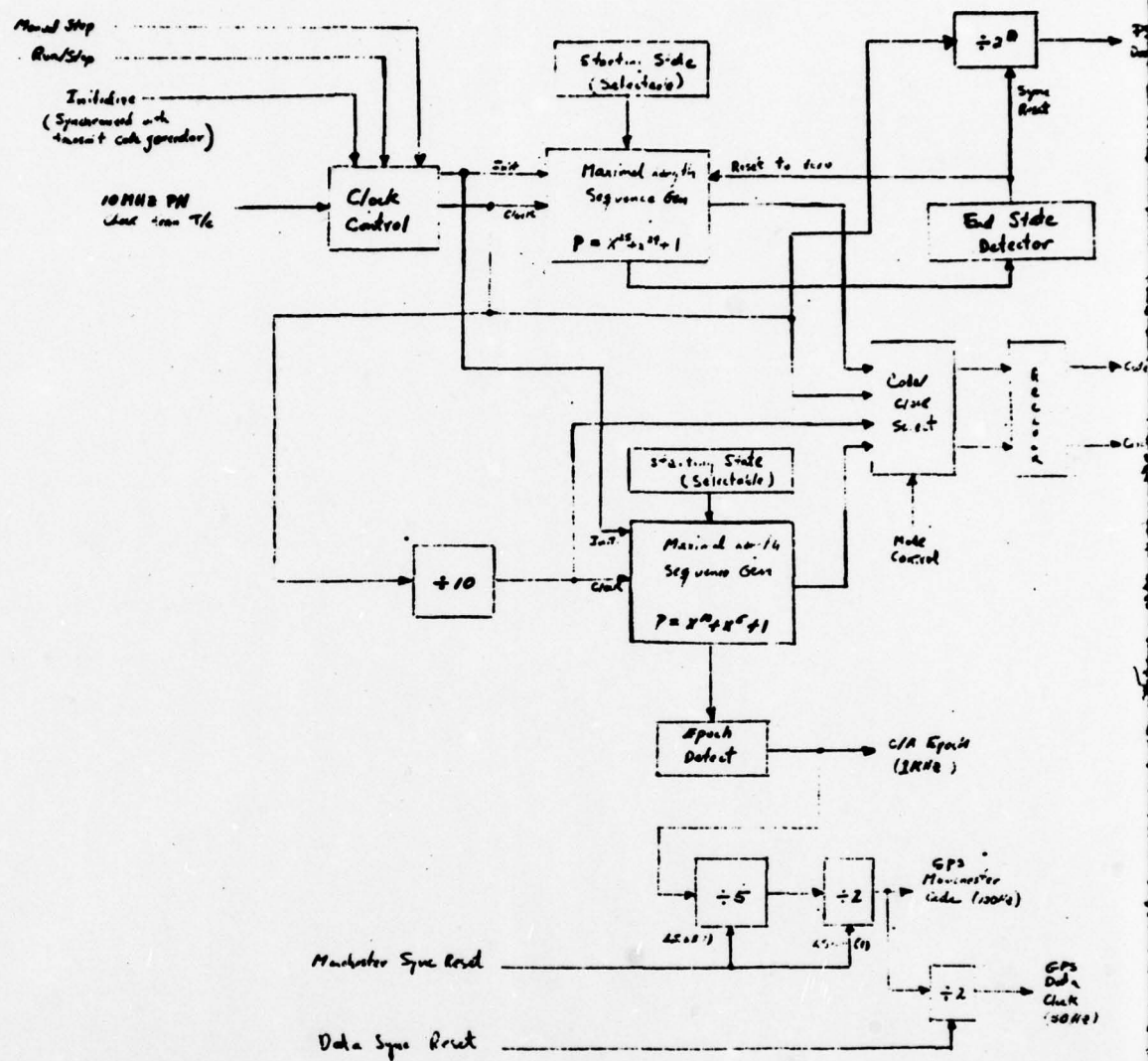


Figure H-6. Rate Reduction Timing

H.4 Code Generator

A block diagram of the demonstration PRN code generator is shown in Figure H-7. The design is aimed at GPS capabilities, although the handover feature is not included. A long or short code may be generated and acquisition of either is possible. Each code has a selectable starting state which is parallel loaded upon receipt of an initialization command. Thus, acquisition from any given offset may be performed. Data and Manchester sync are derived from the epoch of the short code for GPS as required. In the generic PSK applications the data rate is derived by a binary division of the code clock and the long code is used as the PRN sequence. Data sync is derived by resetting the binary counter with the end state pulse, which implies that the code epoch must contain an integral number of data periods. This subject is discussed further in Section VI.



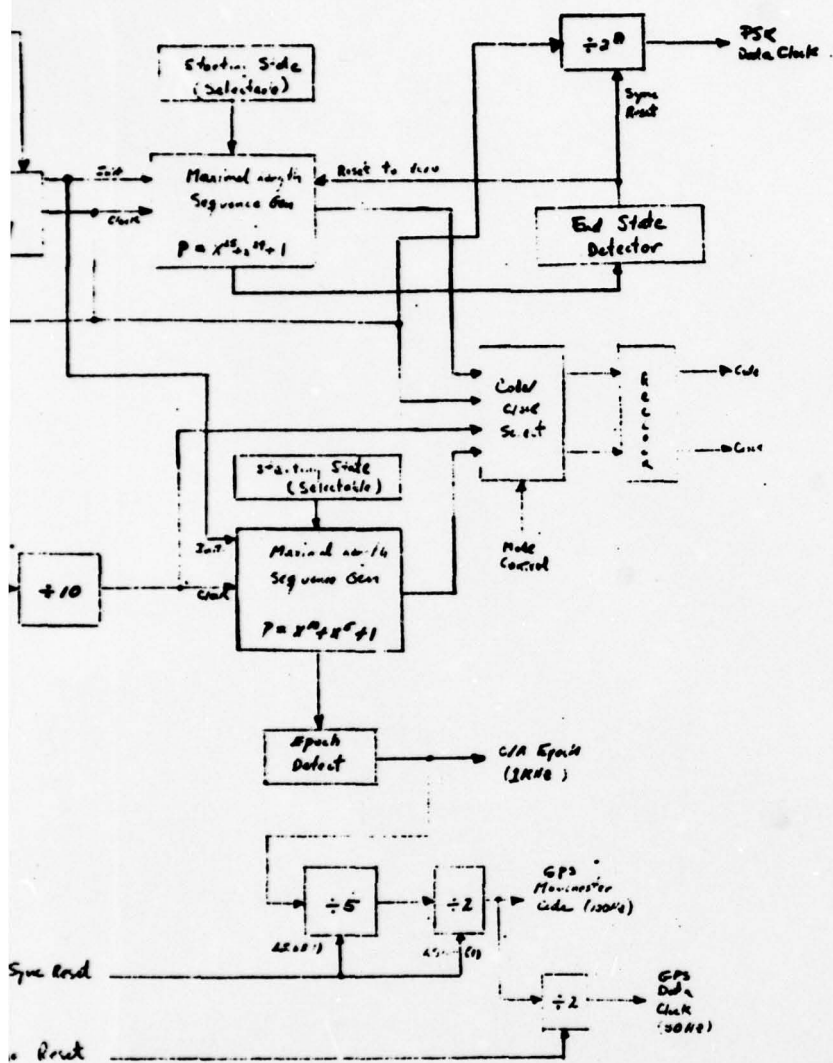


Fig. 6

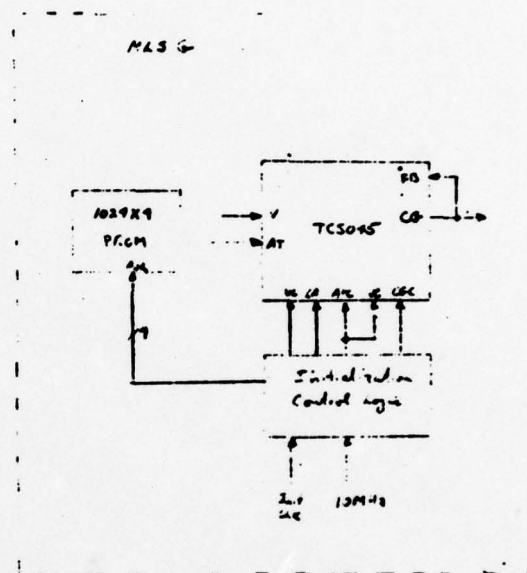


Figure H-7. Demonstration Code Generator

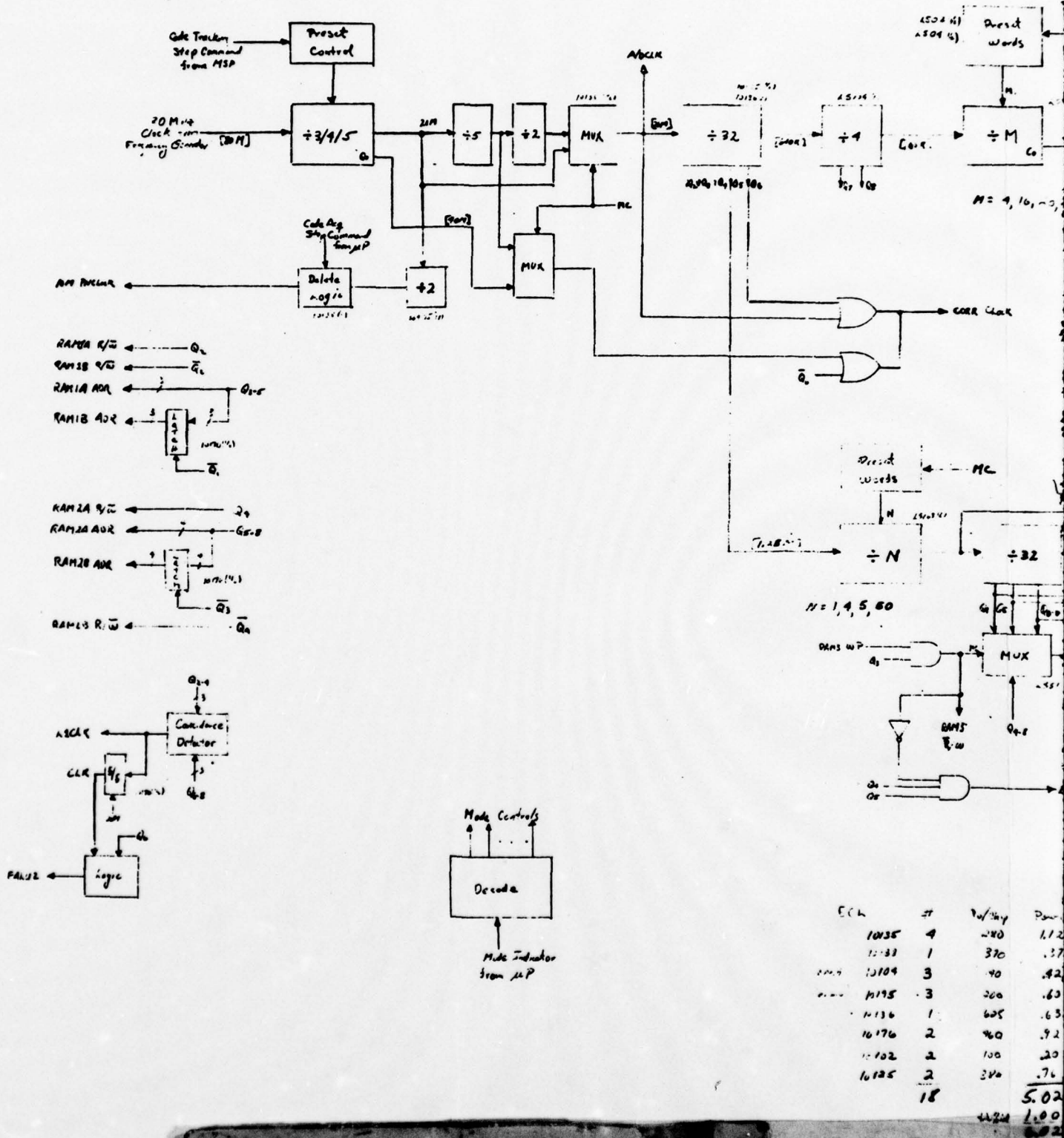
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H.5 Controller (Timing and Control)

The controller generates timing signals for the three sections mentioned previously. This module should not be construed as a system controller and is itself under control of the MSP. A block diagram of the controller is shown in Figure H-8. The controller is essentially a divider chain from which all clocks, RAM addresses, etc, are generated. The system clock runs at 8 times the PN code rate and addition and deletions are made in units of $1/8$ chip, or $1/4$ a sample period. Acquisition and tracking step commands from the MSP allow code acquisition and code/sample tracking. A mode indicator is received from the MSP which configures the controller for the various timing modes. Provision is also made for synchronization of the clocks to the data upon command from the MSP.

All Rates Approx - 10
ROM @ 8189MHz

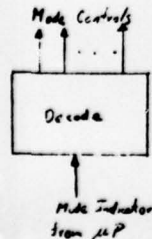
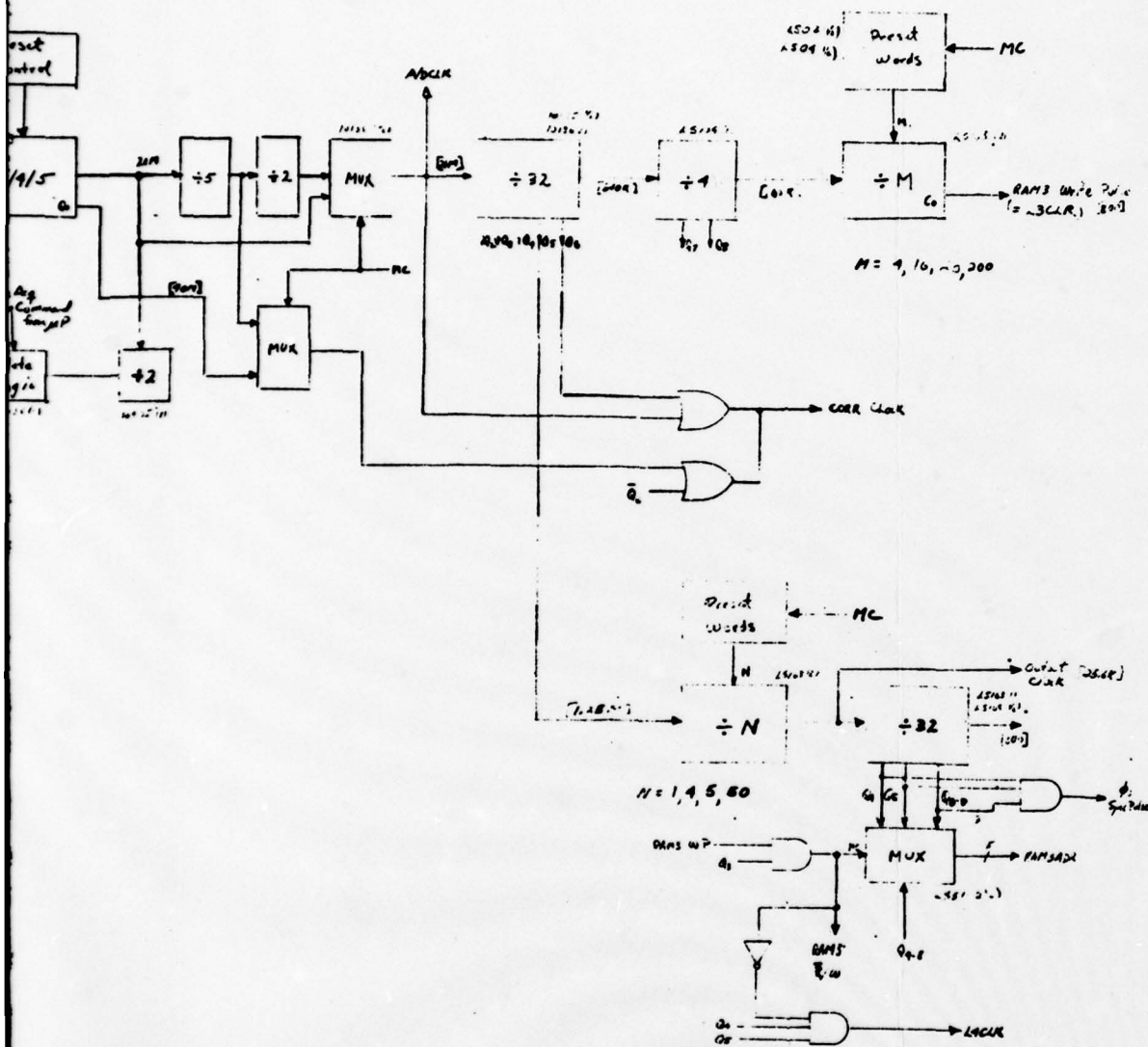
Rates shown are for Direct Acc. PCalc), Search RER



Total 28% 42

10
19MHz

For Direct Address, Search R/R



IC#	#	Vol/Temp	Power (W)	TL	Vol/Temp	Power (W)
10135	4	280	1.12	15163	5	98
10133	1	370	.37	15105	4	20
10104	3	40	.42	1500	2	8
10195	3	200	.60	1502	1	11
10136	1	605	.63	1504	3	12
10176	2	400	.92	1530	2	2
10102	2	100	.20	1551	3	6
10125	2	370	.76		20	
	18		5.02			
			1.00			
			6.02			

Figure H-8. T/C Block Diagram

Total ICs 42

Total Power 6.65 W

H.6 General PSK Applications

The hardware described above is intended to be applied to generic PSK waveforms having a ratio of PN Rate/Data Rate from 2^4 to 2^{17} in steps of powers of two only. (The GPS application does not fit this formula and is treated separately below.) The covered PN and data rates are shown in Table H-1.

The hardware described above is designed to fit these requirements, given certain limitations. As can be seen from Figure 7, the present configuration allows for output rates to the processor of

$$\frac{f_{\text{SAMPLE}}}{128M} = \frac{f_{\text{CODE}}}{64M}.$$

Since $f_{\text{DATA}} = 2^{-D} f_{\text{CODE}}$, we have $f_{\text{OUT}}/f_{\text{DATA}} = 2^D/64M$. When D is large the rates are acceptable. For example, when $D = 12$, $f_{\text{OUT}} = (2^6/M) f_{\text{DATA}}$, and we may take M to be 4 giving an output rate of 16 times the data rate. This is suitable for data demodulation, tracking, etc. It must be verified that the rates are compatible with acquisition requirements such as doppler bandwidth. The value of M can be decreased, if necessary, to provide larger bandwidths. The only important limitation for large D is that accumulation times become long, meaning that storage capacities are taxed. For example, for $D = 17$ $f_{\text{OUT}} = 2^{11}/M$ and to obtain a rate of 16 times the data, we must have $M = 2^7 = 128$. The accumulators have been designed to handle values of M at least up to 200 for the GPS application.

PN RATE DATA RATE	76.8K	153.6K	307.2K	614.4K	1.2288M	2.4576M	4.9152M	9.8304M	1.023M	10.23M	0
75 BPS	16x64	16x128	16x256	16x512	16x1024	16x2048	16x4096	16x8192	-	-	32x 1/32 (2400)
150 BPS	16x32	16x64	16x128	16x256	16x512	16x1024	16x2048	16x4096	-	-	32x 1/32 (4800)
300 BPS	16x16	16x32	16x64	16x128	16x256	16x512	16x1024	16x2048	-	-	32x 1/32 (9600)
600 BPS	16x8	16x16	16x32	16x64	16x128	16x256	16x512	16x1024	-	-	32x 1/32 (19200)
1200 BPS	16x4	16x8	16x16	16x32	16x64	16x128	16x256	16x512	-	-	32x 1/32 (39400)
2400 BPS	16x2	16x4	16x8	16x16	16x32	16x64	16x128	16x256	-	-	32x 1/32 (72300)
4800 BPS	16x1	16x2	16x4	16x8	16x16	16x32	16x64	16x128	-	-	32x 1/32 (153600)
9600 BPS	-	16x1	16x2	16x4	16x8	16x16	16x32	16x64	-	-	32x 1/32 (307200)
19200 BPS	-	-	16x1	16x2	16x4	16x8	16x16	16x32	-	-	32x 1/32 (614400)
38400 BPS	-	-	-	16x1	16x2	16x4	16x8	16x16	-	-	32x 1/32 (1228800)
76800 BPS	-	-	-	-	16x1	16x2	16x4	16x8	-	-	32x 1/32 (2457600)
50 BPS	-	-	-	-	-	-	-	-	20x32x31x1/2	200x32x31x1/2	

Table H-1. PN/Data Rate Combinations

For small D , however, the limitations are of a different nature. For example, when $f_{\text{CODE}}/f_{\text{DATA}} = 16$, we have $f_{\text{OUT}}/f_{\text{DATA}} = 1/4M$, which is clearly not acceptable for data demodulation. The problem arises because we have used the 4 times rate reduction to allow for high rate applications. When D is small the 4 x RR must be bypassed to allow for higher output rates. This will present no logic speed difficulties because, as may be seen from the table, when M is less than 4 the code rate is less than $1/4$ the fast GPS rate for which the rate reduction is required. Thus, the effective operation rate is less than in the GPS mode with the rate reduction.

The above assumes that it is possible to work with output rate approaching or equal to the data rate. If this is not acceptable, the only recourse is to operate without the correlators, since they provide an automatic rate reduction of 32 vs. the sample rate. It should also be noted that bypassing the 4 times rate reduction eliminates the scrambling of the phase estimates mentioned above. Thus, the compensation effected in the final rate buffering RAM must be undone for these cases. This is not a major problem since it involves only some switching of address lines to the rate buffer RAM.

Data synchronization is derived for the generic PSK waveform from the PN code generator clocks (Figure H-7). For the demonstration system we will assume that the length of the PN code may be selected to be equal to 2^{D+K} chips, where K is chosen for convenience. For example, with $D = 10$, we may choose $K=11$. This gives a code length of 2^{21} chips and the bit sync clock is obtained by dividing the code generator clock by 2^{10} . Timing is shown in Figure H-9. The counter range must account for the worst case in which $f_{\text{CODE}}/f_{\text{DATA}} = 2^{17}$. A seventeen stage counter is therefore required.

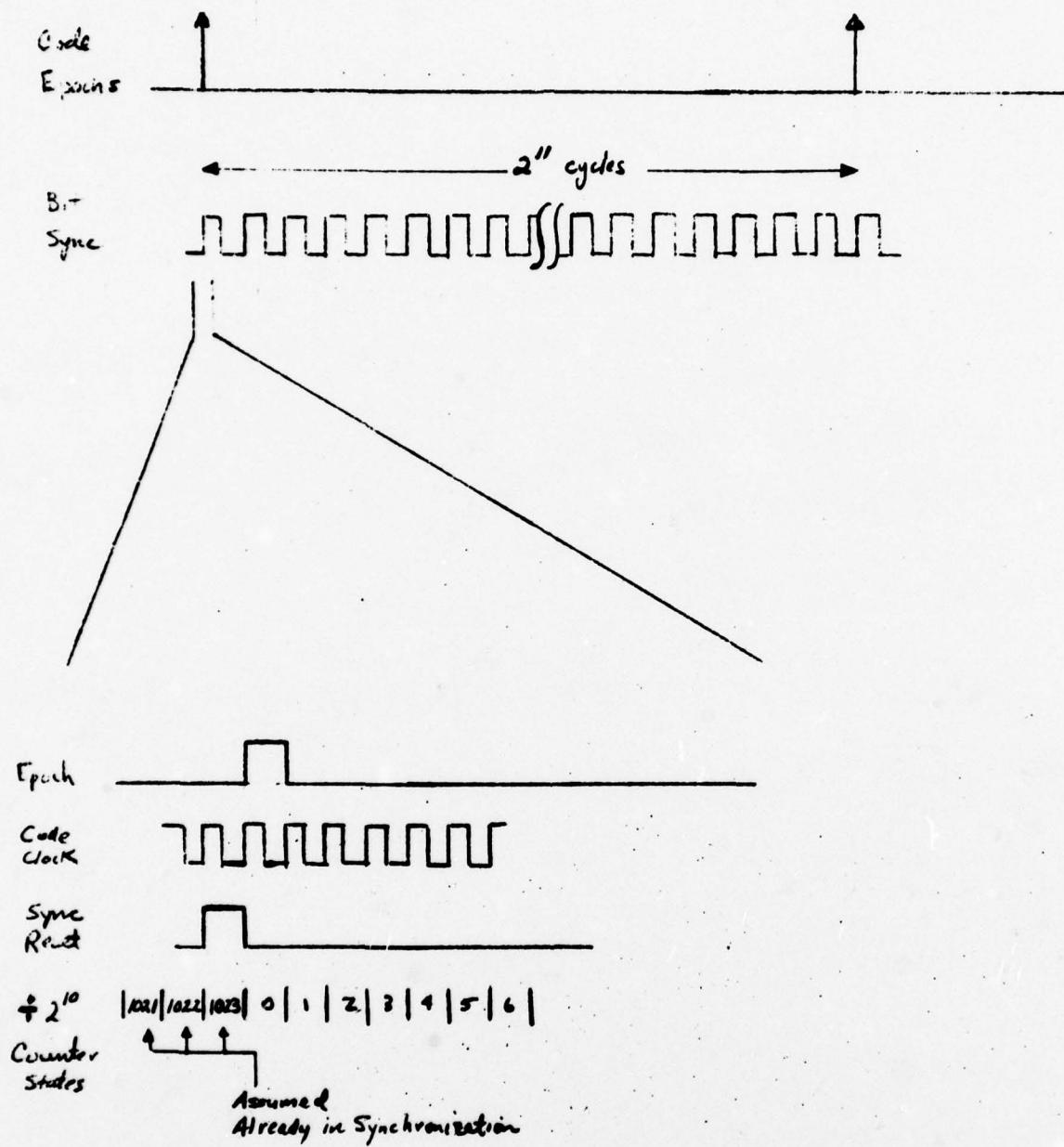


Figure H-9. PSK Code/Data Timing (D - 10, K - 11)

If K were chosen to be 4 in this case the code length again would be 2^{21} chips. By keeping the code length fixed, we maintain a fixed end state for the code and simplify the logic.

H.7 GPS Application

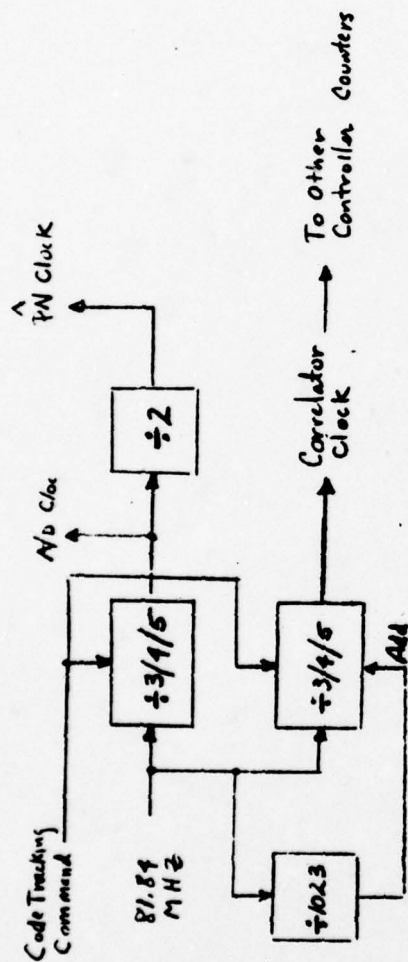
As mentioned above the GPS application causes difficulty because its code rate/data rate ratios are not a power of two. (The actual requirement is that the ratios have 2^6 as a factor). The ratios for GPS are 1023:200 and 1023:20 for the high rate and low rate codes. Since these are very close to $2^{10} \cdot 200$ and $2^{10} \cdot 20$, one approach for adapting the hardware is to assume the binary ratio and add one count every 1023. Another approach is to use the correlator as a 31-bit device since 1023 factors as 31.33. The former method has the disadvantage that it raises logic speed requirements and/or creates timing problems within the system as pulses are added. The latter method is complicated by having to adapt the 32-bit correlators to 31-bit operation. In this case the loading becomes involved as 31-bits of the reference must be loaded in 15 sample times. In addition, there is a one sample overlap between adjacent correlations as only 31 bits are flushed out of the correlator each cycle. Although a final decision will be deferred until detailed logic design becomes clearer, adding pulses apparently represents less of a modification to the existing design and is therefore proposed at this time.

There are two general methods for effectively speeding up the output rate to match the data rate. The system can operate with a faster system clock, or counts may be deleted in counters within the system. The former is conceptually simpler if speed requirements are not excessive, since it simply allows the system to run as usual but speeds up the clock. The latter method appears

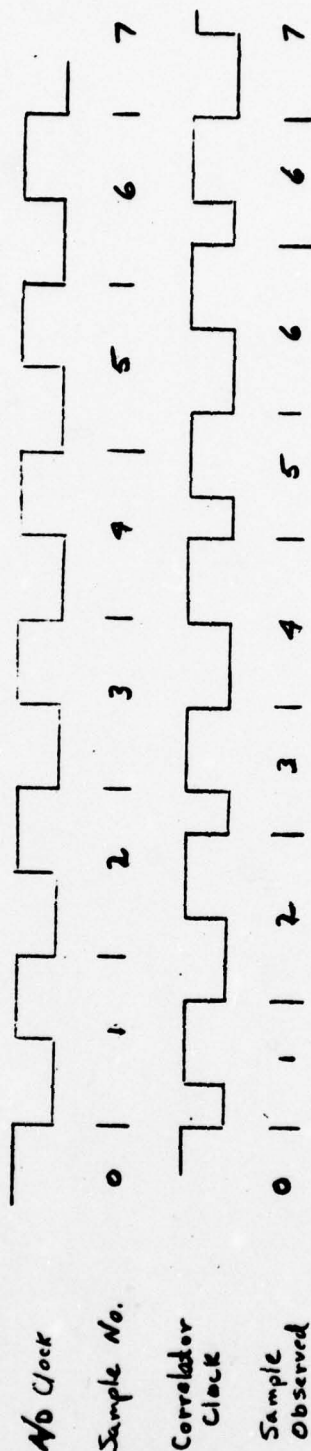
feasible here but timing effects within the system are not easily foreseen until detailed design is clear. Also, this method result in periodically shortened times between outputs to the MSP, which presents problems if processing time is critical. Since we must add pulses to the system clock anyway in order to do code tracking, the first method appears preferable and is proposed at this time.

The modification to the controller is shown in Figure H-10. The system clock is run at 81.84 MHz which is 8 times the code rate of 10.23 MHz. The counters shown are nominally $\div 4$, but may be changed to $\div 3$ or $\div 5$ to add or delete one count. The add/delete signal for code tracking goes to both counters, but the counter driving the correlators has an additional count added every 1023 counts. This effectively changes the rates in the lower leg of the diagram by $\frac{1024}{1023}$ without affecting system operation. The effective clock rate seen by the correlators is 20.48 MHz which may be divided by $2^{10} \cdot 400$ to produce the 50 Hz data rate (in the case of the high rate code). Now the correlators and the A/D are no longer driven from the same clock and the addition of pulses cause slippage of the samples with respect to the correlator clocks. The result is that one sample is repeated every 4×1023 cycles of the 81.84 MHz, or every 1023 samples. This is shown in Figure H-10(b) where a count is added every 7 cycles to speed up the process.

The repetition of one in every 1023 samples will have negligible effect on system operation. The hardware requirements, however, may become severe. When a pulse is added, the effective 20.46 MHz operating rate is raised to $4/3 \times 20.46$ MHz, or the operation time goes from 48.7 nsec to 37.5 nsec. The correlators are able to handle this increase in speed, but additions in the first RAM (4 times rate reduction) will probably not be possible. It may be necessary, therefore, to inhibit writing into the RAM when a pulse is added. This effect again will be insignificant.



(a) Timing Chain Modification



(b.) Correlator - A/D Slippage

Figure H-10. Controller Modifications for GPS

H-8. Doppler Wipeoff

The current configuration for accomplishing doppler wipeoff is shown in Figure H-11. frequency shift is performed digitally by phase rotating the I and Q correlator outputs through complex multiplication by sin/cos outputs from a ROM. This approach works well at high PN rates where the correlation interval is short and therefore, the correlation loss due to a frequency offset is small. However, at lower values of PN rates, the correlation interval increases for a fixed length correlator and therefore the loss due to a frequency offset increases. To remedy this situation, the doppler wipeoff must be performed prior to correlation. There are several ways of accomplishing this, of which two will be presented here. The first approach is shown in Figure H-12 The doppler wipeoff is performed digitally just prior to correlation in a phase rotator just as in the previous approach. The difference, is that the word size is smaller. In terms of performance, these are losses involved in truncating the phase rotator output back to two bits to keep the number of correlators the same. This also affects the frequency tracking accuracy. It is difficult to assess the degradation except through simulation, but the losses will be greater than in the approach described below.

A second approach to providing doppler wipeoff is to convert the 70 MHz LO source in the quadrature A/D converter to a tunable source. This is shown in Figure H-13 The tunable 70 MHz signal is generated in a digital synthesizer (NCO) whose frequency is controlled by the microprocessor. The filtered NCO output is used to down-convert the 70 MHz IF signal to baseband. The NCO is required to have a resolution of 1 Hz and a tuning range of ± 15 KHz range and can be preset to any frequency in this range. In addition, the doppler frequency is given directly by the tuning command to the NCO and is as accurate as the NCO clock accuracy. It will therefore be the approach implemented for the SAM program.

Currently, the design activity is centered around optimizing the design of the digital NCO for this application in terms of minimizing implementation complexity and degradation due to spurious responses.

Included is an updated schematic of the special purpose processor (SSP) showing the deletion of the doppler wipe off logic and the simplification of the past accumulator.

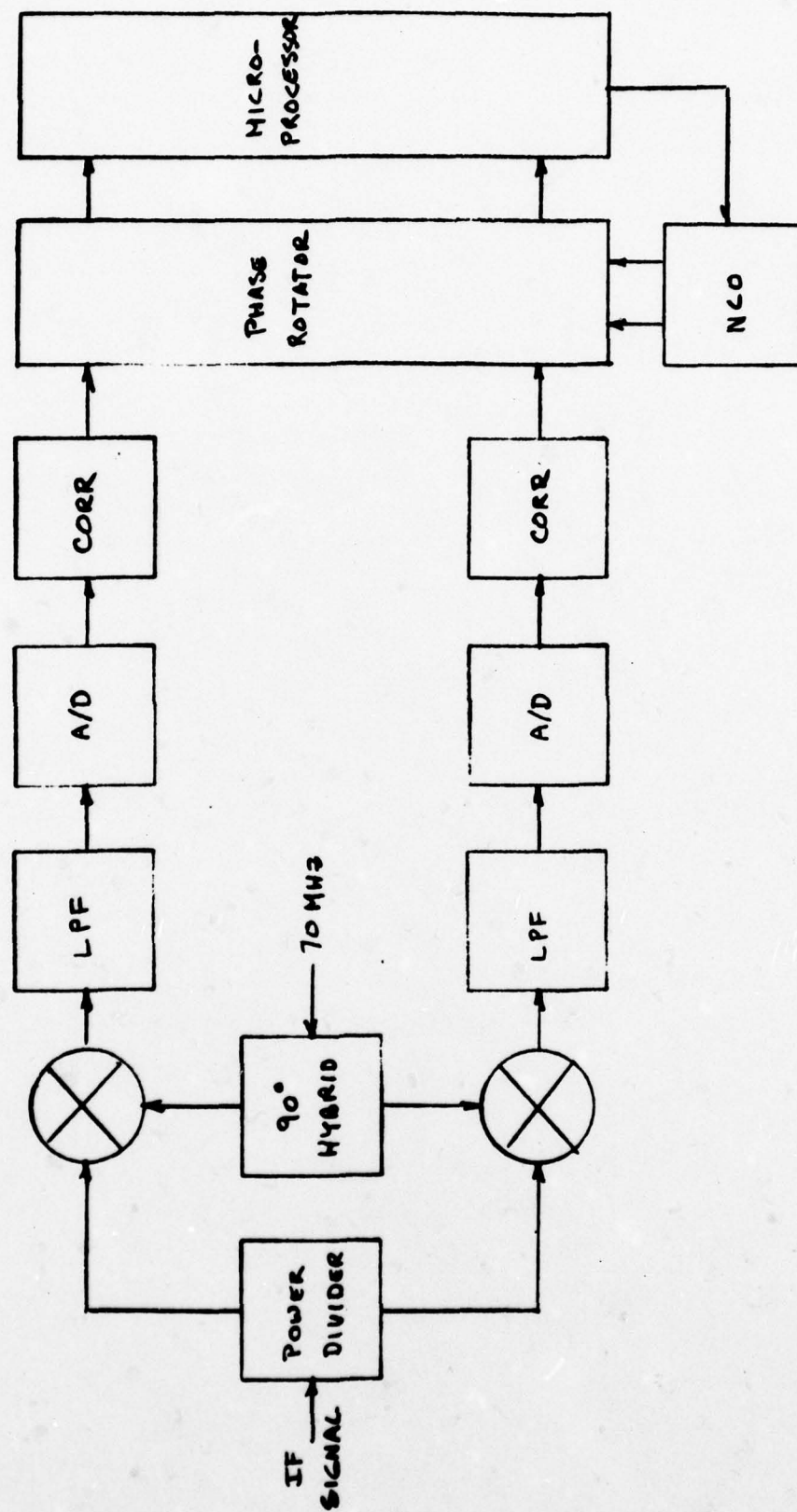


Figure H-11. Post Correlation Doppler Wipeoff

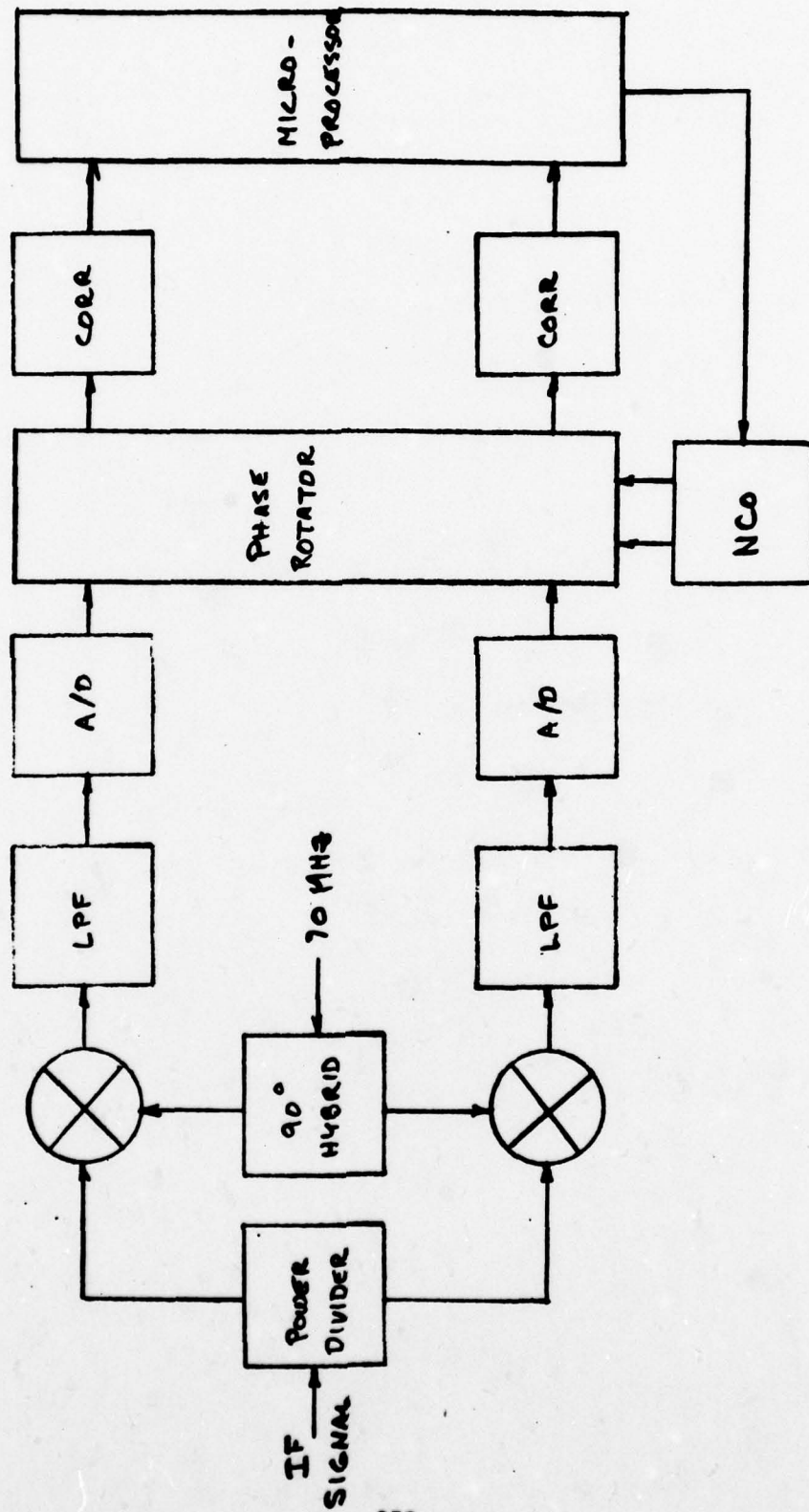


Figure H-12. Pre-Correlation Digital Doppler Wipeoff

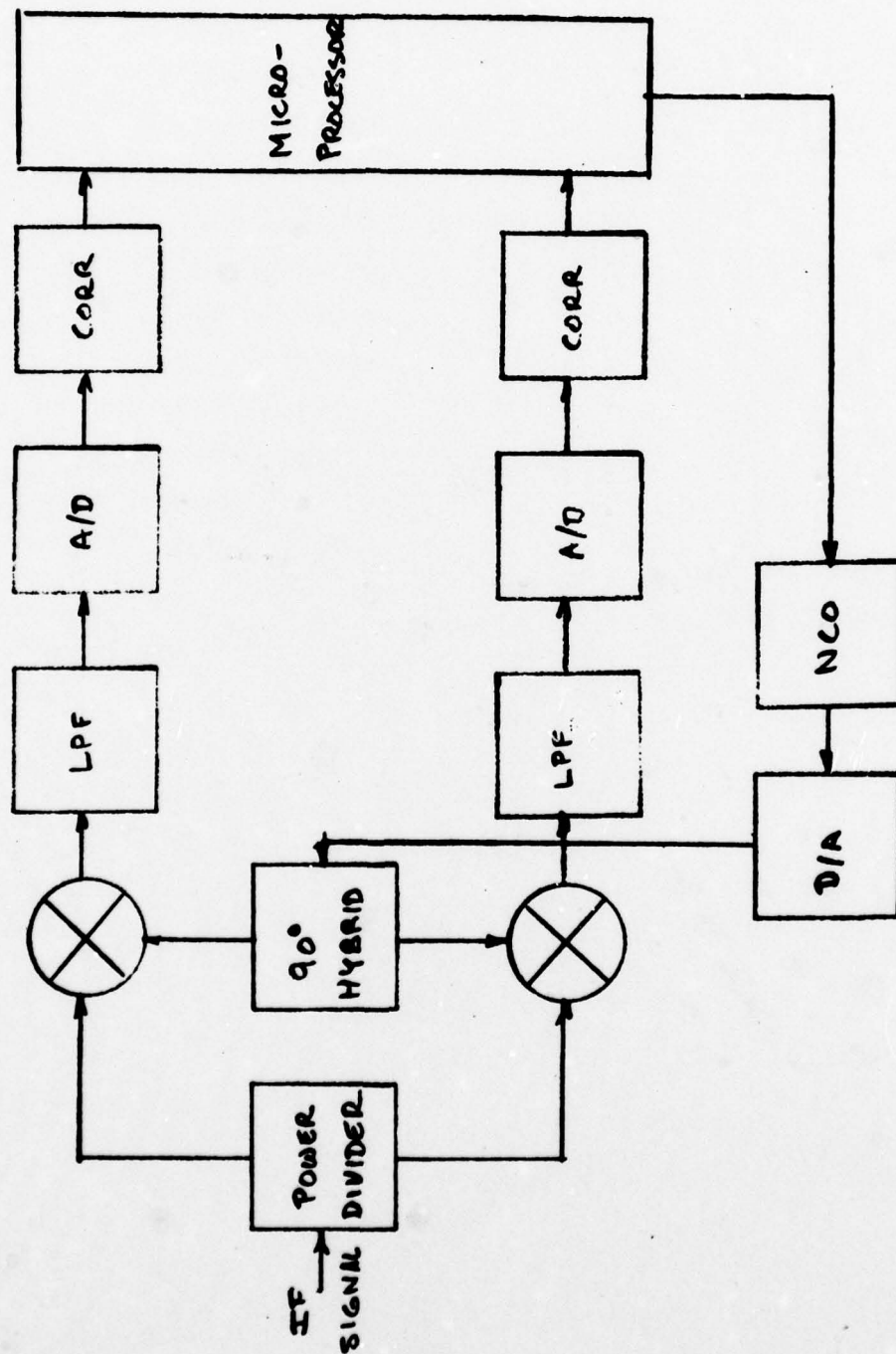
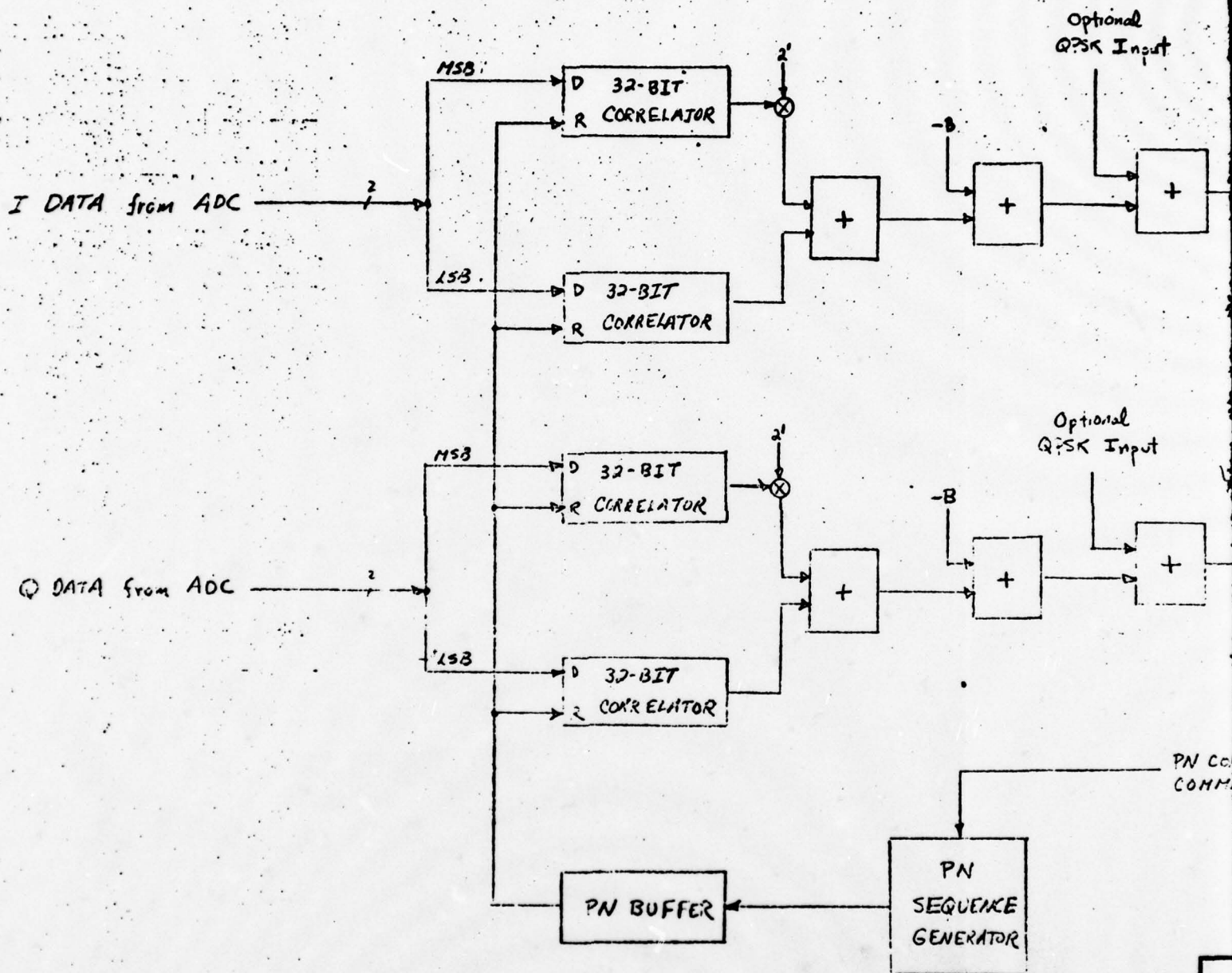


Figure H-13. Pre-Correlation Analog Doppler Wipeoff

SK



SK

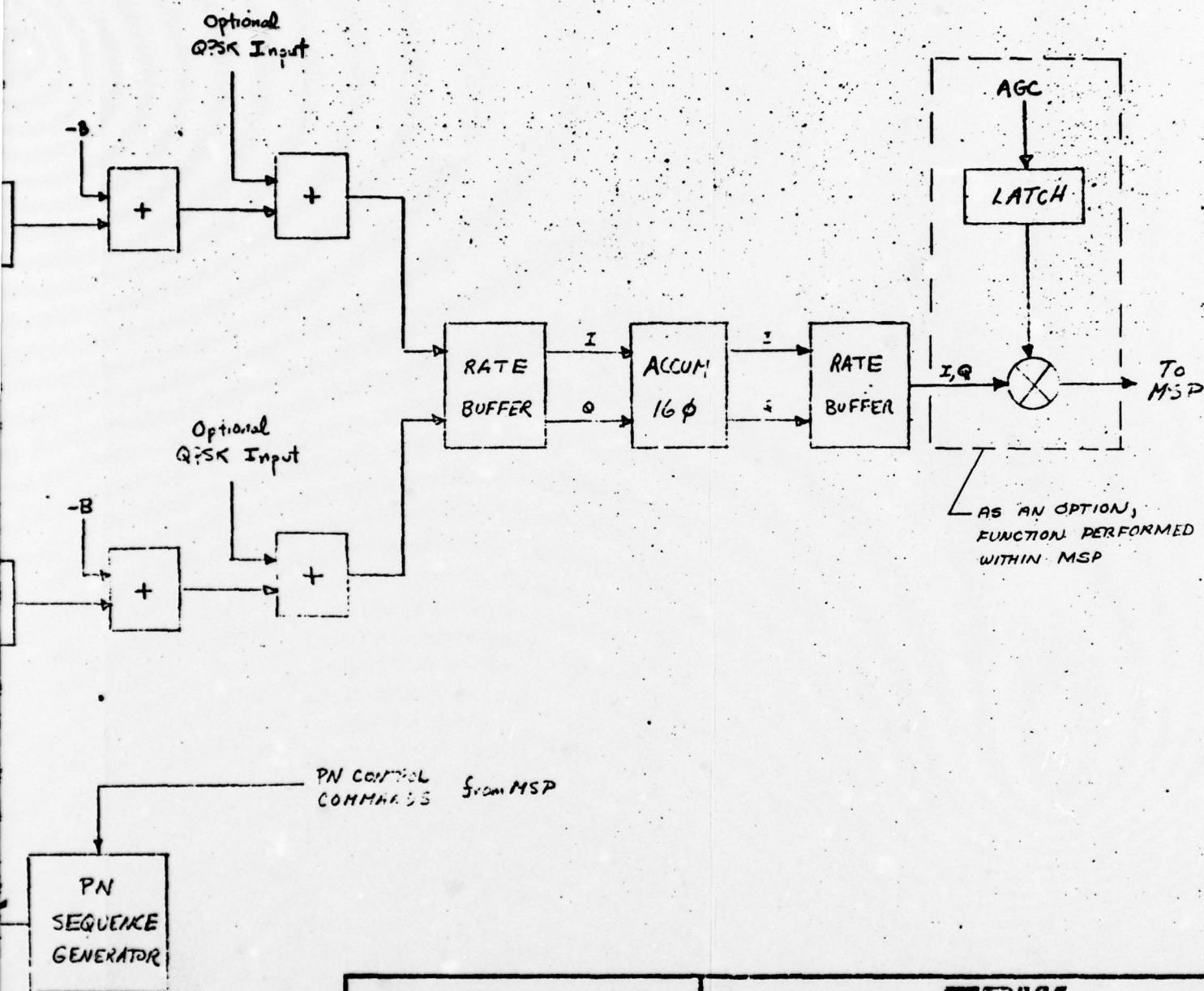
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ENGINEERING SKETCH

ORIGINATOR

C. T. ...

DATE

1-1-7

MJO

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SPECIAL PURPOSE DIGITAL HARDWARE

BLOCK 6A SRAM

SIZE

B

CODE IDENT NO.

11982

SK

361

SCALE

SHEET 1 OF

2

APPENDIX I
FREQUENCY GENERATOR DESCRIPTION

SUMMARY (Refer to the block diagram of Figure I-1)

The Frequency Generator module design is intended to serve as a standard frequency source for many modem applications. In the SAM system it will be used in two places — one to generate the 70 MHz local oscillator (L.O.) signal and another to generate $8f_{pn}$ (either 81.84 MHz or 78.64 MHz) for the Code Generator.

The Frequency Generator is a phase-locked loop type of indirect synthesis. All three of the frequencies required can be obtained by proper programming of the dividers. The designed capability is over 100 MHz. The sections of the Frequency Generator are:

- $\div M$: Includes a buffer to receive the input reference signal and an 8-bit programmable divider to scale the reference frequency.
- $\div N$: A programmable swallow counter in the feedback of the phase-locked loop. A dual modulus (10/11) prescaler divides the output frequency down to a range that can be handled by an 8-bit LS-TTL counter (P-Counter). The 10/11 prescaler modulus is controlled by a 4-bit counter (S-counter).
- ϕ/f : A Phase Frequency Detector consisting of a single I.C. plus a divider on the output to create an offset so the detector will operate in its linear region.
- $E(s)$: The low-pass Loop Filter which is an active filter prescaled by an R-C prefilter. The active filter components are on a plug-in DIP to accommodate other frequencies in the future. The cut-off frequency of this filter is at approximately 1/50 of f_{ref} .
- $F(s_2)$: The Spur Filter is required to attenuate the energy at f_{ref} that would otherwise modulate the VCO. The use of offset in the phase detector works to increase this energy.
- VCO : The Voltage Controlled Oscillator is a plug-in module to permit substituting a VCO in a different frequency range. This is the only part of the design that has been breadboarded. The operating frequency was approximately 50 to 125 MHz for control voltages within the range of the loop filter amplifier. A MECL device provides four buffered outputs from the VCO.
- $\div L$: This is a single I.C. auxiliary divider that can provide an output at the VCO frequency divided by 2, 4, 8, or 16. The selection is made with a hardware jumper on the board.

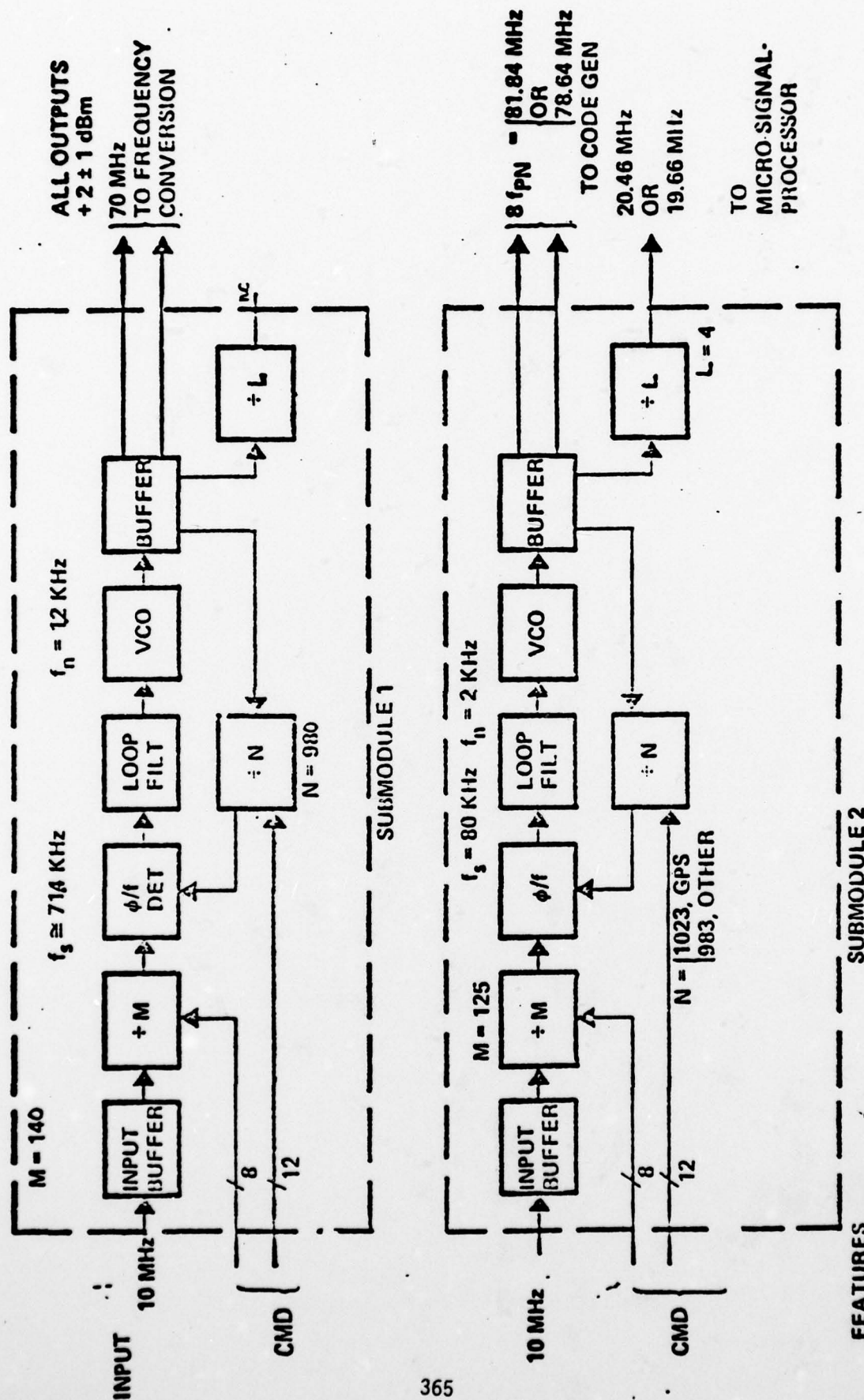


Figure I-1. Frequency Generator

DESIGN DETAIL (Ref. Schematic, Figure I-2)

÷ M (Figure I-3)

- The input buffer features are:
 - Capacitive-coupled input.
 - Select in test (or by individual design) input pad to permit attenuation and line termination.
 - Comparator buffer to accept virtually any input level and convert it to TTL. (The gain of the device is 3000 so an input on the order of the 5 mV input offset voltage is sufficient to provide a TTL output.
 - The comparator specs indicate operation to 13 MHz. Hirsh V. Marantz has tested an NE529 to 58 MHz with -45 dBm input (slightly over 1 mV)
 - Auxiliary TTL output to drive another board, if required.
- The input divider features are:
 - TTL input, output, and control lines.
 - Programmable divide range of 90 to 2579.
 - Maximum operating frequency calculated to be 13.3 MHz (see timing analysis, Appendix)
 - Minimum parts count by using the Carry-out signal rather than decoding and by not reclocking the decode with a flip-flop.

For the 70 MHz L.O., divide by M is set for 140 to give a reference frequency of 71.4 KHz.

For the 8 f_{pn} generator, the divide by M is set for 125 to give a reference frequency of 80 KHz.

÷ N Features: (Figure I-4)

- MC12513 prescaler with
 - MECL input to accept the VCO signal
 - On board MECL-to-TTL converter to permit driving low power Schottky counters.
 - TTL modulus control input to permit control by a TTL S-Counter.

- Divide range of 90 to 2579
- 4-bit S-counter which is programmed to give the "ones" digit in the divide ratio.
- 8-bit P-counter which is programmed to give the tens, hundreds, and thousands digits.
- f_{MAX} calculated to be 133 MHz. (See timing, Appendix)
- Minimized parts count by using carry-out to decode the final count and by not reclocking the terminal count with a flip-flop.

For a 70 MHz synthesizer, $\div N = 980$

For a 78.64 MHz synthesizer, $\div N = 983$

For a 81.84 MHz synthesizer, $\div N = 1023$

Offset Detector

- MC4344 I.C. with offset on the \bar{D} output to force the detector to operate in a linear region away from zero crossover.

The offset was arrived at by arbitrarily choosing a large but practical resistor divider ($1K : 100K = R_8 : R_9$) for the \bar{U} output of the phase comparator. The result is a 120 nS (calculated) pulse on the \bar{D} output. The disadvantage of this pulse is that it feeds through to the VCO and generates sidebands on the output. Thus, the need for the spur filter described below.

Note that R_q is included on a DIP platform with the loop filter components so it can be changed for different applications.

$\bar{F}(s)$

The synthesizer is fixed frequency so settling time is not a consideration. Setting $N=1000$, $f_N = 1.5$ KHz, $\zeta = 0.8$, $K_V = 6 \times 10^6$ Hz/V, $K_\phi = .12$ V/rad, $C = .047$ μ F and using Mike Cheong's HP9800 calculator routine yields $R_F = 3.6K$ and $R_S = 1.08K$. R_7 (R_F) was chosen to be 3.83K to insure sufficient damping if the loop is used under other conditions. The value of $R_5 + R_6$ (R_S) is 1K. The value is split into two components to provide a point for insertion of C_5 . The resulting RC network serves as a prefitter, eliminating the high frequency components (as do C7 and R8).

The loop filter components are installed on a pluggable DIP platform to permit changing the performance for different applications. This concept ties with the plug-in VCO to make the Frequency Synthesizer module adaptable to many applications.

F^(S2) Spur Filter

As mentioned above, a significant reference frequency signal can reach the VCO as a result of the offset technique used with the phase comparator. The relative magnitude of the sidebands generated by this signal on the VCO control line was calculated (See appendix) to be 19-25dB down from the VCO fundamental. A suppression of 60 dB was felt to be desirable so a spur filter (L3-C36) was included in this design to provide the necessary attenuation. The 3dB point of this network is 16 KHz which is a decade above the loop filter breakpoint. Inside the VCO housing is a second L-C filter that starts at 160 KHz. In applications where the reference frequency is higher, this section alone may be a sufficient spur filter.

VCO

The VCO uses Motorola's oscillator I.C. plus a varactor-tuned tank (D1,L2). This is the only circuit that has been breadboarded. The tuning curve is shown in the appendix. A test to determine the VCO sensitivity to power supply noise (See Figure I-5) shows only 10 to 20 dB sideband suppression with 100 mV peak-peak ripple on the power supply line. Thus supply line filtering is required even if the sidebands are reduced to 30-40 dB with a more realistic 10 mV ripple. Active filtering (regulator) would be desirable but the only supply voltages available are 5 and 15 volts. A regulator on the 15-volt line would dissipate twice the power required by the VCO itself, therefore, an LC passive network has been used.

÷ L

This auxiliary divider is simply a straight binary counter with optional ÷ 2, ÷ 4, ÷ 8, or ÷ 16 outputs selected by a hardwire jumper. The present application on SAM requires a ÷ 4 for the $8f_{pn}$ source.

A more general purpose programmable divider would be more desirable but it would have to be much more complex to operate up to 100 MHz.

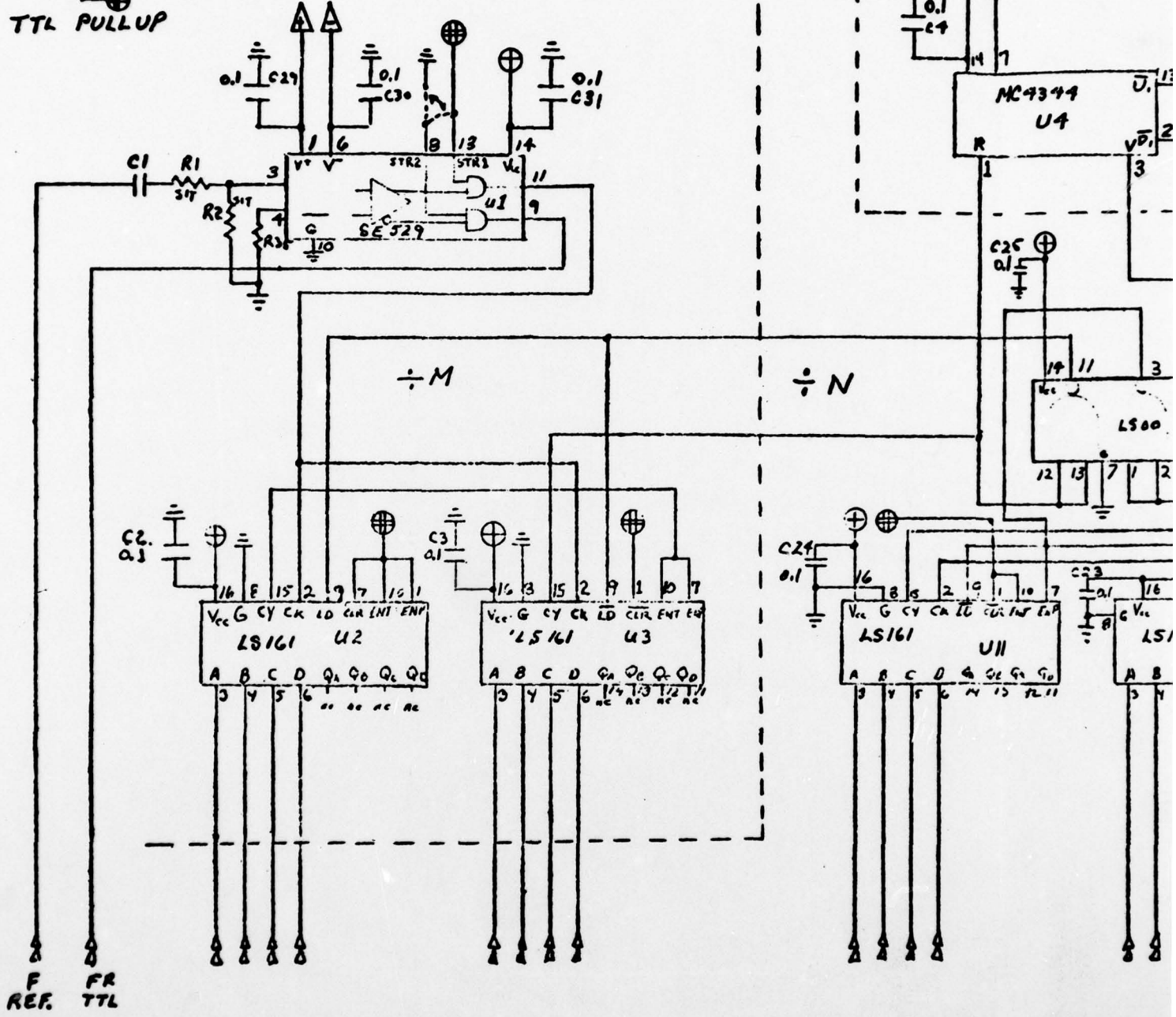
Frequency generator power requirements are given in Figure I-6.

X_{IN}
 R_{25}
 TTL PULLUP

ANALOG GND

DIGITAL GND

ϕ/F COMPARATOR



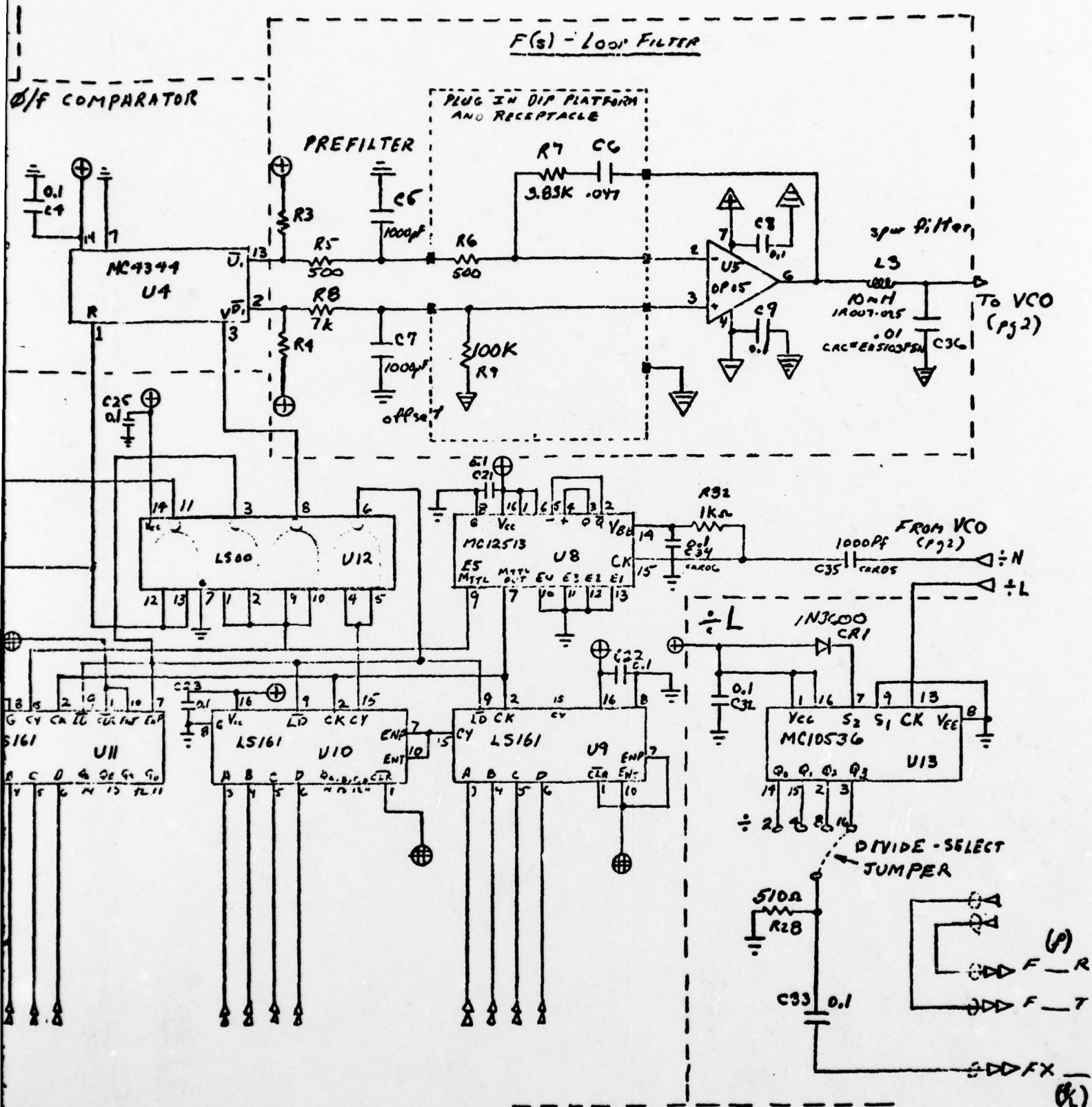
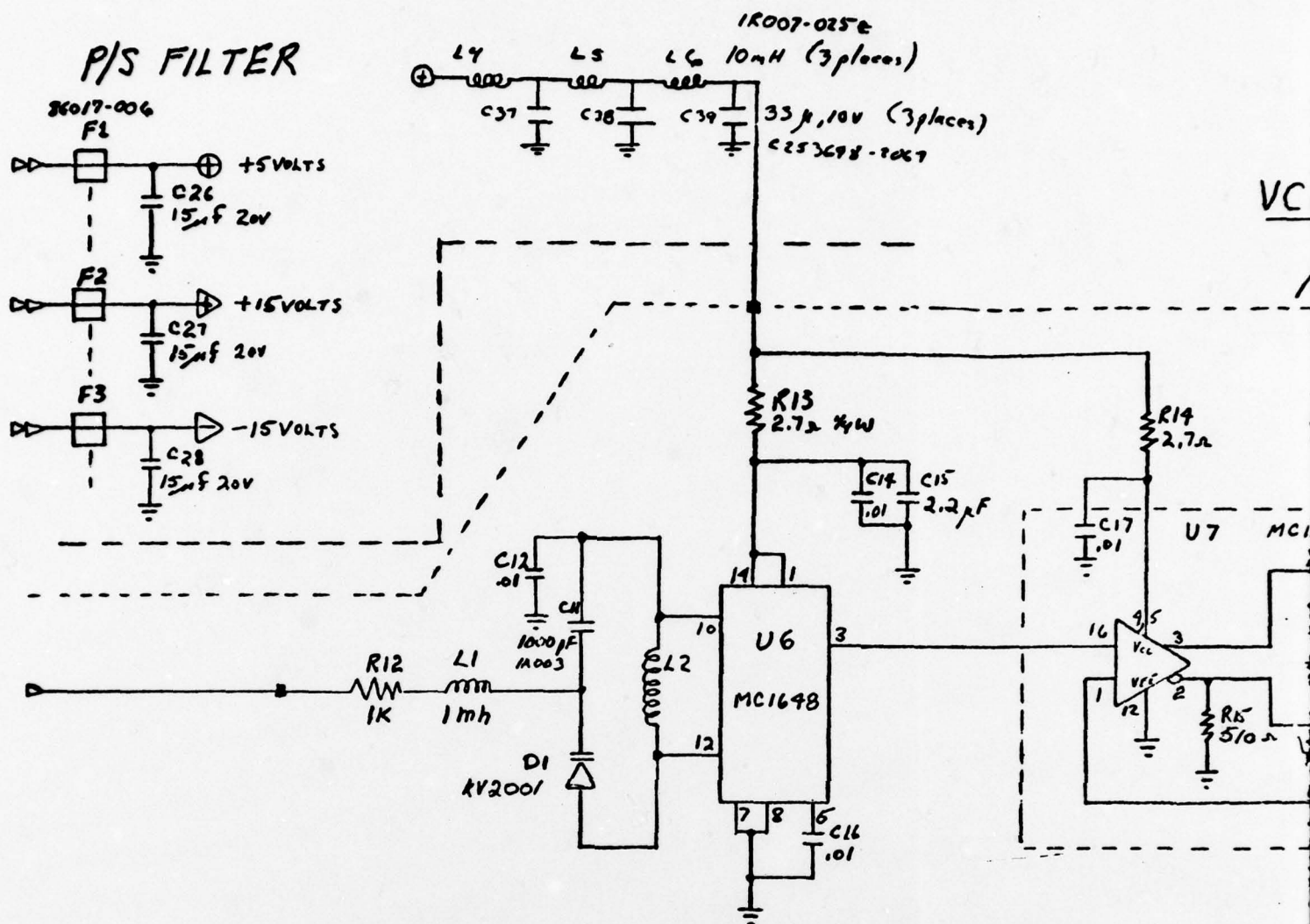


Figure I-2. SCHEMATIC, SAM-FREQ. GEN.

Fig 2a

2



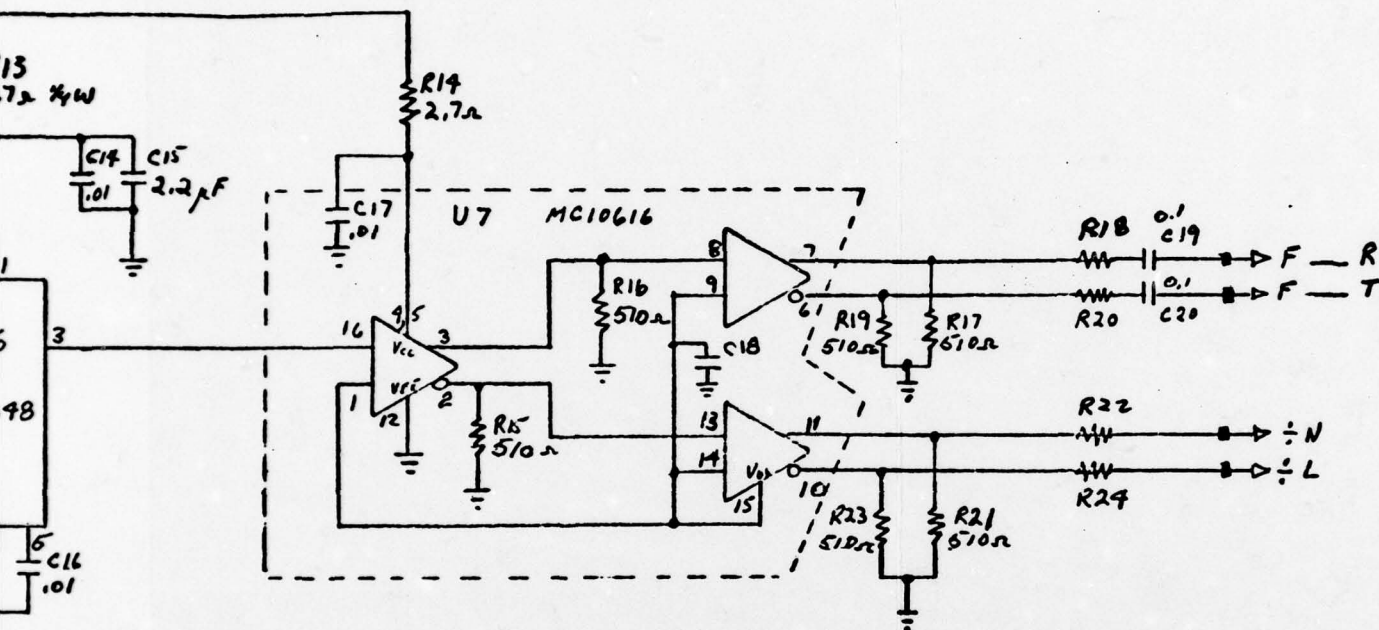
NOTES:

1. L2 IN VCO MODULE IS 6 TURNS OF NUMBER 22 MAGNET WIRE 3A025-46BV WOUND ON COIL FORM SP0163-4 WITH THREADED END REMOVED. 175 ± 10 MH.
2. ALL RESISTORS IN VCO ARE TYPE RC05. ALL CAPS IN VCO ARE 1A068-007 (UY12-113). EXCEPT C15 AND C11. C15 IS CSR13 2.2µF. AND C11 IS 1A003 1000 PP.
3. ALL RESISTORS IN ÷M, ÷N AND ÷L CKTS ARE RNC55's. ALL CAPS ARE CKR05 OR CKR06.
4. ALL CAPS IN P/S FILTER CIRCUIT ARE TANTALUM 20 VOLT TYPE CSR13
5. R25 IS RC07 TYPE.

6. VCO ICs ARE FLAT PACK AND FLAT PACK. A 14 PIN OR 16 EXCEPT 45 WHICH
7. R18, R20, R22 WIRES.

7-025e
(3 places)
10, 10V (3 places)
53698-7007

VCO PLUG-IN MODULE



6. VCO ICs ARE MC1498 14 LEAD FLAT PACK AND MC10616 16 LEAD FLAT PACK. ALL OTHERS ARE 14 PIN OR 16 PIN DIP PACKAGES, EXCEPT U5 WHICH IS 8-PIN TOS (TOTA)
7. R18, R20, R22 AND R24 ARE JUMPER WIRES.

Figure I-2. SCHEMATIC, SAM-FREQ. GEN.
(Cont)

M TIMING

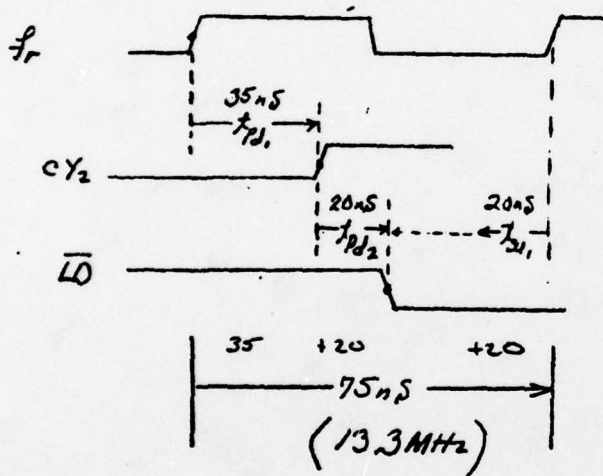
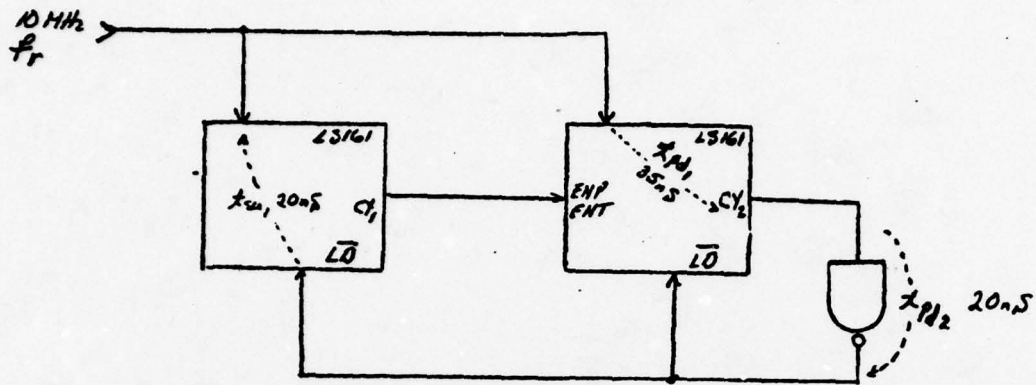


Figure I-3

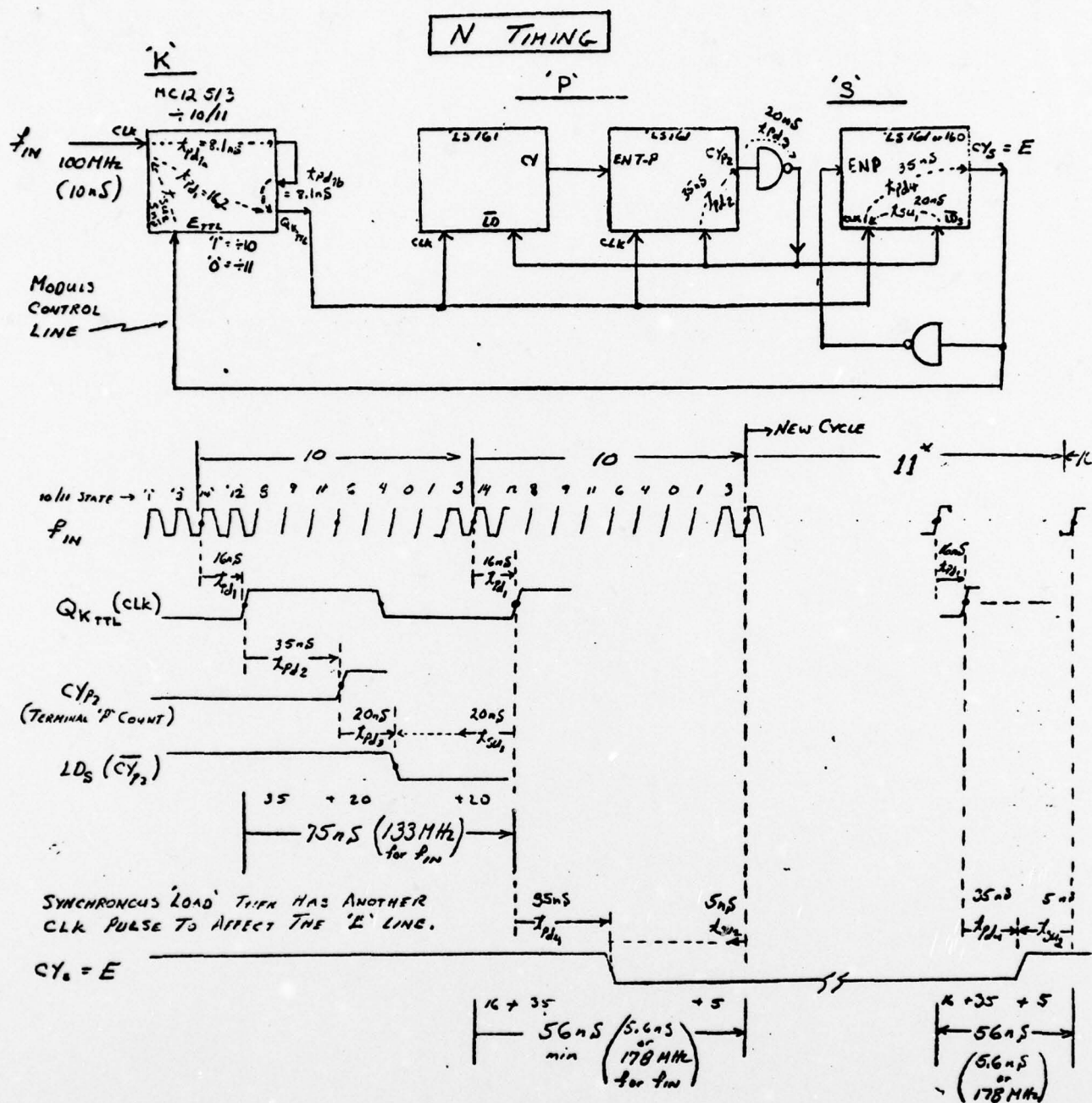


Figure I-4

All propagation delays and setup times are worst case times.

* If S counter is loaded with '15', CY_S (E) will stay 'Hi' to give no '11' counts.

SAM VCO TEST DATA

CONTROL VOLTS VRS; OUTPUT AMPLITUDE
AND FREQ

3/4/77
W.E.F.

CONTROL		OUTPUT			
VOLTS		VOLTS PP		FREQ (MHZ)	
1	min possible Diode forward bias 306	1.32		44.54(?)	
2		1.32		57.9	6
3		1.36		69.23	5
4		1.36		69.29	5
5		1.36		79.09	5
6		1.36		78.93	6
7		1.32		84.94	10
8		1.30		94.78	9
9		1.24		104.06	7
10		1.24		111.19	4.5
11		1.22		115.52	3.5
12		1.20		119.02	2.5
13		1.20		121.53	2
14		1.20		123.59	1.5
15		1.19		125.16	1.4
16	last point tried.	1.19		126.56	

CONTROL
VOLTAGE
P/S
HP 6204

10K

VCO

FREQ
COUNTER
HP 5341A
on development
test set

DVM
FUEL

Vcc
P/S

TEK
485
OSCILLOSCOPE

Figure I-5

SAM VCO TEST DATA

3/4/77
MST.

VCO TEST

VRIPPLE CONSTANT
SPUR SUPPRESSION

NO SERIES "R"
AND AC COUPLED

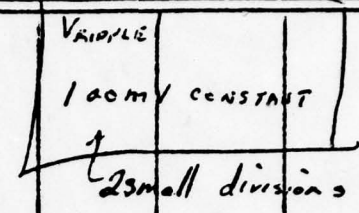
FREQ KHZ	SPURS dBc	VRIPPLE 100mV CONSTANT
1	-26 +4	
2	-10 -8	
3	-10	
4	-12	
5	-13	
6	-17	
7	-15	
8	-16	
9	-16	
10	-17	
11	-18	
12	-19	
13	-20	
14	-21	
15	-20	
16	-22	
17	-22	
18	-23	
19	-22	
20	-23	

Figure I-5 (Cont)

FREQUENCY GENERATOR

POWER REQUIREMENTS

SECTION	DEVICE	QUAN REQ	TYP POWER EACH (mW)	NET POWER	TOT POWER FOR SECTION	TOTAL MODULE
÷M	SE 529	1	250	250	450	
	LS 161	2	100	<u>200</u>		
÷N	LS 161	3	100	300	618	
	LS 00	1	8	8		
	MC12513	1	310	<u>310</u>		
φ/P	MC 4344	1	85	<u>85</u>	85	
F(s)	OF 05	1	90	<u>90</u>	90	
VCO	MC1648	1	150	150	490	
	MC 10616	1	100	100		
	PULLDOWN	6	40	<u>240</u>		
÷L	MC10536	1	625	625	665	
	PULLDOWN	1	40	<u>40</u>		
					665	
						2,398 mW

Figure I-6

AD-A065 629

TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CALIF
STANDARD AVIONICS MODULES (SAM) FOR EXISTING MODEMS.(U)
OCT 78 D AU, S 061

F/G 9/5

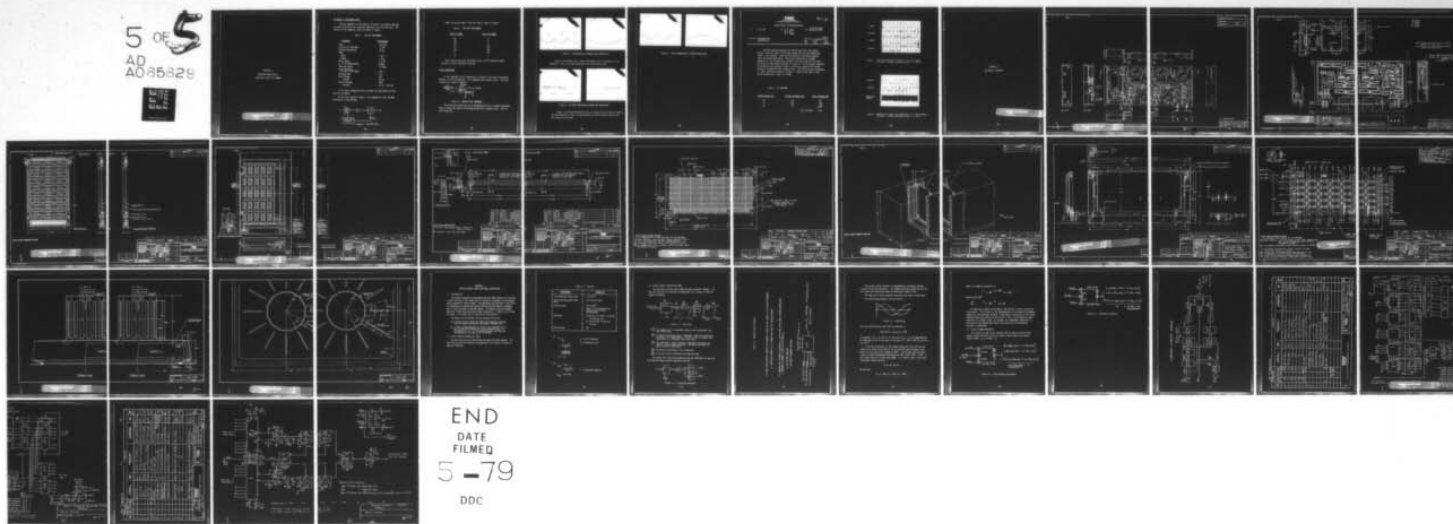
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APPENDIX J
MODULATOR (MOD) AND IF
AMPLIFIER (IFA) TEST SUMMARY

IFA MODULE: AGC MODULE TESTS

The key component in the receiver IF module, the Avantek AGC-330, has been tested both as a separate component, and in an AGC loop. The results of the component tests are shown in Table 1.

Table 1. AGC-330 PERFORMANCE

<u>Parameter</u>	<u>Measurement</u>
Gain	22.4 dB
Flatness (0 -200 MHz)	+1 dB
Maximum Attenuation	37 dB
VSWR	
Input	1.37:1
Output	1.19:1
Noise Figure	3.7 dB
P_o (1 dB Compression)	+3 dBm
Intercept Point	+10 dBm
Phase Variation (no AGC to full AGC)	163°
Response Time	3 μ s
Bias Voltage	15V
Current	27 mA
Control Voltage	0-5V
Current	20 μ A - 18.7 mA

All of these parameters meet or exceed the requirements of the receiver IF module.

An AGC loop, shown in Figure 1, was assembled to test the AGC performance of the AGC-330.

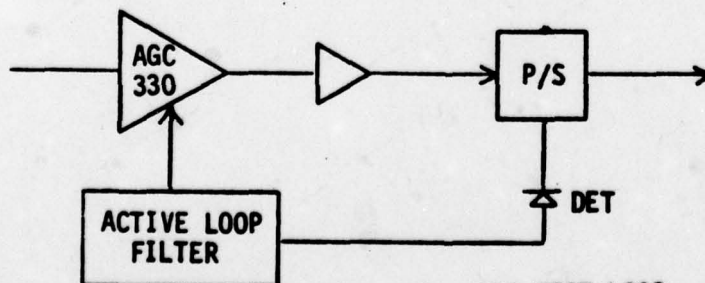


Figure 1. AGC TEST LOOP

Power out versus power in for the loop is shown in Table 2.

Table 2. AGC LOOP PERFORMANCE

<u>Power In (dBm)</u>	<u>Power Out (dBm)</u>
-32	0
-27	0
-22	0
-17	.03
-12	.05
-7	.07
-2	.1

These results show that the output level is held constant within .1 dB over an input variation of 30 dB.

ACTIVE MODULATOR

A key component of the transmitter IF module is the Texas Instruments SN56514, an active modulator. This component was tested as well. The test schematic is shown in Figure 2.

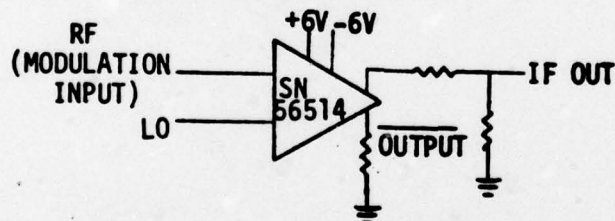


Figure 2. SN56514 TEST SCHEMATIC

The 56514 was tested both as an AM modulator and as a biphase modulator. Figure 3 shows the results of AM modulating with a triangle wave. This is true linear AM.

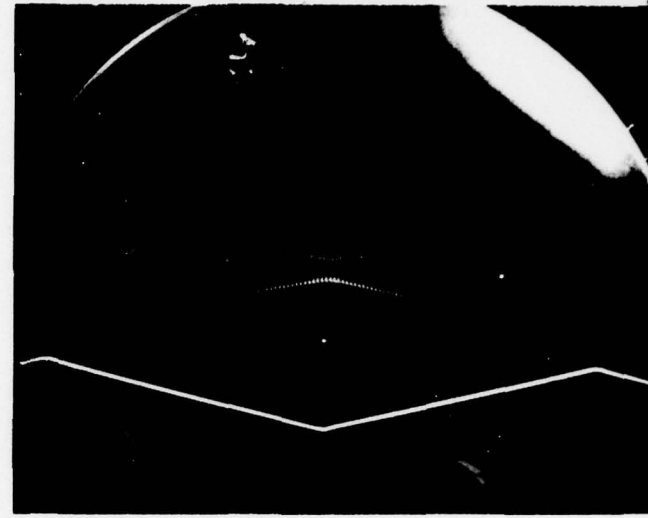
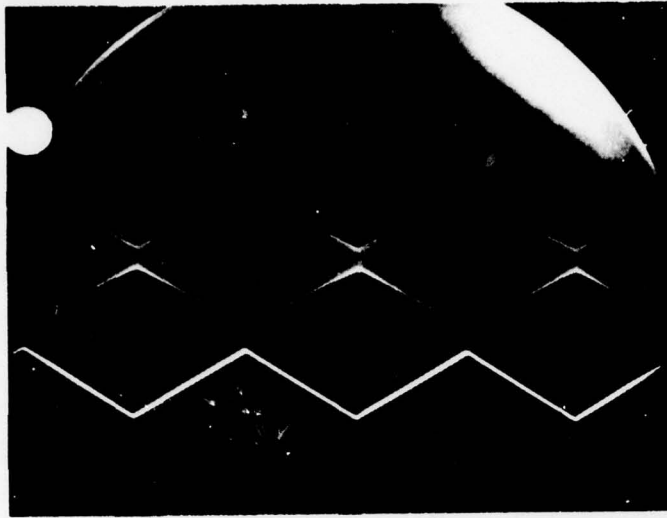


Figure 3. AM MODULATION, TRIANGLE WAVE MODULATION

Figure 4 illustrates the bi-phase performance with a squarewave as the modulator. This is bi-phase modulation with only slight error.

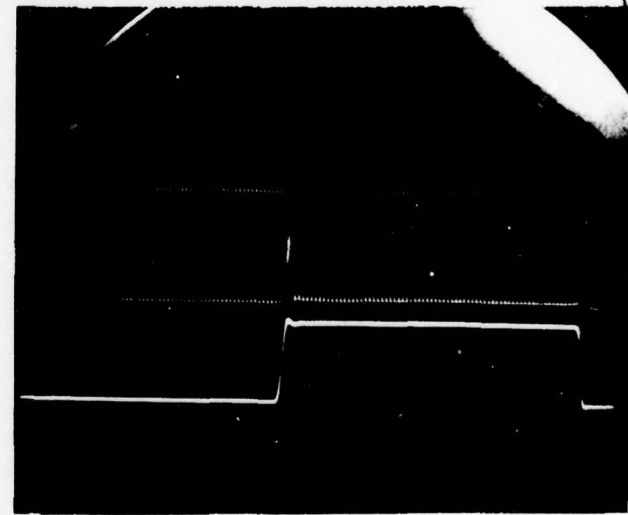
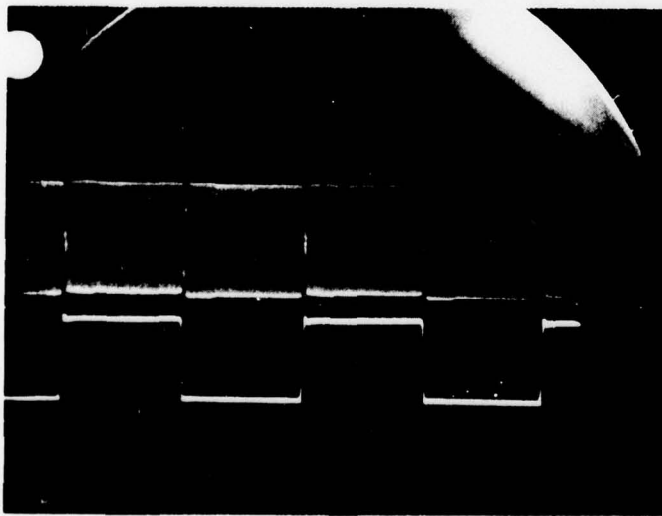


Figure 4. BI-PHASE MODULATION, SQUARE WAVE MODULATION

Figure 5 is 200% AM modulation with a sinusoid such as would be required for MSK modulation. There is some distortion at the crossover points, but this seems to be minimal.

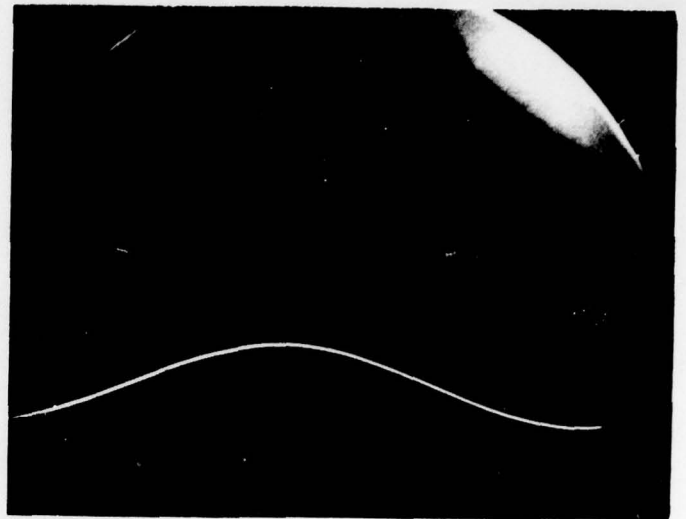
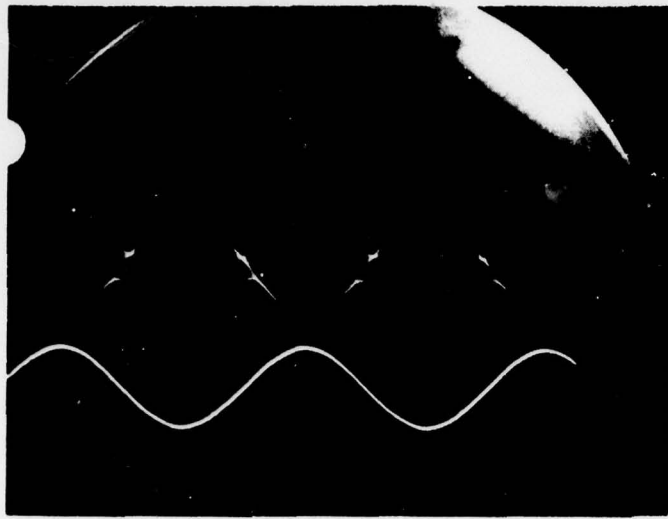


Figure 5. 200% AM MODULATION, SINEWAVE MODULATION

MAR 31 1977

INTEROFFICE CORRESPONDENCE

TO: S. K. Ogi

CC: R. K. Asato
D. K. Au
M. Y. Huang

DATE: 77-7327.01-023
March 31, 1977

SUBJECT: Performance of
SAM Modulator

FROM: D. E. Carlile *DEC*
BLDG MAIL STA. EXT.
M5 1170 63104

The QPSK modulator designed for SAM has been built and tested. Figure 1 shows the input I and Q data streams and also the demodulated output I and Q streams. Note the high degree of correlation between input and demodulated output. These data streams are at 10 MBPS. Demodulated I and Q output data streams at the same rate are also found along with the modulated RF output, in Figure 2. The DC voltages required for operation are included in Table I, which also contains the current and power consumed for each voltage source. The total DC power consumption is 1.32W. Required LO power at 70 MHz is -3 dBm and the level of the output demodulation signal is -20 dBm.

Table I. DC VOLTAGES

<u>Voltage Source (V)</u>	<u>Current Consumed (mA)</u>	<u>Power Consumed (W)</u>
+5	64	.32
-5	130	.650
+15	23	<u>.345</u>
Total DC Power		1.315

I INPUT

I OUTPUT

Q INPUT

Q OUTPUT

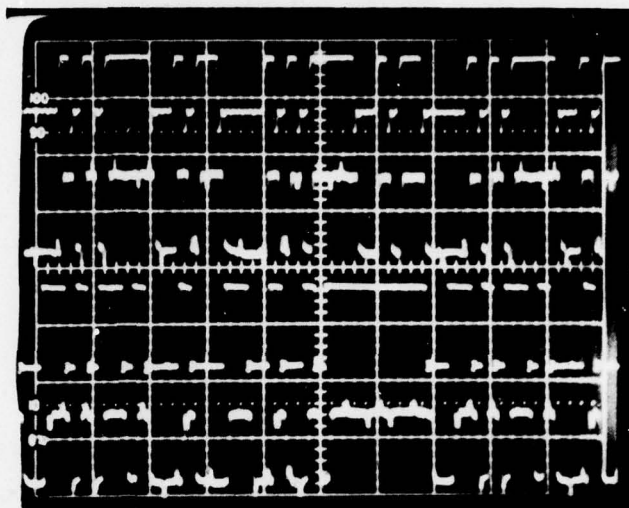


Figure 1. INPUT AND DEMODULATED OUTPUT I & Q DATA STREAMS,
BIT RATE = 10 MBPS, HORIZONTAL SCALE = .5 μ s/Div

I OUTPUT

Q OUTPUT

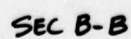
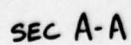
MODULATED
OUTPUT



Figure 2. MODULATED RF OUTPUT AND DEMODULATED I & Q DATA STREAMS,
BIT RATE = 10 MBPS, HORIZONTAL SCALE = .2 μ s/Div

APPENDIX K
SAM MODULE PACKAGING

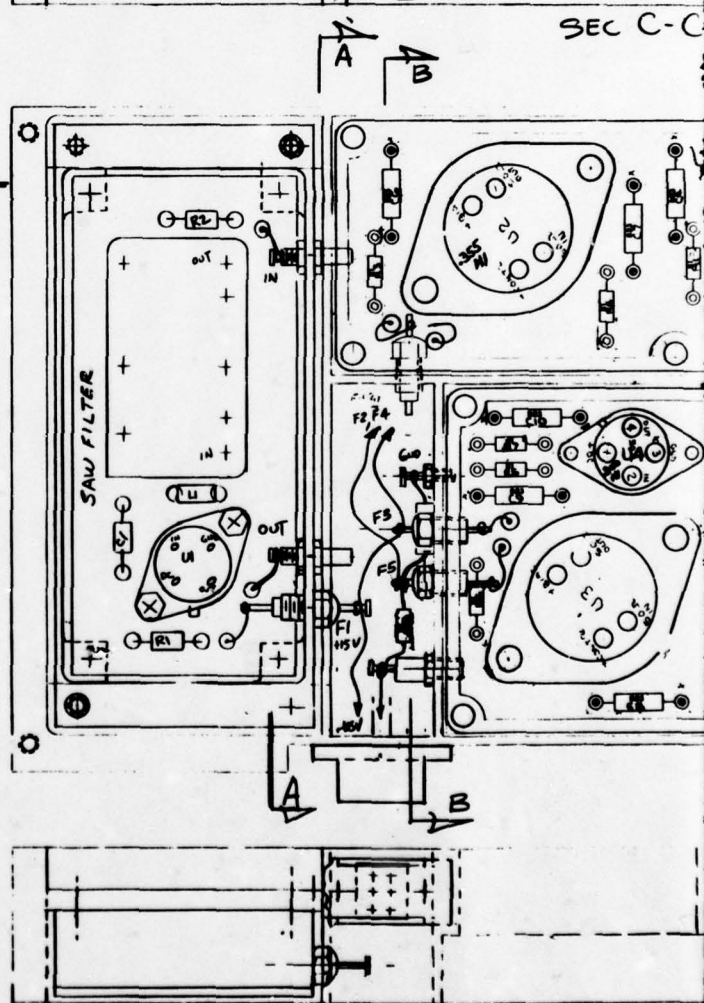
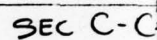




PTI-18/FALHIZC
3TUD, NON-INSL
2-56

F5 FILTER 3-92

PTI-12/210486E
TERM, INSULATED
A-40



FIGURE/TABLE NO. _____

PAGE NO. _____

REDUCE TO 55 %

SEC C-C

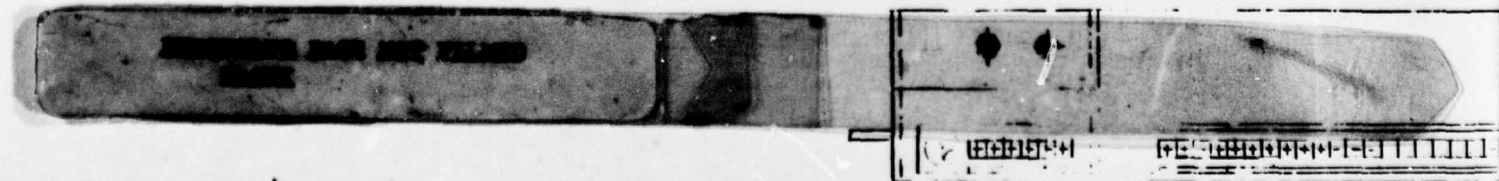
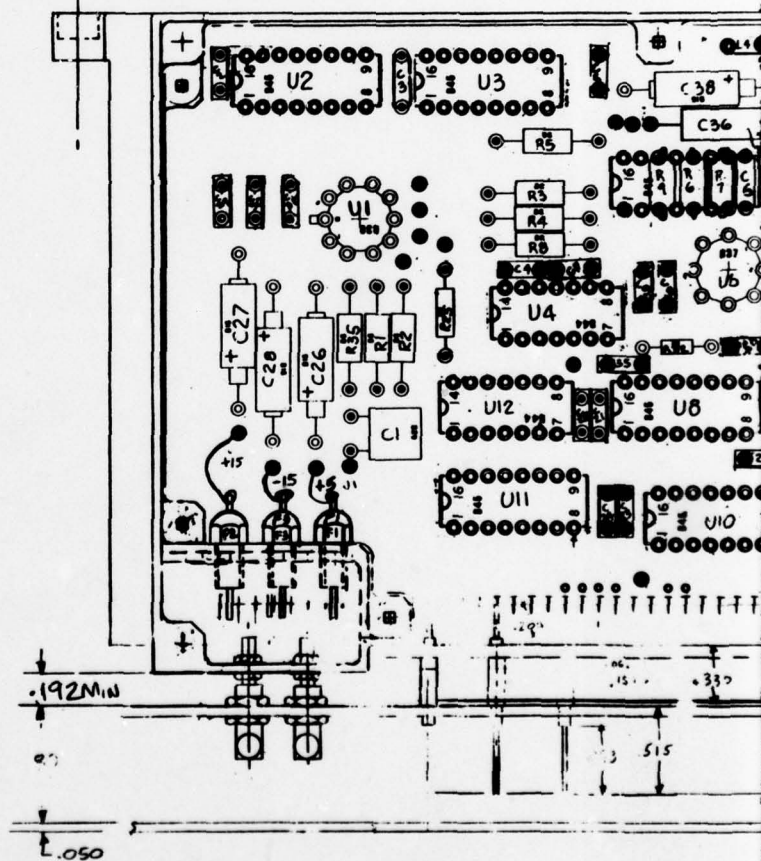
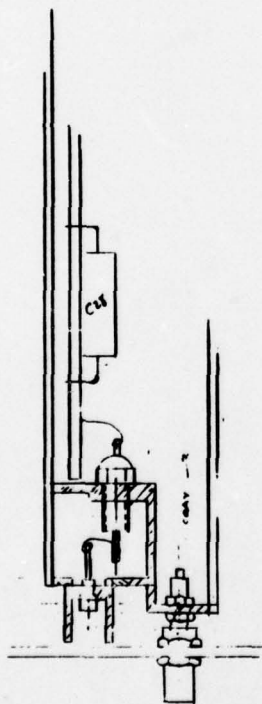
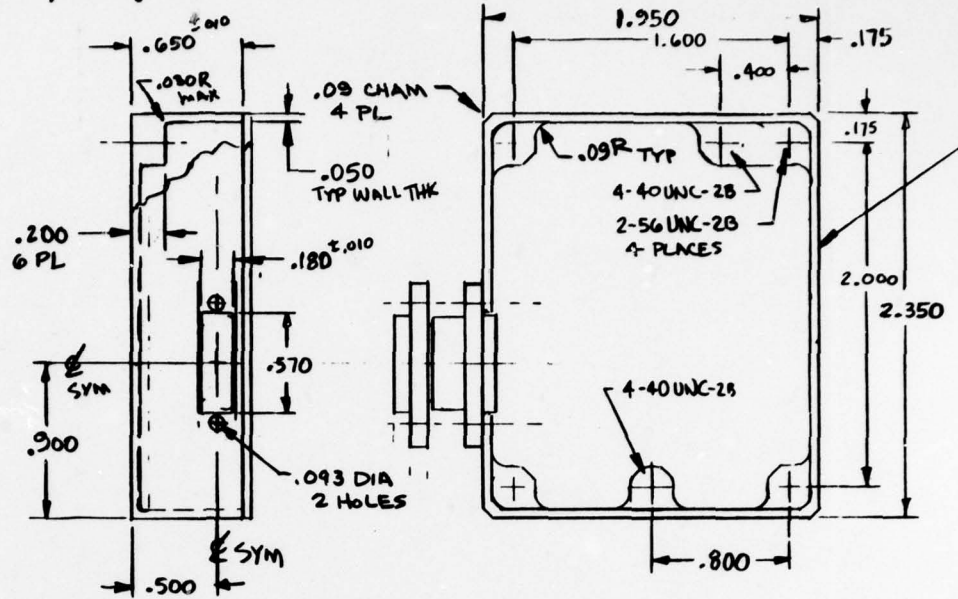
4C

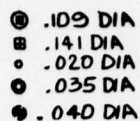
IF AMPLIFIER

SIZE	FORM NO.	LSK9225770	REV.
D	11982		
SCALE			SHEET

389

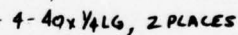
INCH SCALE





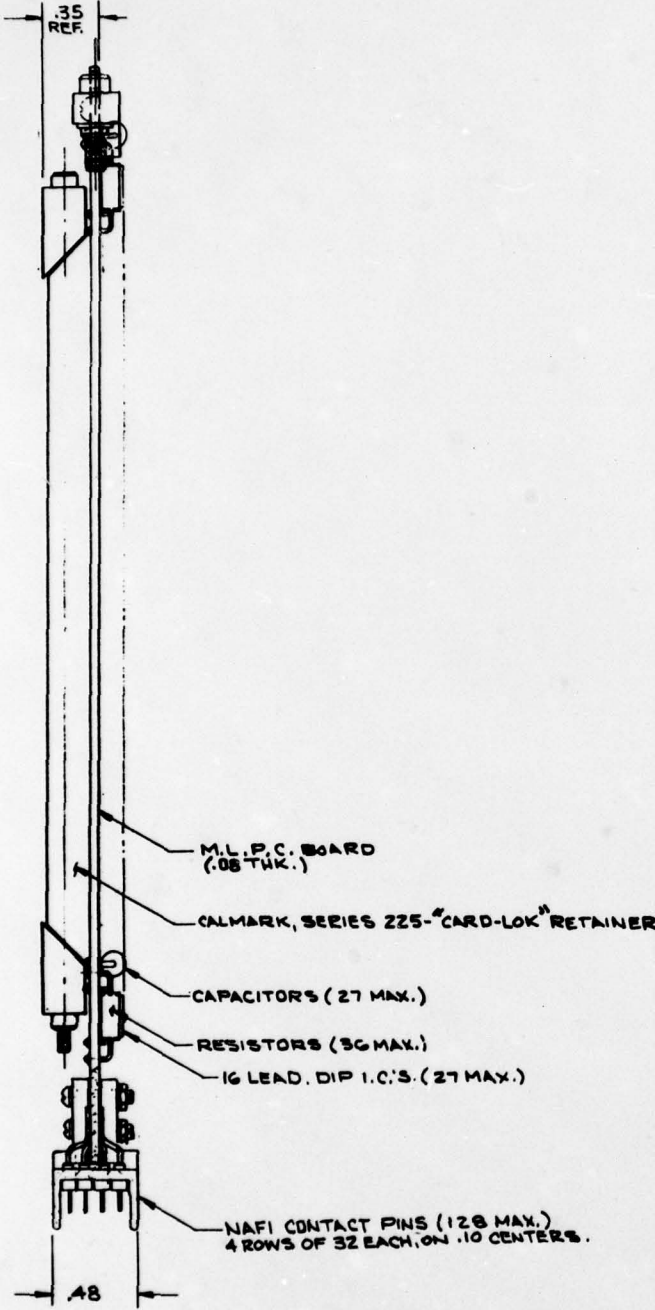
MALE CONTACT - 001-2513-501, M1000 SERIES
INSULATOR 304-0001-002 " "

FEM. CONTACT 010-2509-501, S1000 SERIES
INSULATOR 302-0002-002 " "



SIZE	FROM NO.		REV
D	11982	SK9228770	
SCALE			SHEET

REW ASSY.
(O.E.S.)



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

QTY REQD PER ASSY		PARTS LIST	
UNLESS OTHERWISE SPECIFIED		CONTRACT NO.	
1. DO NOT SCALE DRAWING. 2. INTERPRET PER MIL-STD-883. 3. DIMENSIONS ARE IN INCHES. 4. SURFACE TEXTURE SHALL BE 320 RMS. 5. REMOVE BURRS AND SHARP EDGES. 6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING. 7. DIMENSIONS, DATA IS FOR REFERENCE ONLY.		DRAWN CHECKED STRUCTURED DESIGNED SUPERVISOR PROJECT OTHER APPROVALS	
TOLERANCES		THE FOLLOWING EDS HAVE BEEN ATTACHED TO THIS PRINT	
ON ALL HOLE DIAMETERS		TRW	
UNDER .500 +.005		ONE SPACE PARK - REDWOOD BEACH, CALIFORNIA	
.500 THRU .750 +.005		1/2 ATR MODULE ASSEMBLY	
.750 THRU 1.000 +.005		SIZE CODE IDENT NO.	
1.000 THRU 1.500 +.005		D 11982	
1.500 THRU 2.000 +.005		SCALE 2 to 1	
2.000 THRU 3.000 +.005		393	
3.000 THRU 4.000 +.005			
4.000 THRU 5.000 +.005			
5.000 THRU 6.000 +.005			
6.000 THRU 7.000 +.005			
7.000 THRU 8.000 +.005			
8.000 THRU 9.000 +.005			
9.000 THRU 10.000 +.005			
ON DECIMAL DIMENSIONS			
.001 ± .001			
.002 ± .002			
.005 ± .005			
.010 ± .010			
.020 ± .020			
.050 ± .050			
.100 ± .100			
.200 ± .200			
.500 ± .500			
1.000 ± 1.000			
2.000 ± 2.000			
5.000 ± 5.000			
10.000 ± 10.000			
ON ANGULAR DIMENSIONS			
DOWNSIDE ± 5°			
UPSIDE ± 5°			
FURNISH			
HEAT TREAT			
APPLICABLE SPECIFICATIONS			
MIL-STD-883			
MIL-STD-130			
MIL-STD-153			
MIL-STD-169			
MIL-STD-199			
MIL-STD-200			
MIL-STD-202			
MIL-STD-203			
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MIL-STD-563			
MIL-STD-564			
MIL			

INCH SCALE

3.88
EDGE TEST
CONNECTOR
AREA
(30 PER. MAX.)

4.70
NAFI CONTACT
PIN AREA (144
PLACES MAX.)
3 ROWS OF 48.

7.62

.50 PITCH

ML/PC BOARD,
MODULE
16 LEAD I.C.
(25 PLACES MAX.)
CAPACITOR
(25 PLACES MAX.)
BOARD SUPPORT
STRUCTURE
RESISTOR
(30 PLACES MAX.)
ML/PC BOARD,
BASE
GROUND PLANE,
HEAT SINK

NOTES: UNLESS OTHERWISE SPECIFIED

AIR PLENUM

JACKSCREW ASSEMBLY

CALMARK, SERIES 225,
"CARD-LOK" RETAINER

.55 INTER-
CONNECT
AREA

4.88

4.70
NAFI CONTACT
PIN AREA (144
PLACES MAX.)
3 ROWS OF 48.

7.62

ML/PC BOARD,
MODULE

16 LEAD I.C.
(25 PLACES MAX.)
CAPACITOR
(25 PLACES MAX.)
BOARD SUPPORT
STRUCTURE

RESISTOR
(30 PLACES MAX.)
ML/PC BOARD,
BASE

GROUND PLANE,
HEAT SINK

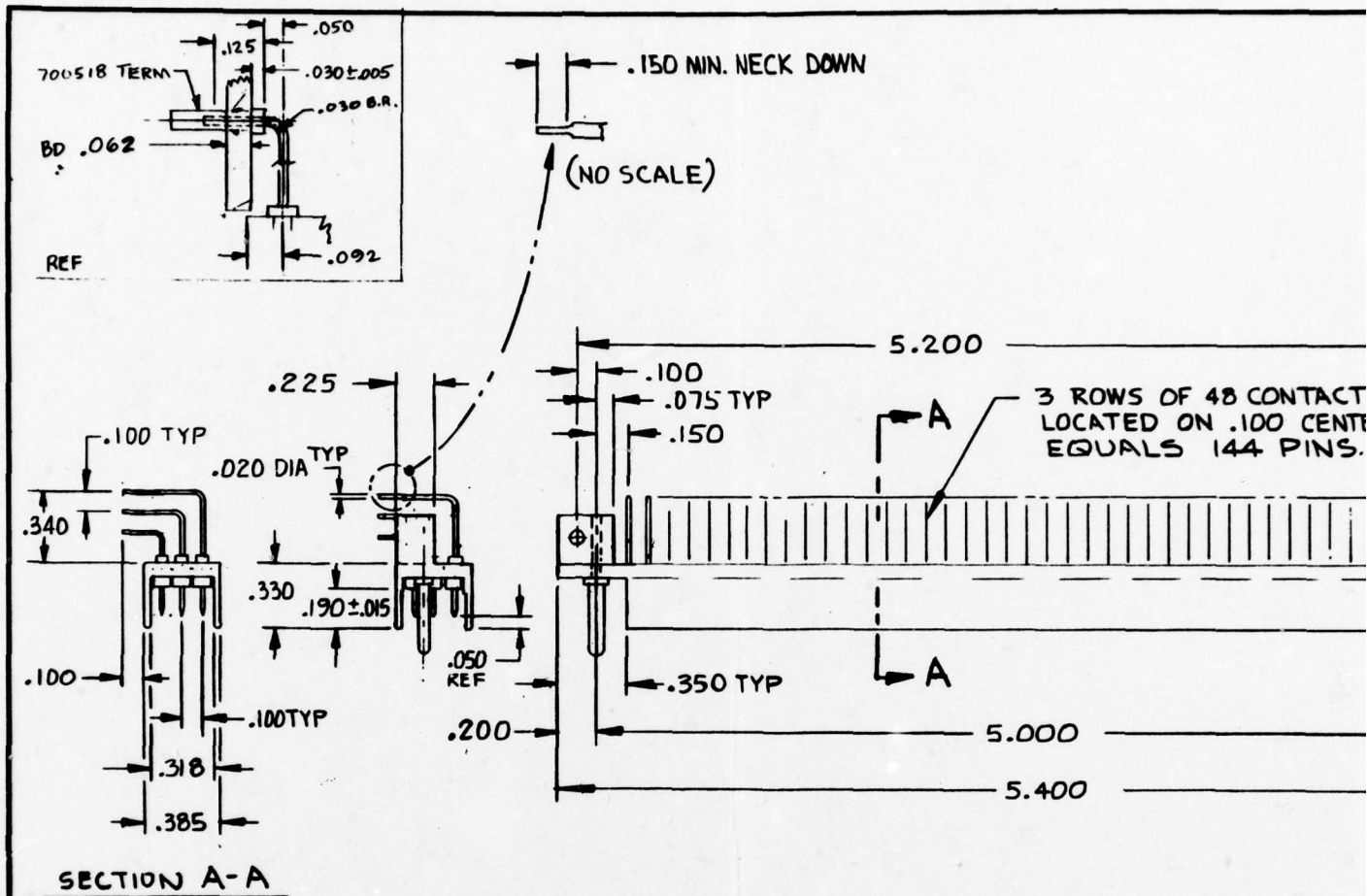
AIR PLENUM

JACKSCREW ASSEMBLY

CALMARK SERIES 225,
"CARD-LOK" RETAINER

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

QTY REQD PER ASSY	CODE IDENT NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPEC.	REV.	ITEM NO.												
<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>UNLESS OTHERWISE SPECIFIED</p> <p>1. DO NOT SCALE DRAWING. 2. INTERPRET PER MIL-STD-189. 3. DIMENSIONS ARE IN INCHES. 4. SURFACE TEXTURE SHALL BE 5. REMOVE BURRS AND SHARP EDGES. 6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING. 7. PARENTHEetical DATA IS FOR REFERENCE ONLY.</p> </div> <div style="width: 45%;"> <p>TOLERANCES</p> <table border="1"> <tr> <th colspan="2">ON ALL HOLE DIAMETERS</th> </tr> <tr> <td>UNDER .010</td> <td>+.000 -.005</td> </tr> <tr> <td>.014 THRU .125</td> <td>+.001 -.001</td> </tr> <tr> <td>.126 THRU .390</td> <td>+.002 -.002</td> </tr> <tr> <td>.391 THRU .590</td> <td>+.003 -.003</td> </tr> <tr> <td>OVER .591</td> <td>+.005 -.005</td> </tr> </table> <p>ON MECHANICAL DIMENSIONS: XXX ± .005 XX ± .003 X ± .001</p> <p>ON ANGULAR DIMENSIONS: HATCHED ± .010 LOCATING ± .010 FORMED ± .010 CHAMFERS ± .010</p> <p>FINISH</p> <p>HEAT TREAT</p> </div> </div>								ON ALL HOLE DIAMETERS		UNDER .010	+.000 -.005	.014 THRU .125	+.001 -.001	.126 THRU .390	+.002 -.002	.391 THRU .590	+.003 -.003	OVER .591	+.005 -.005
ON ALL HOLE DIAMETERS																			
UNDER .010	+.000 -.005																		
.014 THRU .125	+.001 -.001																		
.126 THRU .390	+.002 -.002																		
.391 THRU .590	+.003 -.003																		
OVER .591	+.005 -.005																		
<p>CONTRACT NO.</p> <p>DRAWN C.W.P.</p> <p>CHECKED</p> <p>STRUCTURES</p> <p>MATERIAL/PROCESS</p> <p>ENGINEER</p> <p>SUPERVISOR</p> <p>PROJECT</p> <p>OTHER APPROVALS</p>				<p>THE FOLLOWING EDS HAVE BEEN ATTACHED TO THIS PRINT</p> <p>TRW ONE SPACE PARK • REDWOOD BEACH, CALIFORNIA</p> <p>1/2 ATR BOX CROSS SECTION, WITH COMPATIBLE MODULE MOUNTED</p> <p>SIZE CODE IDENT NO. D 11982</p> <p>SCALE 2/1</p>															
<p>APPLICABLE SPECIFICATIONS</p> <p>THE ABOVE TRW SYSTEMS GROUP SPEC FOR A PART OF THIS DRAWING</p>		<p>395</p> <p>SHEET 10 of 1</p>																	



NOTES: UNLESS OTHERWISE SPECIFIED

- ① MAYBE PURCHASED FROM TERADYNE, LOWELL, MASS.
- ② CHEMICAL FILM PER MIL-C-5541

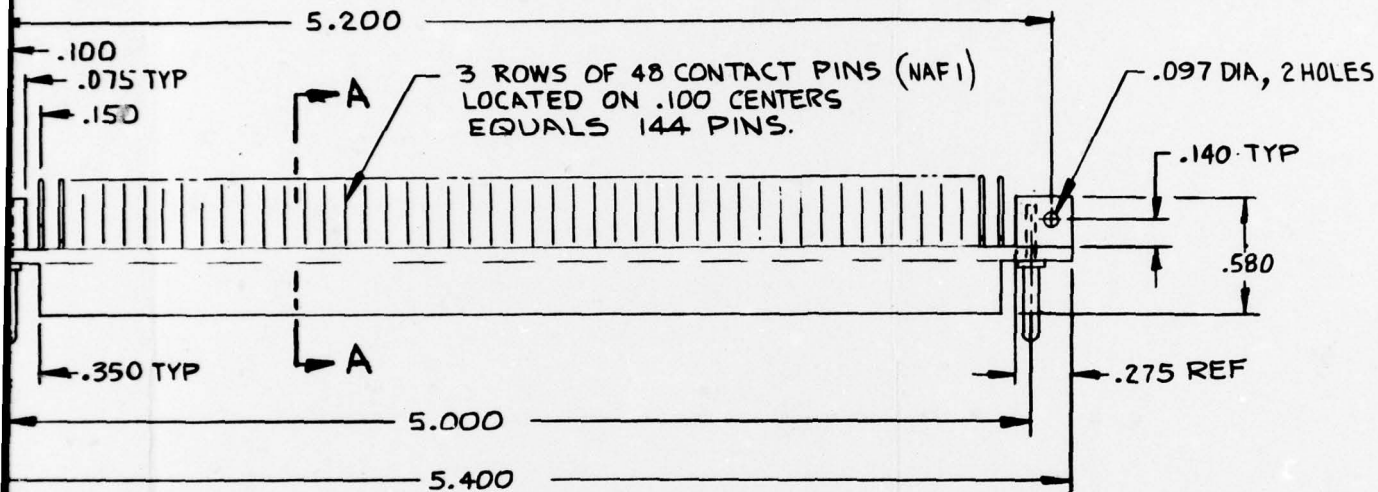
2	①	TBD	GUIDE
48		001-18 -509	CONTA
48		001-18 -509	CONTA
48		001-18X -509	CONTA
144		304-0001-002	INSULA
②	①	-11	FRAM

QTY REQD PER ASSY		CODE IDENT NO.	PART OR IDENTIFYING NO.	NOM
UNLESS OTHERWISE SPECIFIED				
1. DO NOT SCALE DRAWING. 2. INTERPRET PER MIL-STD-100. 3. DIMENSIONS ARE IN INCHES. 4. SURFACE TEXTURE SHALL BE 5. REMOVE BURRS AND SHARP EDGES. 6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING. 7. PARENTHEMETICAL DATA IS FOR REFERENCE ONLY.		TOLERANCES ON ALL HOLE DIAMETERS UNDER .010 $\pm .002$.501 THRU .750 $\pm .001$.014 THRU .125 $\pm .001$.751 THRU 1.000 $\pm .001$.126 THRU .250 $\pm .001$ 1.000 THRU 2.000 $\pm .001$.251 THRU .500 $\pm .001$ OVER 2.000 $\pm .001$ ON DECIMAL DIMENSIONS: .XXX $\pm .010$.XX $\pm .005$.X $\pm .001$ ON ANGULAR DIMENSIONS: MACHINED $\pm 9^{\circ}30'$ LOCATING $\pm 9^{\circ}30'$ FORMED $\pm 2^{\circ}$ CHAMFERS $\pm 9^{\circ}$		
FINISH		HEAT TREAT		
APPLICABLE SPECIFICATIONS		THE ABOVE TRW SYSTEMS GROUP SPEC FORM A PART OF THIS DRAWING		
USED ON	NEXT ASSY	NEXT ASSY QTY REQD	OTHER APPROV	

SAMS		
USED ON	NEXT ASSY	NEXT ASSY QTY REQD
APPLICATION		

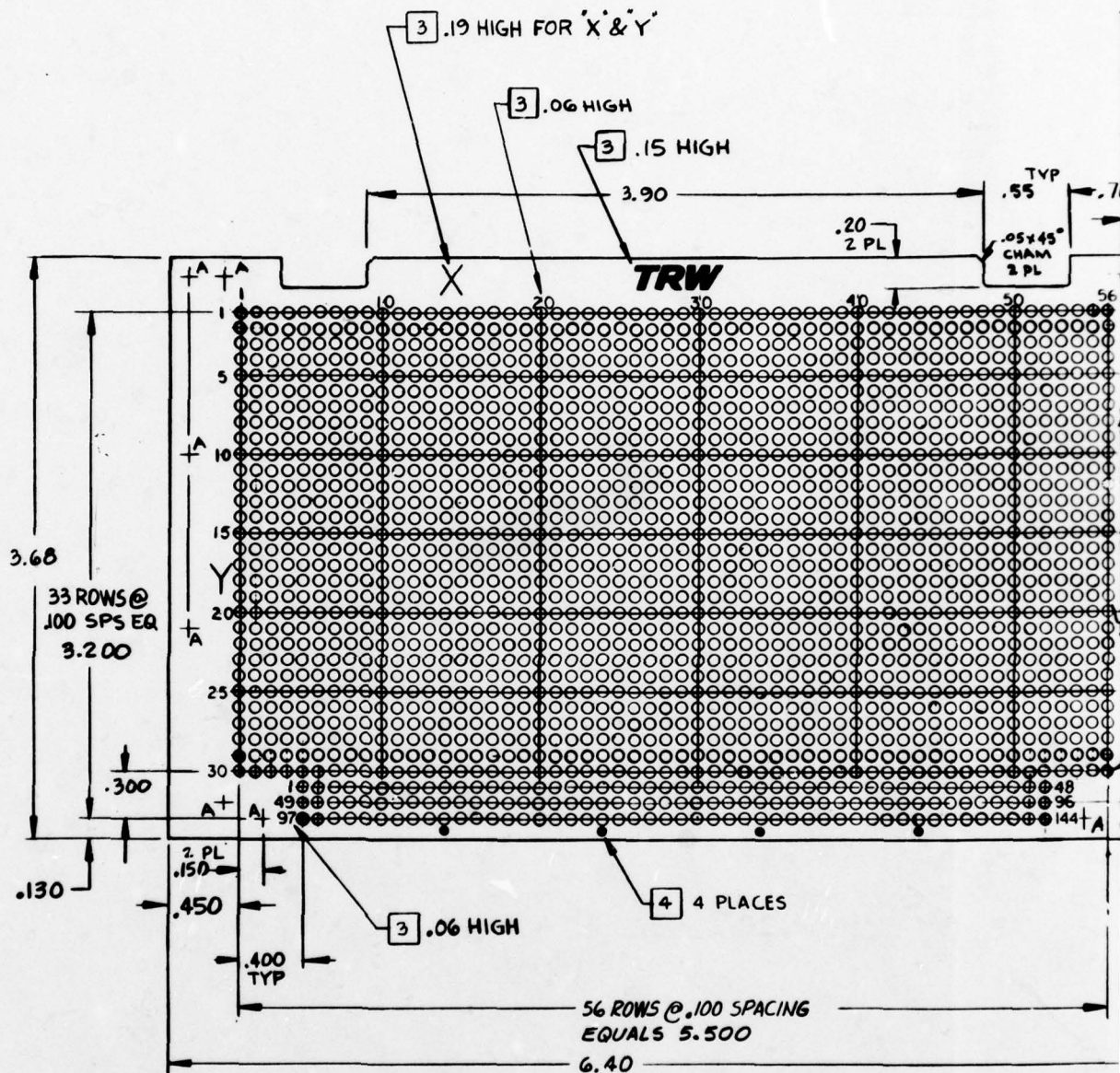
SCALE)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



2	1	TBD	GUIDE PIN				6			
48		001-18 - 509	CONTACT, LONG				5			
48		001-18 - 509	CONTACT, MED.				4			
48		001-18XX - 509	CONTACT, SHORT				3			
144		304-0001-002	INSULATOR				2			
2	1	1	-11	FRAME	6061-T6 OR 6063-T6 AL ALY		1			
			-1	CODE IDENT NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPEC	REF DES	ITEM NO.
QTY REQD PER ASSY				PARTS LIST						
UNLESS OTHERWISE SPECIFIED				CONTRACT NO.		THE FOLLOWING EO'S HAVE BEEN ATTACHED TO THIS PRINT				
<div>1. DO NOT SCALE DRAWING.</div> <div>2. INTERPRET PER MIL-STD-100.</div> <div>3. DIMENSIONS ARE IN INCHES.</div> <div>4. SURFACE TEXTURE SHALL BE</div> <div>5. REMOVE BURRS AND SHARP EDGES.</div> <div>6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING.</div> <div>7. PARENTHETICAL DATA IS FOR REFERENCE ONLY.</div>				TOLERANCES		DRAWN J.HOWE 4/27/77		<div>TRW</div> <div>SYSTEMS INC.</div> <div>ONE SPACE PARK • REDONDO BEACH, CALIFORNIA</div> <div>144 PIN CONNECTOR</div>		
				ON ALL HOLE DIAMETERS		CHECKED				
				UNDER .010 +.0025 -.0005		.501 THRU .750 +.008 -.001				
				.014 THRU .125 +.004 -.001		.751 THRU 1.000 +.010 -.001				
				.126 THRU .250 +.005 -.001		1.000 THRU 2.000 +.012 -.001				
		.251 THRU .500 +.006 -.001		2.001 THRU 2.800 +.015 -.005		STRUCTURES				
		ON DECIMAL DIMENSIONS:		ON ANGULAR DIMENSIONS:		MATERIAL/PROCESS				
		JXX ± .010		MACHINED ± 0°30'		ENGINEER				
		JXX ± .005		LOCATING ± 0°30'		SUPERVISOR				
		X ± .1		FORMED ± 2°		PROJECT				
		CHAMFERS ± 2°		OTHER APPROVALS						
FINISH						SIZE		CODE IDENT NO.		
HEAT TREAT						C		11982		SK9127771
APPLICABLE SPECIFICATIONS						SCALE 2/1				SHEET
THE ABOVE TRW SYSTEMS GROUP SPEC IS PART OF THIS DRAWING										

2

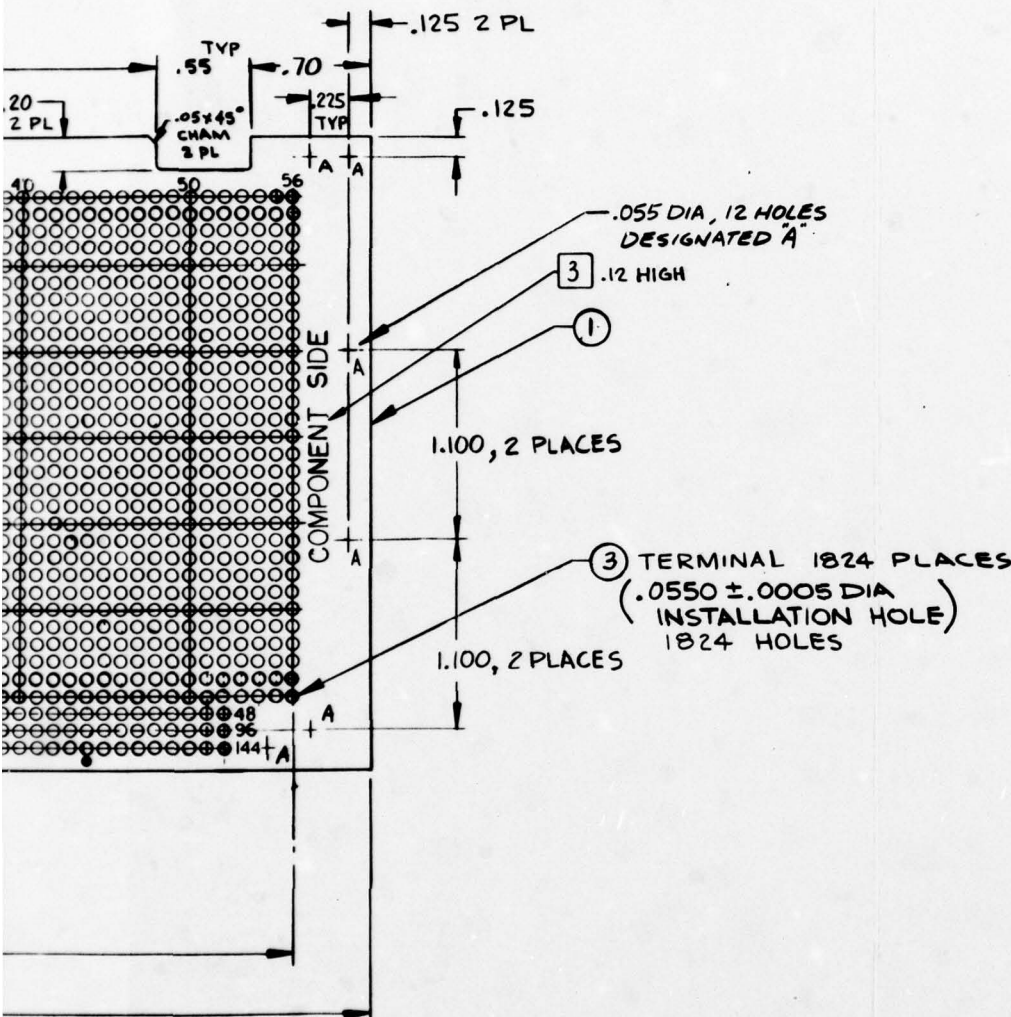


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL TERMINALS TO BE LOCATED ON .100 CENTERS
2. BOARD MATERIAL : .062 THK EPOXY GLASS CORE, BLUE COLOR, WITH 2 OZ COPPER FOIL ONE SIDE, SOLDER PLATED.
3. SILKSCREEN CHARACTERS WHITE, LOCATE APPROX AS SHOWN.
4. SILKSCREEN DOTS WHITE, .03 DIA. LOCATE ON EVERY TENTH PIN APPROX AS SHOWN.

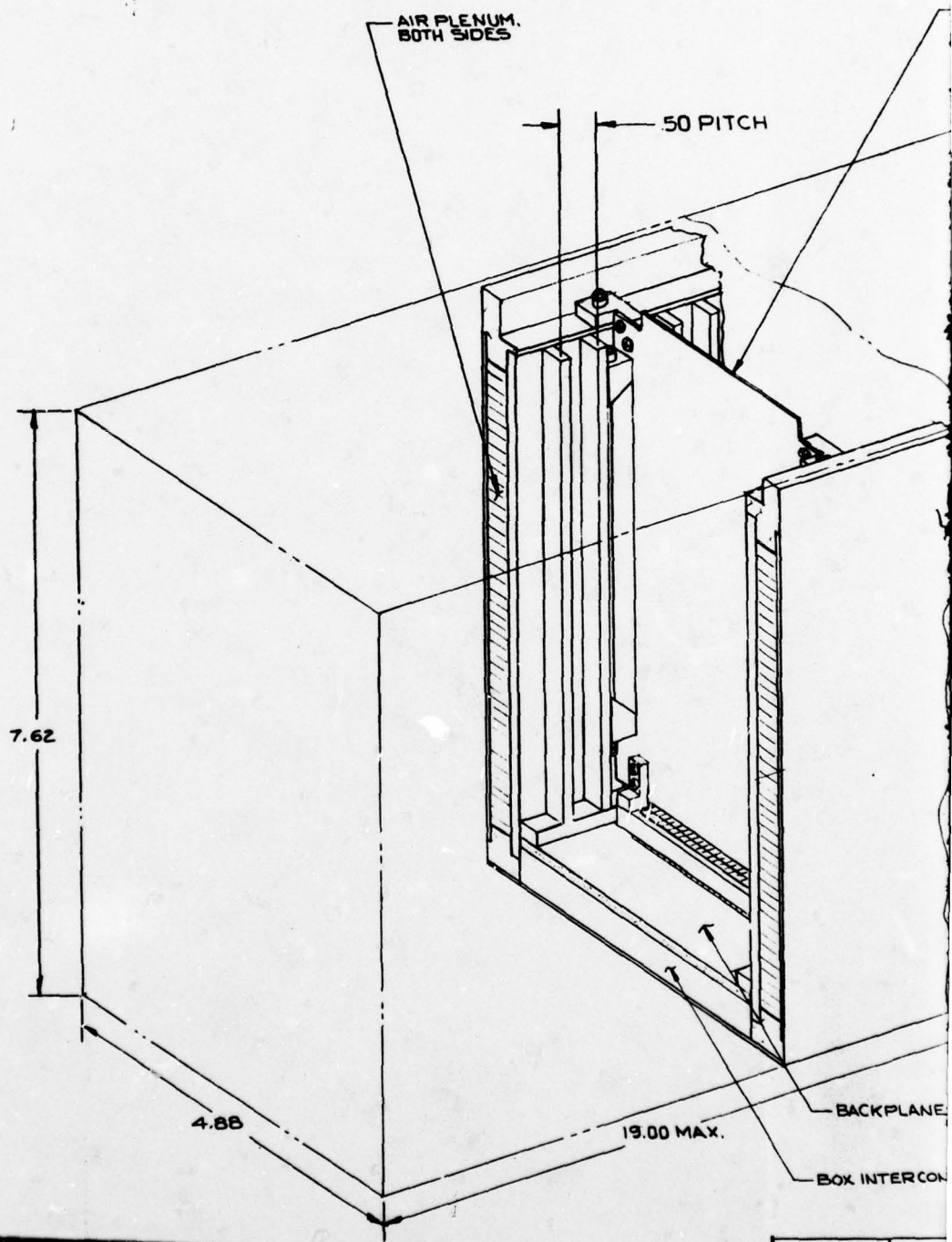


REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ADDED NOTES 2 & 4 ¹³ ADD CONN PIN NO. 5' 90N	2/21/77	
B	ADDED TRW LOGO 90N	3/3/77	
C	REVISED VIEW TO SHOW ALL TERMINALS 2). ADDED "COMPONENT SIDE" SILK SCREEN 90N	3/24/77	



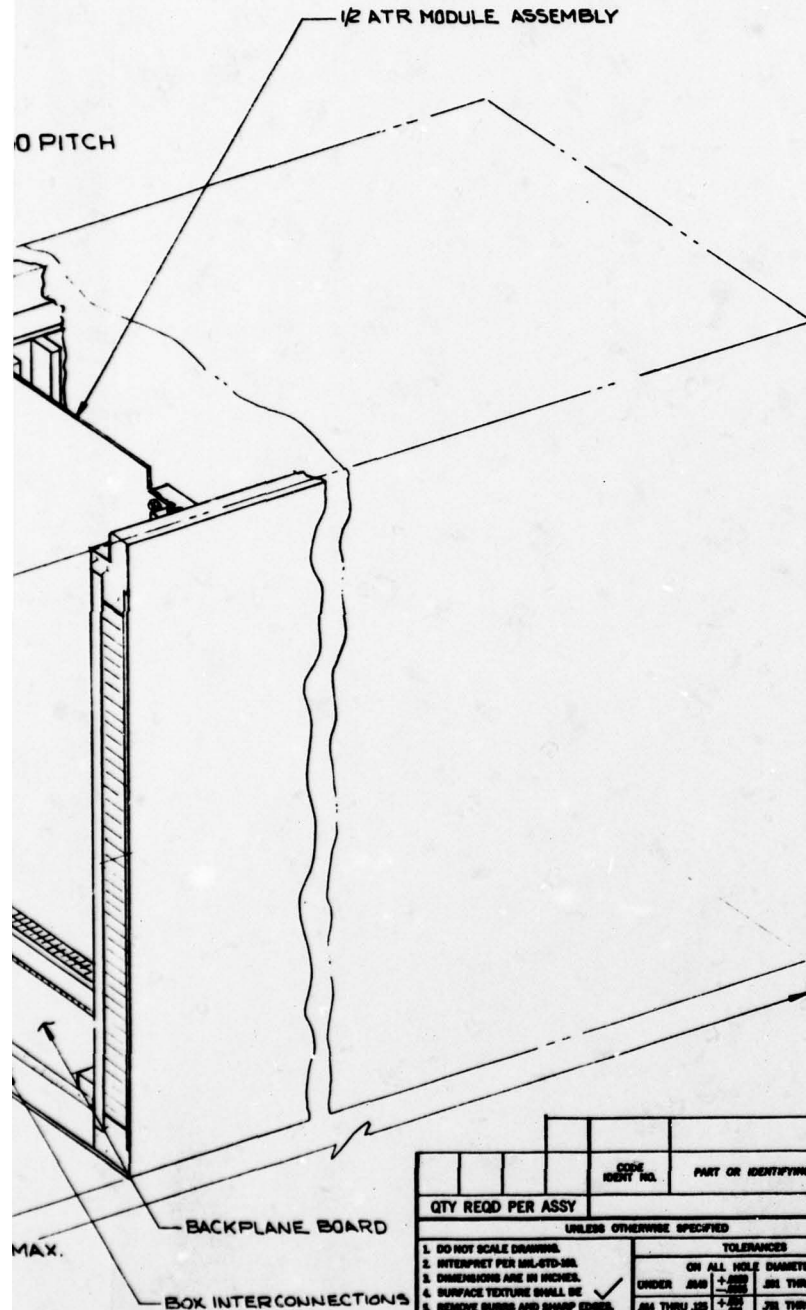
1824	700518	TERMINAL, STITCH - WIRE				3
1	-11	BOARD	2	G-10		2
-1	CODE IDENT NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPEC	REV

QTY REQD PER ASSY		PARTS LIST	
1. DO NOT SCALE DRAWING. 2. INTERPRET PER MIL-STD-188. 3. DIMENSIONS ARE IN INCHES. 4. SURFACE TEXTURE SHALL BE 5. REMOVE BURRS AND SHARP EDGES. 6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING. 7. DIMENSIONAL DATA IS FOR REFERENCE ONLY.		UNLESS OTHERWISE SPECIFIED TOLERANCES ON ALL HOLE DIAMETERS UNDER .250 +.000/-0.005 .251 THRU .750 +.001/-0.001 .751 THRU 1.000 +.002/-0.002 1.001 THRU 2.000 +.003/-0.003 2.001 THRU 3.000 +.004/-0.004 OVER 3.000 +.005/-0.005 ON DECIMAL DIMENSIONS: .001 ± .001 .01 ± .001 .1 ± .001 ON ANGULAR DIMENSIONS: MACHINED ± 0°30' LOCATING ± 0°30' FORMED CHAMFERS ± 0°	
FINISH		HEAT TREAT	
APPLICABLE SPECIFICATIONS		OTHER APPROVALS	
THE ABOVE TRW SYSTEMS GROUP SPEC IS PART OF THIS DRAWING		CONTRACT NO. DRAWN J. HOWE 1/11/77 CHECKED STRUCTURES MATERIAL/PROCESS ENGINEER SUPERVISOR PROJECT	
SAMS USED ON NEXT ASSY APPLICATION		THE FOLLOWING EQ'S HAVE BEEN ATTACHED TO THIS PRINT TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA MATRIX BOARD 2 SIZE CODE IDENT NO. D 11982 SK9131771 SCALE 2/1	



NOTES: UNLESS OTHERWISE SPECIFIED
1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



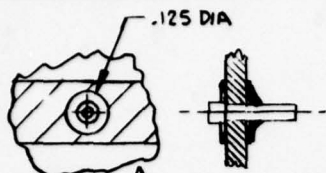
NOTES:
1. SCALE; NONE

QTY REQD PER ASSY	CODE IDENT NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	QTY	UNIT	ITEM NO.
PARTS LIST							
UNLESS OTHERWISE SPECIFIED				CONTRACT NO.			
1. DO NOT SCALE DRAWING. 2. INTERPRET PER MIL-STD-883. 3. DIMENSIONS ARE IN INCHES. 4. SURFACE TEXTURE SHALL BE 32 RMS UNLESS OTHERWISE SPECIFIED. 5. REMOVE BURRS AND SHARP EDGES. 6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING. 7. PARENTHESES DATA IS FOR REFERENCE ONLY.				DRAWN C.W.P. CHECKED STRUCTURES MATERIAL/PROCESS ENGINEER SUPERVISOR PROJECT OTHER APPROVALS			
TOLERANCES ON ALL HOLE DIAMETERS UNDER .250 $\pm .005$.251 THRU .500 $\pm .010$.501 THRU .750 $\pm .015$.751 THRU 1.000 $\pm .020$ 1.001 THRU 2.000 $\pm .030$ 2.001 THRU 5.000 $\pm .040$ 5.001 THRU 10.000 $\pm .050$ OVER 10.000 $\pm .060$				THE FOLLOWING BO'S HAVE BEEN ATTACHED TO THIS PRINT			
ON DECIMAL DIMENSIONS: .001 $\pm .001$.002 $\pm .002$.003 $\pm .003$.004 $\pm .004$.005 $\pm .005$.006 $\pm .006$.007 $\pm .007$.008 $\pm .008$.009 $\pm .009$.010 $\pm .010$.011 $\pm .011$.012 $\pm .012$.013 $\pm .013$.014 $\pm .014$.015 $\pm .015$.016 $\pm .016$.017 $\pm .017$.018 $\pm .018$.019 $\pm .019$.020 $\pm .020$.021 $\pm .021$.022 $\pm .022$.023 $\pm .023$.024 $\pm .024$.025 $\pm .025$.026 $\pm .026$.027 $\pm .027$.028 $\pm .028$.029 $\pm .029$.030 $\pm .030$.031 $\pm .031$.032 $\pm .032$.033 $\pm .033$.034 $\pm .034$.035 $\pm .035$.036 $\pm .036$.037 $\pm .037$.038 $\pm .038$.039 $\pm .039$.040 $\pm .040$.041 $\pm .041$.042 $\pm .042$.043 $\pm .043$.044 $\pm .044$.045 $\pm .045$.046 $\pm .046$.047 $\pm .047$.048 $\pm .048$.049 $\pm .049$.050 $\pm .050$.051 $\pm .051$.052 $\pm .052$.053 $\pm .053$.054 $\pm .054$.055 $\pm .055$.056 $\pm .056$.057 $\pm .057$.058 $\pm .058$.059 $\pm .059$.060 $\pm .060$.061 $\pm .061$.062 $\pm .062$.063 $\pm .063$.064 $\pm .064$.065 $\pm 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$\pm .132$.133 $\pm .133$.134 $\pm .134$.135 $\pm .135$.136 $\pm .136$.137 $\pm .137$.138 $\pm .138$.139 $\pm .139$.140 $\pm .140$.141 $\pm .141$.142 $\pm .142$.143 $\pm .143$.144 $\pm .144$.145 $\pm .145$.146 $\pm .146$.147 $\pm .147$.148 $\pm .148$.149 $\pm .149$.150 $\pm .150$.151 $\pm .151$.152 $\pm .152$.153 $\pm .153$.154 $\pm .154$.155 $\pm .155$.156 $\pm .156$.157 $\pm .157$.158 $\pm .158$.159 $\pm .159$.160 $\pm .160$.161 $\pm .161$.162 $\pm .162$.163 $\pm .163$.164 $\pm .164$.165 $\pm .165$.166 $\pm .166$.167 $\pm .167$.168 $\pm .168$.169 $\pm .169$.170 $\pm .170$.171 $\pm .171$.172 $\pm .172$.173 $\pm .173$.174 $\pm .174$.175 $\pm .175$.176 $\pm .176$.177 $\pm .177$.178 $\pm .178$.179 $\pm .179$.180 $\pm .180$.181 $\pm .181$.182 $\pm .182$.183 $\pm .183$.184 $\pm .184$.185 $\pm .185$.186 $\pm .186$.187 $\pm .187$.188 $\pm .188$.189 $\pm .189$.190 $\pm .190$.191 $\pm .191$.192 $\pm .192$.193 $\pm .193$.194 $\pm .194$.195 $\pm .195$.196 $\pm .196$.197 $\pm .197$.198 $\pm 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$\pm .531$.532 $\pm .532$.533 $\pm .533$.534 $\pm .534$.535 $\pm .535$.536 $\pm .536$.537 $\pm .537$.538 $\pm .538$.539 $\pm .539$.540 $\pm .540$.541 $\pm .541$.542 $\pm .542$.543 $\pm .543$.544 $\pm .544$.545 $\pm .545$.546 $\pm .546$.547 $\pm .547$.548 $\pm .548$.549 $\pm .549$.550 $\pm .550$.551 $\pm .551$.552 $\pm .552$.553 $\pm .553$.554 $\pm .554$.555 $\pm .555$.556 $\pm .556$.557 $\pm .557$.558 $\pm .558$.559 $\pm .559$.560 $\pm .560$.561 $\pm .561$.562 $\pm .562$.563 $\pm .563$.564 $\pm .564$.565 $\pm .565$.566 $\pm .566$.567 $\pm .567$.568 $\pm .568$.569 $\pm .569$.570 $\pm .570$.571 $\pm .571$.572 $\pm .572$.573 $\pm .573$.574 $\pm .574$.575 $\pm .575$.576 $\pm .576$.577 $\pm .577$.578 $\pm .578$.579 $\pm .579$.580 $\pm .580$.581 $\pm .581$.582 $\pm .582$.583 $\pm .583$.584 $\pm .584$.585 $\pm .585$.586 $\pm .586$.587 $\pm .587$.588 $\pm .588$.589 $\pm .589$.590 $\pm .590$.591 $\pm .591$.592 $\pm .592$.593 $\pm .593$.594 $\pm .594$.595 $\pm .595$.596 $\pm .596$.597 $\pm .597$.598 $\pm .598$.599 <							

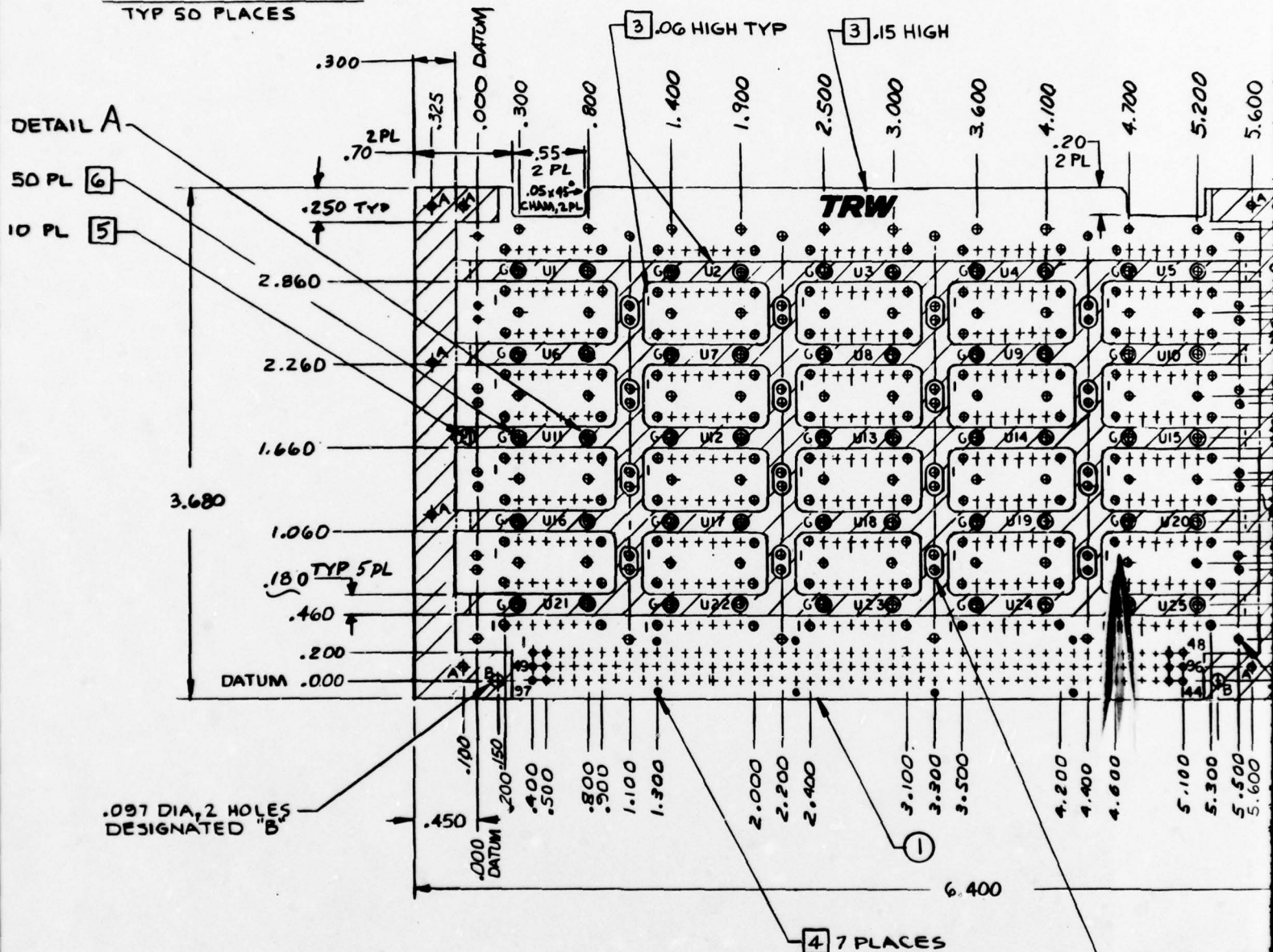
Hand-drawn diagram of a bolted connection. The diagram shows a central bolt with a nut and washer. Dimensions are indicated by arrows and handwritten text:

- 153 (vertical dimension from top flange to bolt center)
- 260 (vertical dimension from bottom flange to bolt center)
- 439 (vertical dimension from top flange to bottom flange)
- 192 MIN (horizontal dimension from bolt center to left edge of flange)
- 202 NOM (horizontal dimension from bolt center to right edge of flange)
- S (horizontal force arrow pointing left)
- P (vertical force arrow pointing down)

2 403



DETAIL A SCALE 4/1
TYP 50 PLACES



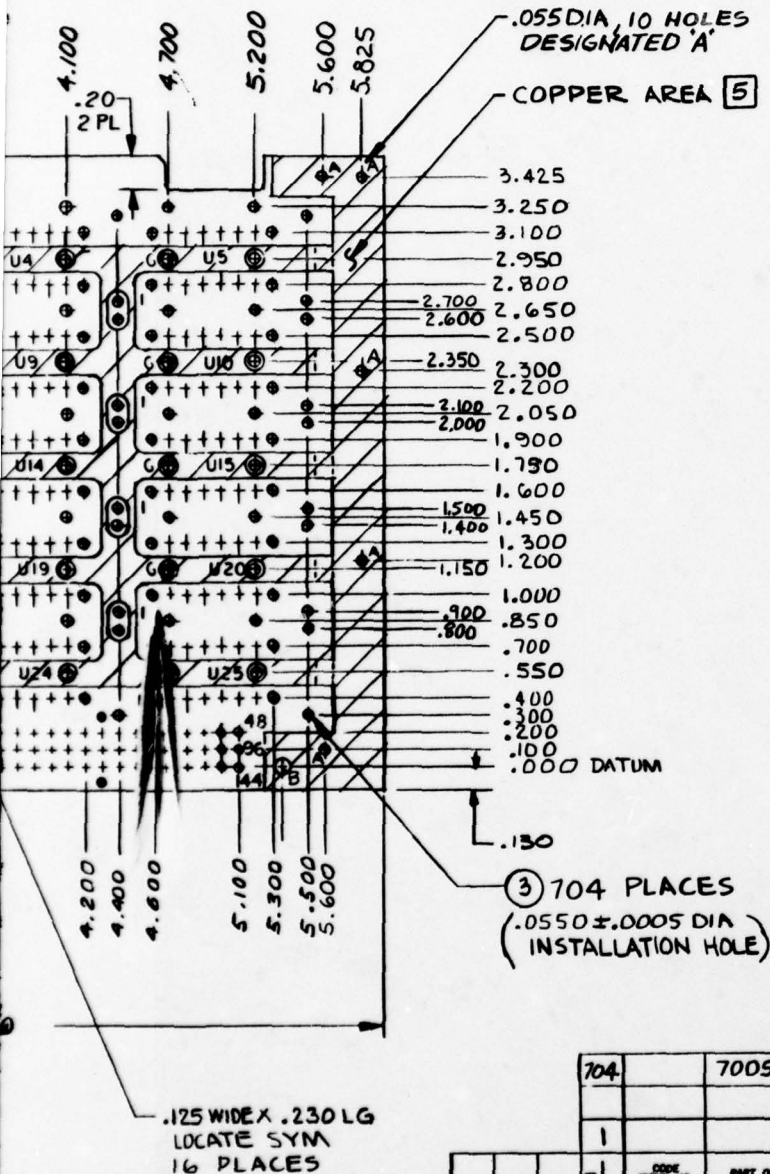
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL TERMINALS TO BE LOCATED ON .100 CENTERS
2. BOARD MATERIAL: .062 THK EPOXY GLASS CORE, BLUE COLOR, WITH 2 OZ COPPER FOIL BOTH SIDES, SOLDER PLATED.
3. SILKSCREEN CHARACTERS WHITE, LOCATE APPROX AS SHOWN.
4. SILKSCREEN DOTS WHITE, .03 DIA. LOCATE ON EVERY TENTH PIN APPROX AS SHOWN.
5. COPPER AREA ON FAR SIDE SAME AS NEAR SIDE EXCEPT FOR .10 WIDE ETCH CUT ON FAR SIDE. TYP 10 PLACES
6. SOLDER ITEM 3 TO NEAR SIDE CIRCUITRY WHERE DESIGNATED "G" SOLDER ADJACENT TERMINAL TO FAR SIDE CIRCUITRY ONLY.

.125 WIDE X .230
LOCATE SYM
16 PLACES

SAMS
USED ON NEXT
APPLICATION

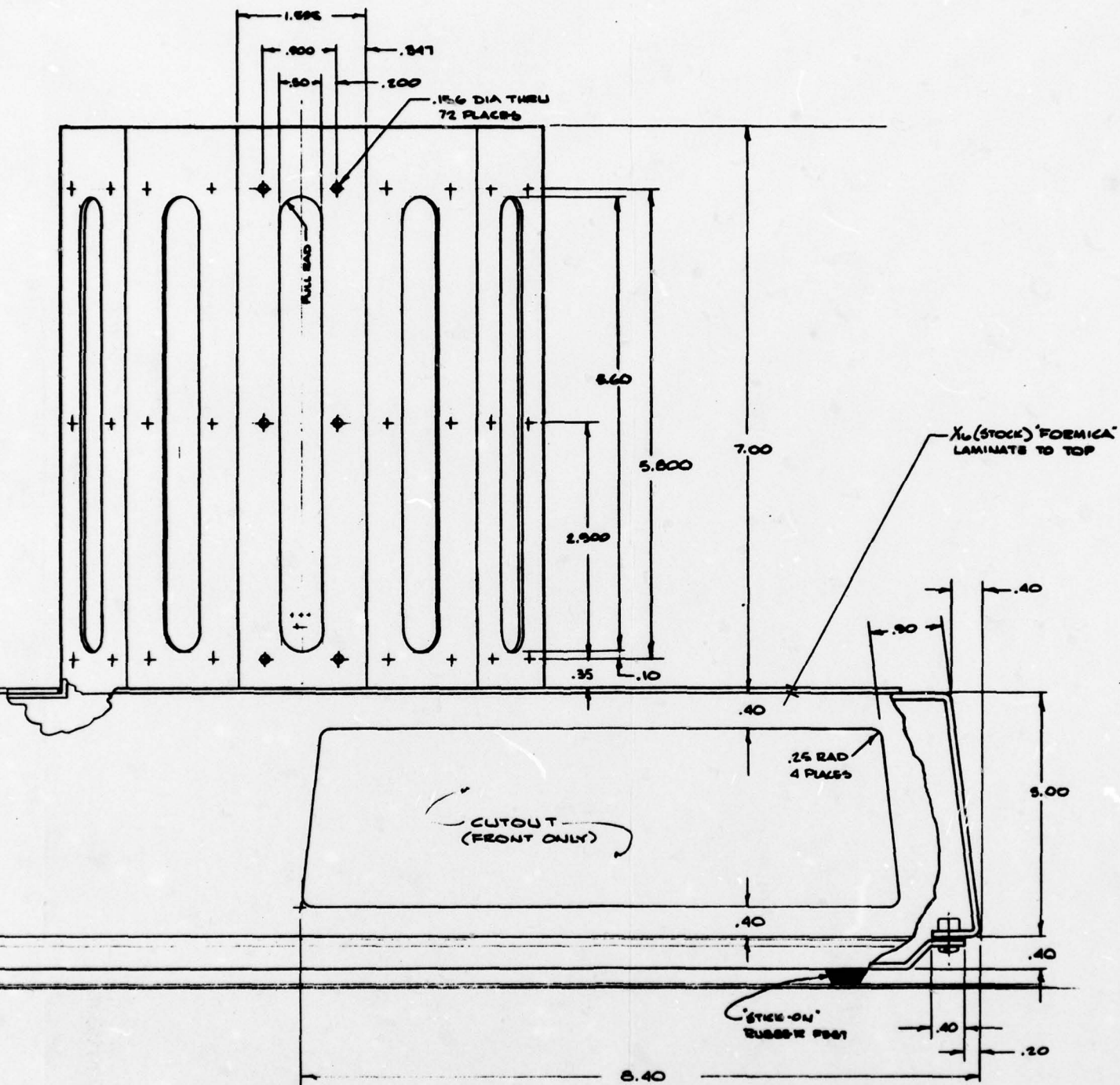
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ADDED "B" DESIGNATED HOLES	2/2/77	
B	REVISED CONNECTOR SILKSCREEN NO. 5.	2/12/77	
C	ADDED TRW LOGO	3/1/77	
D	(1) ITEM 3 WAS 654 REQD. (2) ADDED DETAIL 'A' & ASSOCIATED DIM. (3) REVISED NOTE 3 WAS: --- COPPER FOIL 1 SIDE (4) ADDED NOTES 5 & 6 (5) REVISED COPPER AREA EXTENSIVELY FOR WAS CONDITION SEE 'C' REVISION	3/17/77	



704	700518	TERMINAL, STITCH-WIRE				3
						2
1	-11	BOARD	2	G-10		1

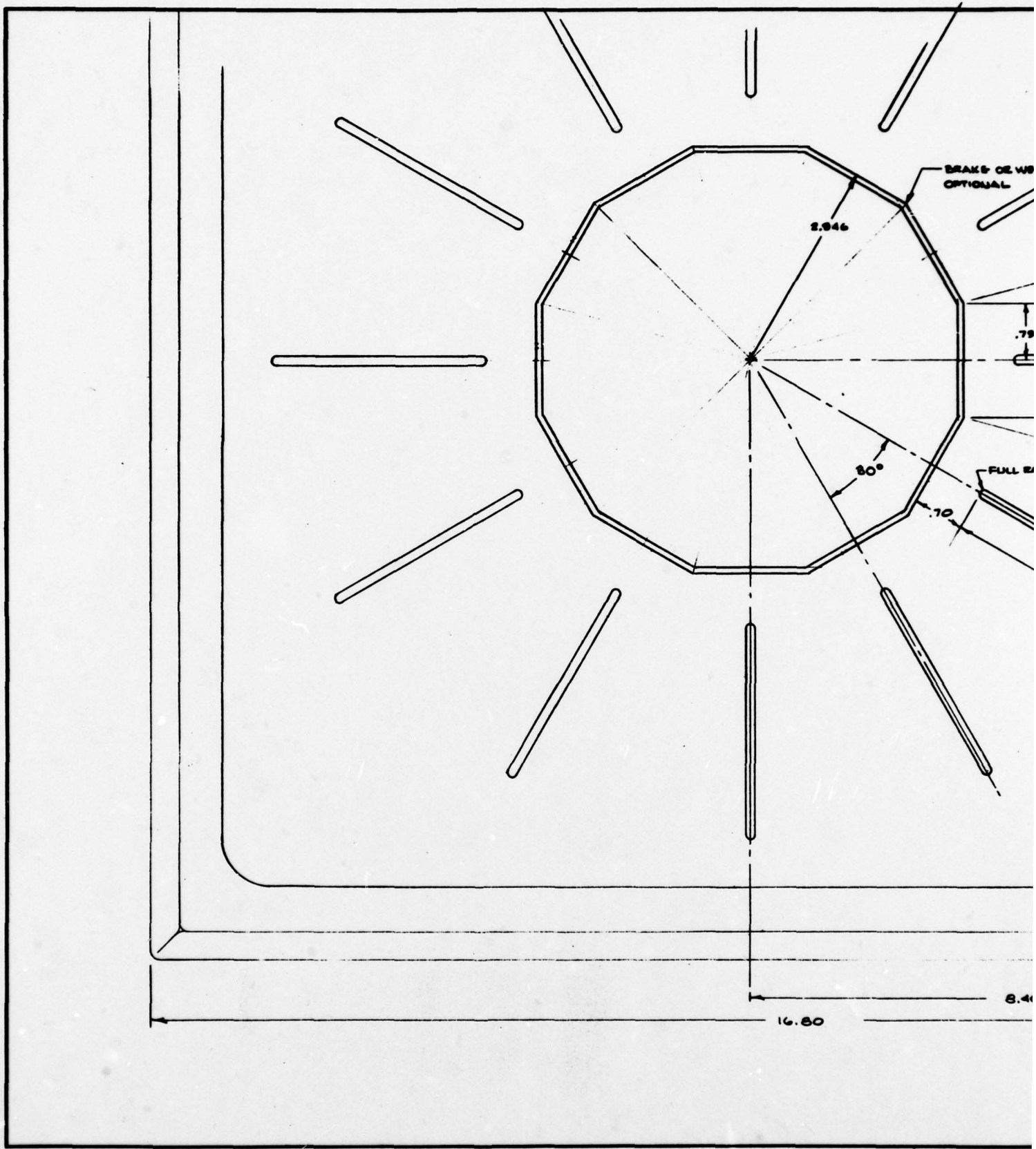
QTY REQD PER ASSY		CODE IDENT NO.		PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION		MATERIAL		SPEC		REV DES		ZONE		ITEM NO.	
1		-		11		BOARD		2		G-10							
PARTS LIST																	
UNLESS OTHERWISE SPECIFIED																	
1. DO NOT SCALE DRAWING.																	
2. INTERPRET PER MIL-STD-188.																	
3. DIMENSIONS ARE IN INCHES.																	
4. SURFACE TEXTURE SHALL BE																	
5. REMOVE BURRS AND SHARP EDGES.																	
6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING.																	
7. PARENTHEetical DATA IS FOR REFERENCE ONLY.																	
TOLERANCES																	
ON ALL HOLE DIAMETERS																	
UNDER .250 +.0025 - .0025																	
.251 THRU .750 +.005 - .005																	
.751 THRU 1.000 +.0075 - .0075																	
1.001 THRU 2.000 +.010 - .010																	
2.001 THRU 3.000 +.0125 - .0125																	
OVER 3.000 +.015 - .015																	
ON DECIMAL DIMENSIONS:																	
.XXX ± .005																	
.XX ± .0025																	
X ± .001																	
ON ANGULAR DIMENSIONS:																	
MACHINED ± 1°																	
LOCATING ± 1°																	
FORMED ± 1°																	
CHAMFERS ± .01																	
FINISH																	
HEAT TREAT																	
APPLICABLE SPECIFICATIONS																	
THE ABOVE TRW SYSTEMS GROUP SPECS FORM A PART OF THIS DRAWING																	
CONTRACT NO.																	
DRAWN J. HOWE 3/1/77																	
CHECKED																	
STRUCTURES																	
MATERIAL/PROCESS																	
ENGINEER																	
SUPERVISOR																	
PROJECT																	
OTHER APPROVALS																	
THE FOLLOWING EDS HAVE BEEN ATTACHED TO THIS PRINT																	
TRW																	
ONE SPACE PARK - REDONDO BEACH, CALIFORNIA																	
CARD, STITCH WIRE																	
SIZE		CODE IDENT NO.															
D		11982		SK9128771													
SCALE 2/1		405															

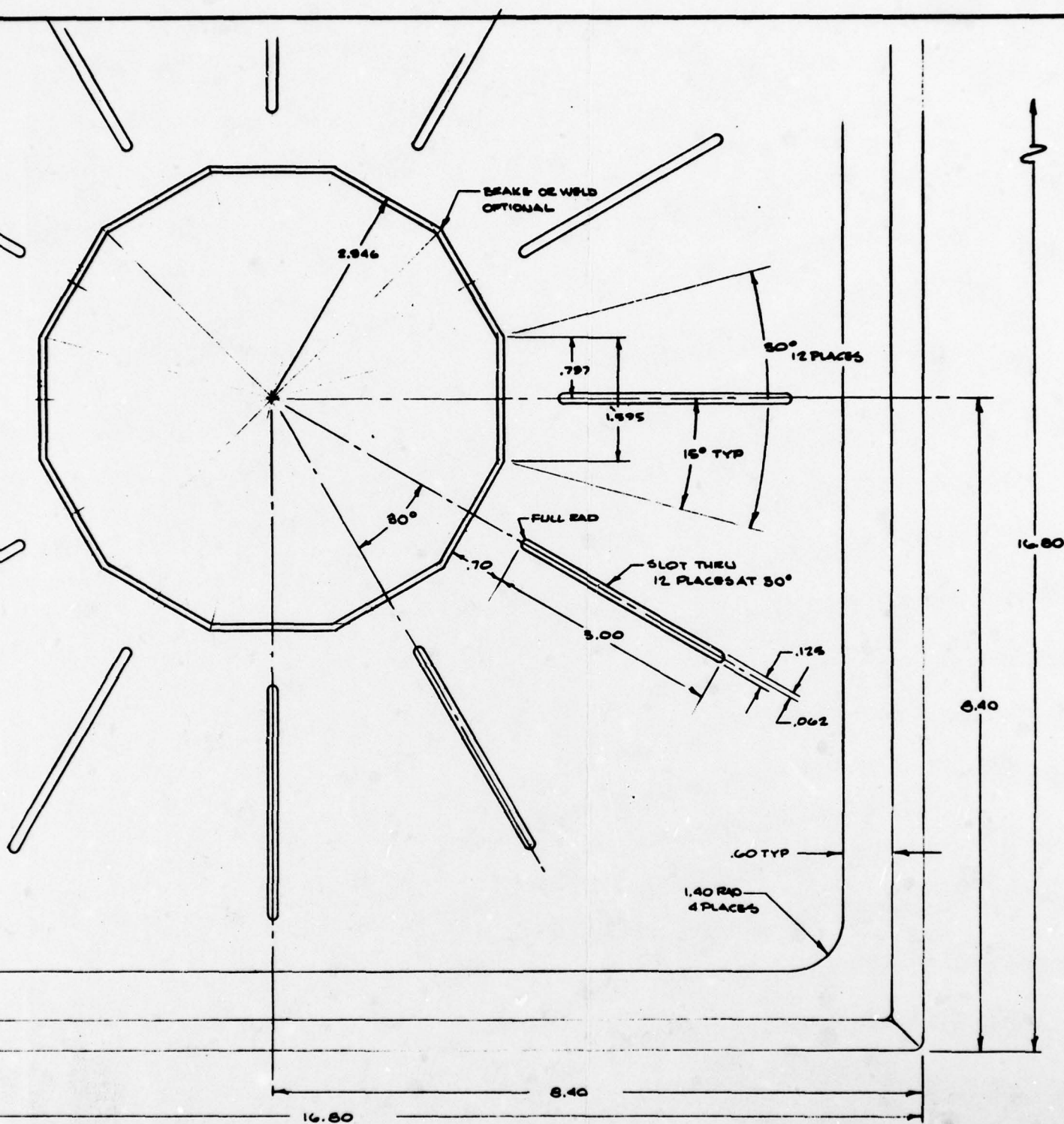
SAMS	
USED ON	APPLICATION
NEXT ASSY	NEXT ASSY
NEXT CITY	NEXT CITY



FRONT VIEW

SIZE	CODE IDENT NO.	L 296 299
C		
SCALE		UNIT





SIZE	CODE IDENT NO.	L 296 299
C		
SCALE		DRY

APPENDIX L

DOPPLER WIPEOFF (DWO) FUNCTIONAL DESCRIPTION

L.1 Introduction

The overall function of the Doppler Wipeoff (DWP) module is to provide a Local Oscillator (LO) signal that is shifted in frequency by the doppler shift presented in the RF signal. The magnitude and direction of the shift are determined in processing circuits outside the DWP module; a command word is then furnished to the DWP module. The module using the command word plus 70 MHz fixed reference signal synthesizer a $70 \text{ MHz} \pm 0 \text{ to } 15 \text{ KHz}$ LO signal. (A 10 MHz clock is also used in the process.)

The module can be divided into two separate functions:

- A direct digital sythesizer (DDS) that generates both the sine and cosine function of the doppler frequency (f_d).
- A single sideband modulation circuit that combines $\sin f_s$ $\cos f_s$ with $\sin 70 \text{ M}$ and $\cos 70 \text{ M}$ to generate $70 \text{ M} \pm f_d$. The choice of + or - f_s is accomplished by inverting the relationship of \sin and $\cos f_s$ in the DDS.

L.2 Direct Digital Synthesizer (DDS)

The DDS takes the basic DDS scheme and adds two major changes: (1) both the sine and cos functions are generated, (2) it works in terms of negative frequency.

Table L-1. The DDS

<u>REQUIREMENT</u>	<u>CAPABILITY</u>
1 Hz resolution (step size)	1.19 Hz ⁽¹⁾
16 Bit maximum control word Input	Full 16 bits used
<u>+15</u> KHz output	<u>+19.5</u> KHz ⁽²⁾ (The (-) is implemented by investing the sin-cos relationship)
100 Hz/sec	39 KHz per 1/2.5 MHz x 2 clocks = 43 MHz per sec So actual limit is the LPF = 20 KHz
50 Hz/sec/sec	TBD

(1)

$$\begin{aligned}\Delta f &= \frac{f_c}{N} \\ &= \frac{2.5 \times 10^6}{2^{21}} \\ &= \frac{2,500,000}{2,097,152}\end{aligned}$$

$$\Delta f = 1.19$$

f_c = Clock frequency
N = Accumulator size

(2)

$$\begin{aligned}f_{\max} &= 1/2 \Delta f \cdot \lambda \\ &= \frac{1.19 (2^{15})}{2}\end{aligned}$$

λ = Accumulator modulus

$$f_{\max} = 19.5 \text{ KHz}$$

L.2 Direct Digital Synthesizer (DDS)

The DDS takes the basic DDS scheme and adds two major changes: (1) both the sine and cos functions are generated, (2) it works in terms of negative frequency.

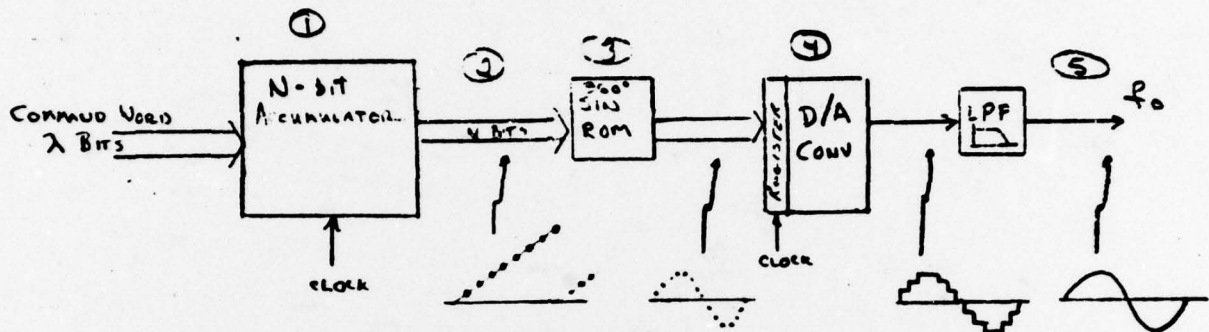


Figure L-1. Basic DDS

- ① The command word is repeatedly added to the accumulator with each clock pulse.
- ② A linearly increasing word is generated. When the accumulator overflows, this ramp repeats. (If N/λ is not an integer, the ramp begins at a different level each time.)
- ③ The ramp word is used to address a ROM which translates the ramp to a binary coded sine wave. (Consider the ramp as a binary coding of the phase.)
- ④ The binary sine drives a D to A converter.
- ⑤ A low pass filter eliminates the sampling steps.

The system still uses one accumulator and one SINE ROM, but they are multiplexed between two D/A registers and D/As.

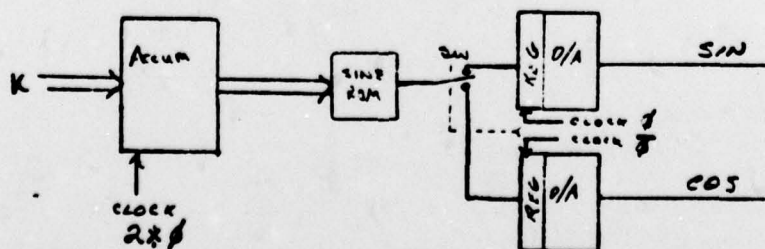
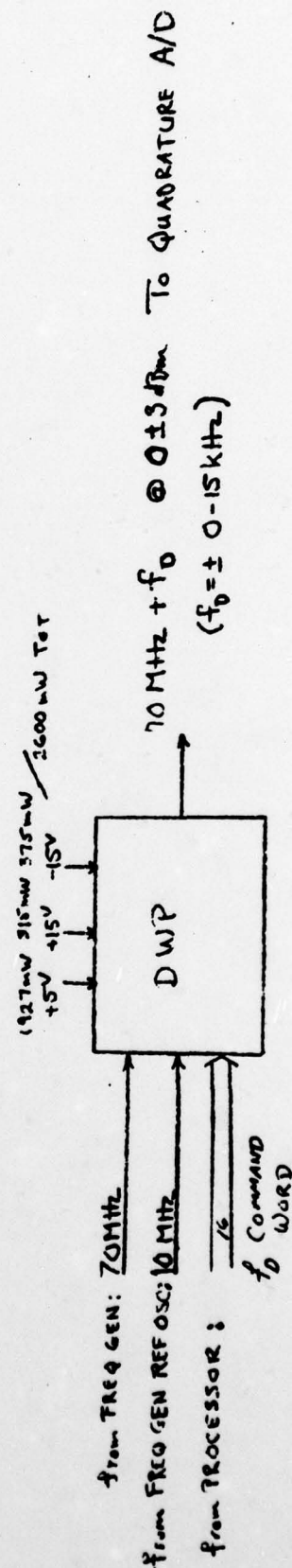


Figure L-2. Sine/Cosine Generator

Table L-2. Doppler Wipe Off Module

- USES DIRECT DIGITAL SYNTHESIS TO GENERATE A SINE AND COS SIGNAL AT THE DOPPLER FREQUENCY
- CONTROLLED DIRECTLY BY A COMMON WORD FROM THE PROCESSOR MODULE
- COMBINES THE INTERNALLY GENERATED f_0 WITH 70 MHZ USING SINGLE SIDEBAND MODULATION TECHNIQUE TO PRODUCE 70 MHZ PLUS OR MINUS f_0 .
- NO FILTERS REQUIRED
- NO OFFSET FREQUENCY REQUIRED



The sin/cos switch function is implemented by alternate clocking (ϕ and $\bar{\phi}$ of the two registers). The command word and accumulator are set up so that two alternating ramps are generated instead of one.

The ramp out of the accumulator represents the phase of the signal.

The relationship between sine and cosine is

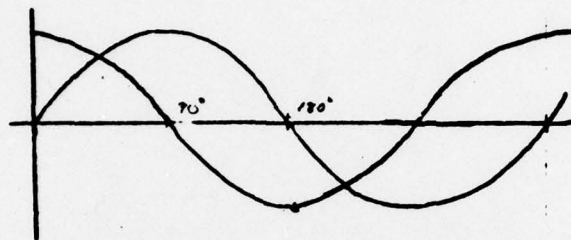


Figure L-3. Sine/Cosine

but note that both must come from the same ROM so

$$\cos [\theta(t)] = \sin [\theta(t) + 90^\circ].$$

For example, at $t = 0$, the sin is 0 but the cos is 1 so the SINE ROM must be addressed for 0° to give the sin and then $(0^\circ + 90^\circ) = 90^\circ$ to give the cos value

To use the accumulator in this manner means that first 90° must be added to its value to go from sin to cos and 270° must be added to get back to a sin value (a net change of 360°). At the same time the accumulator is being incremented alternately by $+90^\circ$, $+270^\circ$, $+90^\circ$, $+270^\circ$, ..., the single step (k) is also being added. As a result, where a basic DDS accumulator output would be

$$0, k, 2k, 3k, 4k \dots$$

we now have

$$0, k + 90^\circ, 2k + 360^\circ, 3k + 450^\circ, \dots$$

which, if sampled alternately is

$$\begin{array}{ccccccc} 0 & & 2k + 360^\circ & & \dots & & \\ & k + 90^\circ & & 3k + 450^\circ & & \dots & \end{array}$$

Removing the 360°

$$\begin{array}{ccccccc} \sin & & 0 & & 2k & & \\ \cos & & k + 90^\circ & & & & 3k + 90^\circ \end{array}$$

An additional feature of the DDS is the ability to invert the sin-cos relationship. This is part of the implementation of the negative frequency capability, the remainder of which is described in discussion of the single sideband modulation portion of the circuit. Thus, if the negative representation of a number (using, for example, 2's complement convention) is presented at the command word input, the output will be decremented instead of incremented.

L.3 Single Sideband Modulator

This portion of the circuit combines the sin and cos terms of the doppler signal with the sin and cos terms of the 70 MHz LO to product either $70 \text{ MHz} + f_c$ or $70 \text{ MHz} - f_c$.

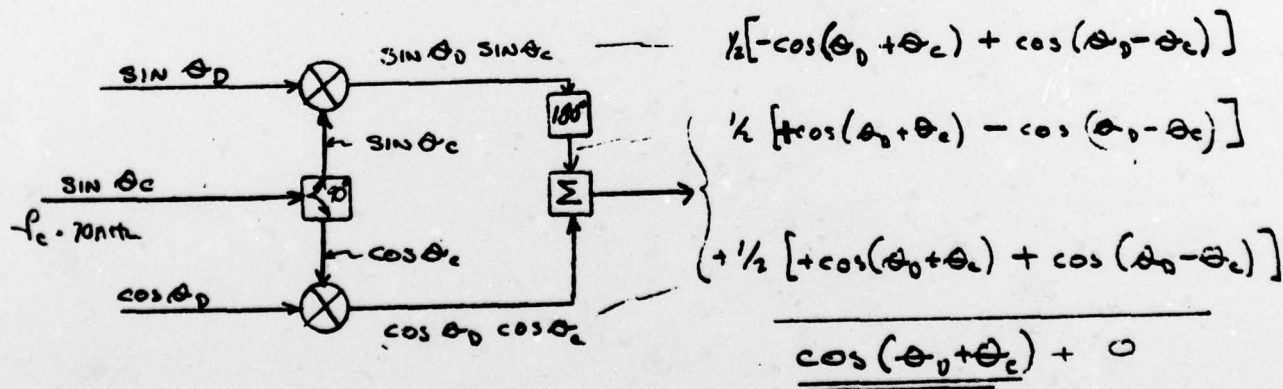


Figure L-4. Block Diagram and Algebra

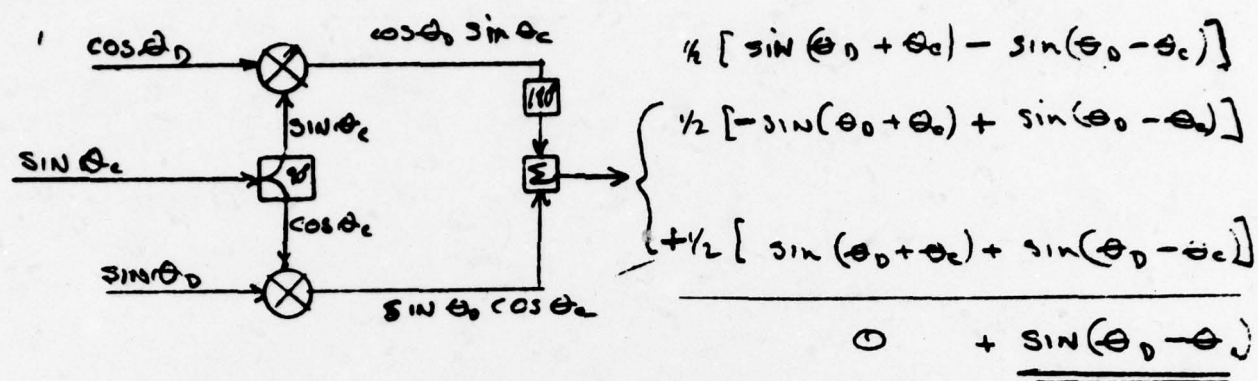
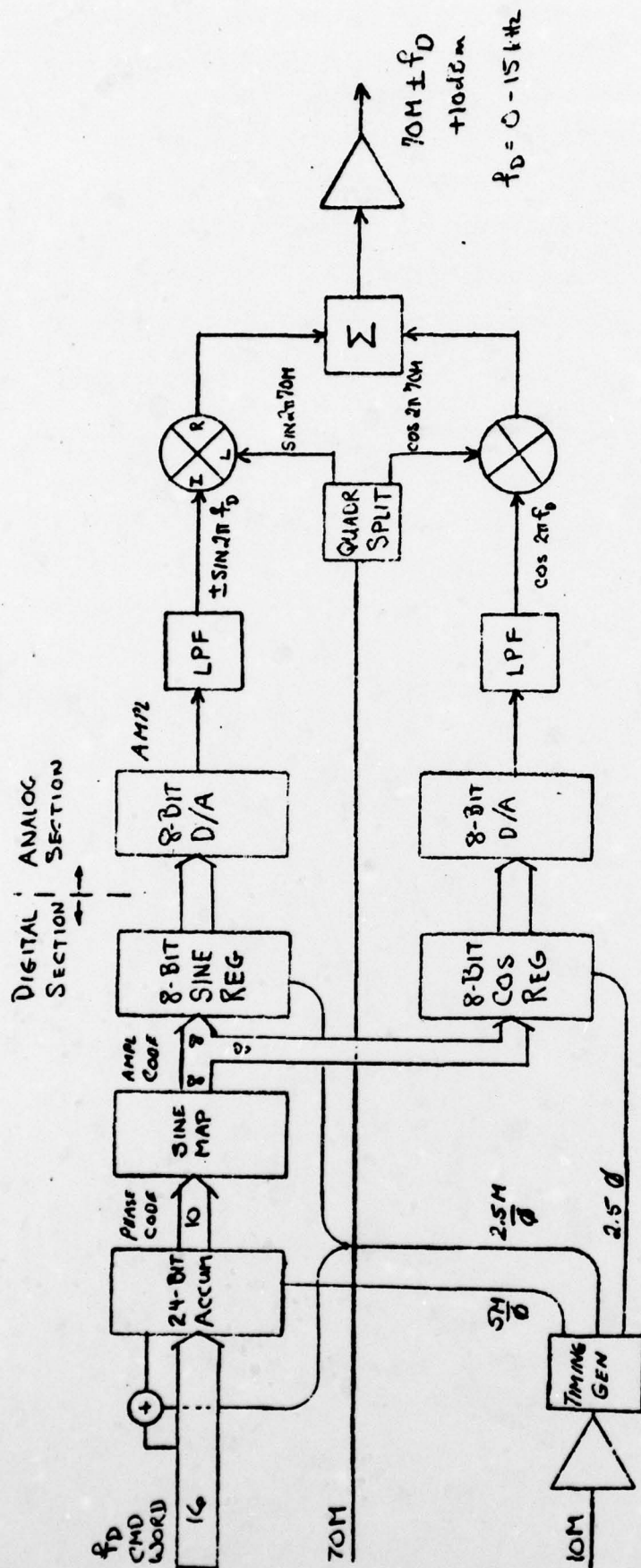
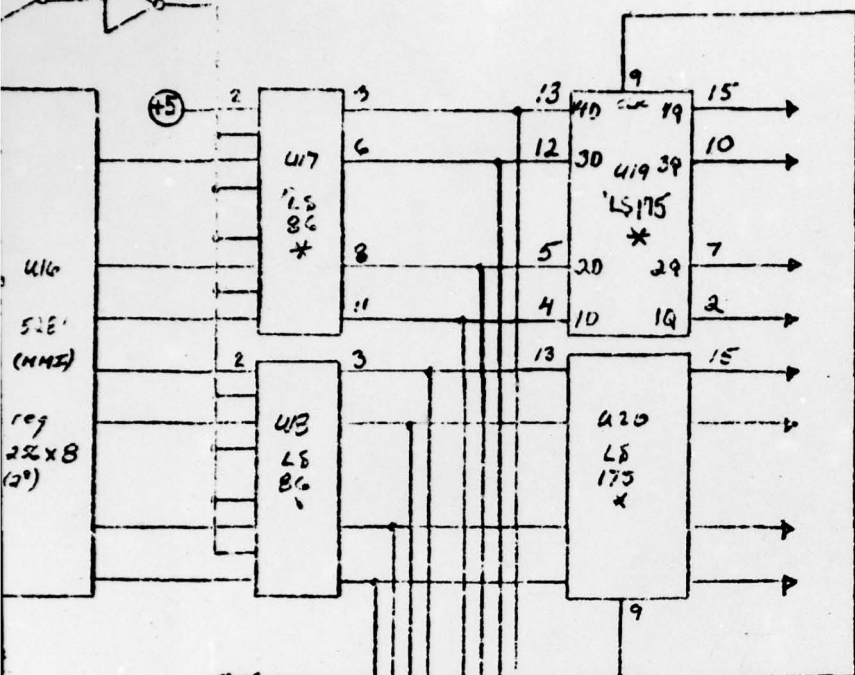


Figure L-5. Difference Frequency

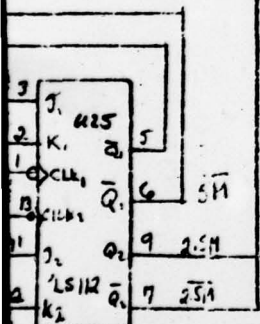
DOPPLER WIPEOFF MODULE



2/6 U23



To SIN
DAC



To COS
DAC

Not Used:

C28-50
U12, 13

Last Used:

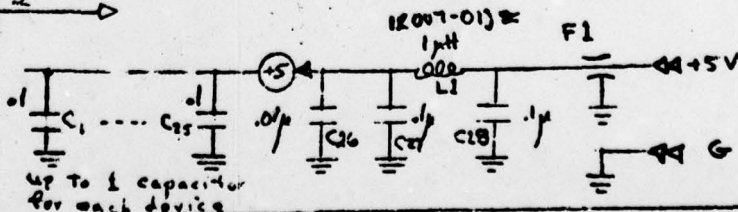
U25, C28, R52, L1, F1

Board limited to 25 I.C.'s

Ver	GND	-15
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586	QUAD EXOR	14	7
283	4BIT FULL ADD	16	8
174	HEX'D FL	16	8
175	QUAD'D P-P	16	8
112	DUAL J-K FL	16	8
04	HEX INV	14	8
K	COMPARATOR TTL B3,10	12	8,4
5281	90° SIN ROM	24	12

ASSIGNMENTS ON THESE DEVICES MAY
BE CHANGED FOR BETTER LAYOUT



SAM - DOPPLER WIPEOFF (DWP)
MODULE

DIGITAL SECTION

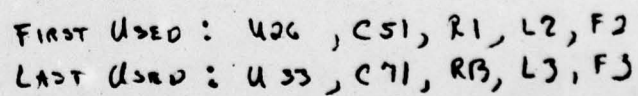
M.D. 3/7/77

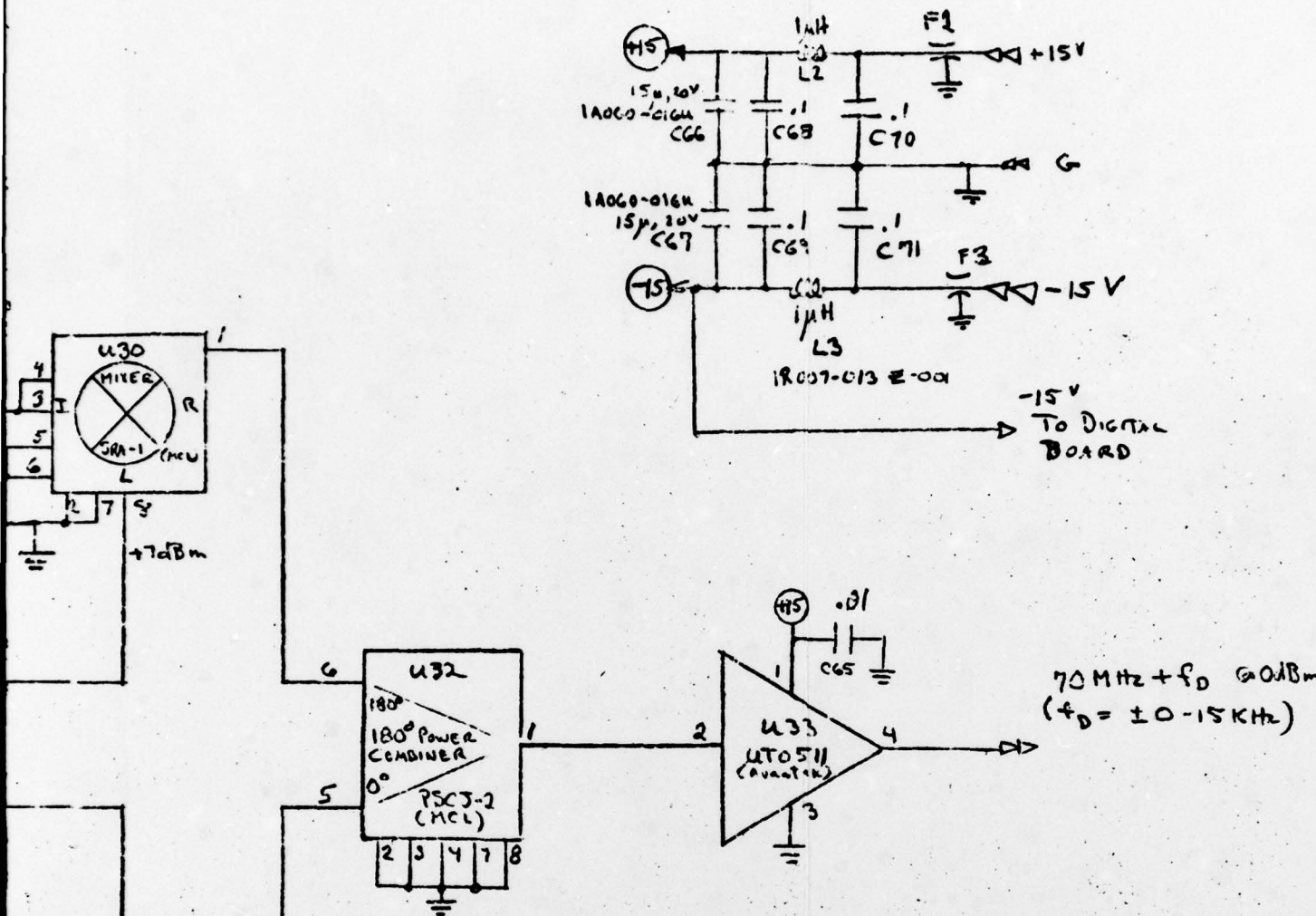
420 P. 1 of 2

2

Power Consumption

CONFIGURATION				PARTS LIST				ITEM NO.	CKT REF	SPECIFICATION OR MANUFACTURER	QTY REQD	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V	QTY REQD 5V	QTY REQD 12V	QTY REQD 15V
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UNLESS OTHERWISE NOTED:

Only CAPACITORS ARE M39014/02-1270

D1µ " " M39014/01-1277

ALL RESISTORS ARE RNC55HxxxxFR, FILM, 1/8W, 1%, VALUES IN OHMS

R1, L2, F2
R3, L3, F3

